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Adaptive And Recursive Vedic Karatsuba Multiplier Using Non Linear Carry Select Adder

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Abstract

Multipliers play a vital role in any applications like signal processing, image processing, floating-point processors etc. These applications require efficient binary multiplications, but it is most powerful as well as time consuming process. An efficient binary multiplication is proposed to reduce the delay. Vedic Karatsuba multiplier is an efficient algorithm which can be used to reduce the delay. The combination of adaptive and recursive approach of Vedic Karatsuba algorithm along with Non - Linear Carry Select Adder is implemented to get the better results. Multiplier designs are coded in Verilog by using Xilinx software.

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Introduction

Multipliers are very important in many applications like image processing, signal processing etc.[1-20] The final goal of researcher's is to work on the multipliers, which can have a very less power consumption, greater speed, less area etc.[21-25]

'Add and Shift' algorithm is one of the common multiplication process. The functional operation of the multiplier is the measure of partial products that are added in the parallel multipliers. The multiplier algorithm combined with non - linear carry select adder algorithm is used to decrease the partial products count that are added.[26-30]

A. Basic Multiplication

1 3 8 * 2 6 5

6 9 0 (Here 138 is multiplied by 5)

8 2 8 (Here 138 is multiplied by 6 and one position is shifted to the left)

+ 2 7 6 (Here 138 is multiplied by 2 and two positions are shifted to the left)

3 6 5 7 0

B. Binary Multiplication

Binary multiplication process is similar to the digit multiplication. In binary multiplication, addition as well as shifting of the digits is performed. In binary multiplication, '0' and '1' are the only digits on which the addition and shifting operations are done.

The multiplication and addition values of the binary digits 'X' and 'Y' are shown in the Table1.

To perform binary multiplication, every digit of the first binary number should be multiplied with every digit of the second binary number, and then an addition operation has to be performed to obtain the final result. The below is the example of binary multiplication that is performed between two binary numbers.

Table 1: Multiplication And Addition Values of Binary Numbers

Binary Digits		Multiplication Value	Addition Value
X	Y	X * Y	X + Y
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1 along with carry =1

```
  1010  * 101
     1010
   0000
+ 1010
 110010
```

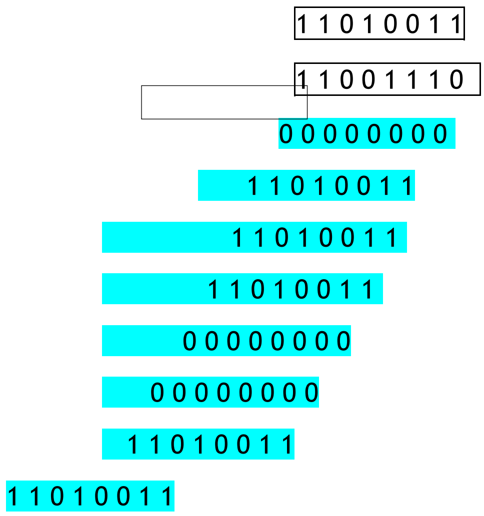
C. Wallace Tree Multiplication

Wallace tree multiplication is the fastest method that is used to multiply the binary integers. Wallace tree multiplication consists of 3 stages.

- Stage1: Partial products
- Stage2: Partial product addition
- Stage3: Final addition

Stage1: Partial products

Two binary integers (represented in red colour) are taken and product (represented in blue colour) is obtained.



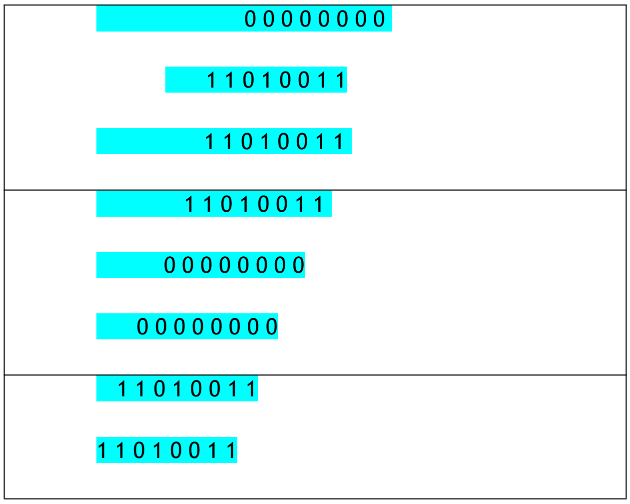
Stage2: Partial Product addition , step1

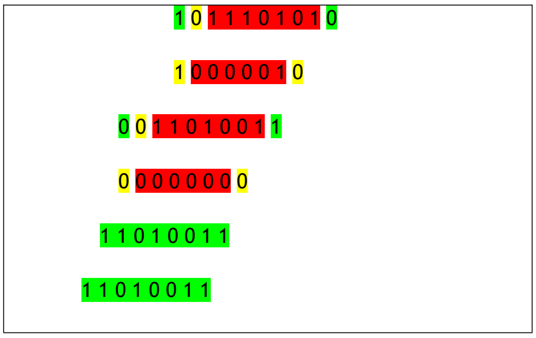
Partial products obtained in stage1 are grouped as three rows and the digits in each row are added at a time. Hence, two set of rows will be obtained as a result of addition of each three row set. First row will result the sum and the second row will result the carry-out that is obtained in the process.

Full adder output is represented in red colour

Half adder output is represented in yellow colour

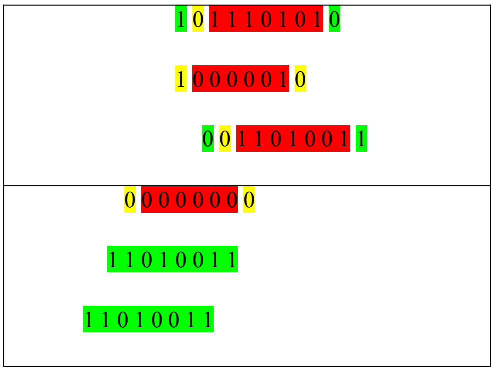
Remaining (left alone) are represented in green colour

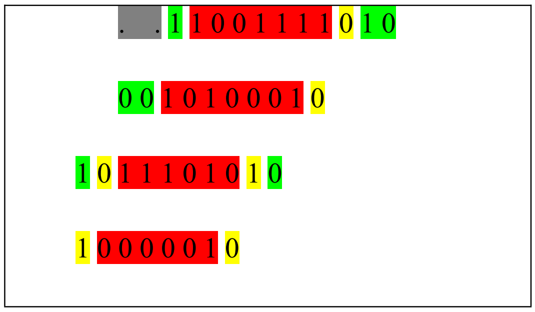




Stage2: Partial Product addition , step2

The same process should be repeated as in step1 as there are two sets of three rows. Similarly, two set of rows will be obtained as a result of the addition of each three row set. In this process, the summation bits are moved to the carry-out row which is indicated by gray boxes.





Stage2: Partial Product addition , step3

The same process is repeated. One set of three rows along with one additional row is present which is carried down. The result of these three rows is two rows and an additional row is carried down. The process is very slow as each step takes a similar time as a full adder. All adders are in parallel.

```
. . 1 1 0 0 1 1 1 1 0 1 0

      0 0 1 0 1 0 0 0 1 0

    1 0 1 1 1 0 1 0 1 0
-------------------------
1 0 0 0 0 0 1 0
```

```
0 1 1 1 1 0 0 0 1 0 1 0 1 0

1 0 0 1 0 1 0 1 0 1 0

1 0 0 0 0 0 1 0
```

Stage2: Partial Product addition , step4

The process is repeated for the last time as only three rows are remaining. The result is obtained in two rows. In this example, Stage2 is completed in 4 steps, so 4 full adder delays are present.

```
    0 1 1 1 1 0 0 0 1 0 1 0 1 0

    1 0 0 1 0 1 0 1 0 1 0

1 0 0 0 0 0 1 0
```

```
  0 0 1 0 1 0 1 1 0 0 0 1 0 1 0

1 0 0 1 0 1 0 0 0 1 0
```

Stage3: Final addition

At this stage the last two rows are remaining, the addition result is obtained by calculating these two rows. In this example, no need to add the 5LSBs.

```
  0 0 1 0 1 0 1 1 0 0 0 1 0 1 0

1 0 0 1 0 1 0 0 0 1 0
```

The above is the result that is obtained by Wallace Tree Multiplication

Wallace tree multiplication takes an equal amount of time as a 2N bit ripple carry adder..

D. Urdhva Tiryagbhayam Method

Urdhva Tiryagbhayam is the Sutra 3 of the Vedic Mathematics. The meaning of Urdhva Tiryagbhayam is " Vertically and Crosswise.

Case (i): Multiplication of two-digit numbers.
Multiplication of 24 and 16 i.e 24 *16

```
Step1:  2   4
       *1   6
            4
```

In Step1, 4 is multiplied by 6 i.e 4*6 =24. So 4 is placed in the units place and carry =2.

```
Step 2:  2   4
        *1   6
         8   4
```

In Step2, 2 is multiplied by 6 i.e 2 * 6 = 12 and also 4 is multiplied by 1 i.e 4*1=4 and finally addition operation is performed by considering the above carry i.e 12 + 4 + 2 = 18. So, 8 is placed in tens place and carry = 1.

```
Step 3:  2   4
       * 1   6
       3 8   4
```

In Step3, 2 is multiplied by 1 i.e 2 * 1 = 2 and carry is added i.e 2 + 1 = 3. Now 3 is placed in hundreds place. The final result obtained by multiplying 24 * 16 is 384.

Case (ii): Multiplication of three-digit numbers.
Multiplication of 142 and 526 i.e 142 *526

```
Step 1:  1  4  2
        *5  2  6
               2
```

In Step 1, 2 is multiplied by 6 i.e 2 * 6 = 12. So 2 is placed in units place and carry = 1

```
Step 2:  1  4  2
        *5  2  6
            9  2
```

In Step2, 4 is multiplied by 6 i.e 4 * 6 = 12 and also 2 is multiplied by 2 i.e 2*2=4 and finally addition operation is performed by considering the above carry i.e 24 + 4 + 1 = 29. So, 9 is placed in tens place and carry = 2.

Step 3: 1 4 2
*5 2 6
6 9 2

In Step 3, 1 is multiplied by 6 i.e 1 * 6 = 6 and 4 is multiplied by 2 i.e 4*2= 8 also 2 is multiplied by 5 i.e 2*5 = 10 and finally addition operation is performed by considering the above carry i.e 6+8+10+2 = 26. So, 6 is placed in hundreds place and carry = 2.

Step 4: 1 4 2
*5 2 6
4 6 9 2

In Step 2, 1 is multiplied by 2 i.e 1 * 2 = 2 and also 4 is multiplied by 5 i.e 4*5=20 and finally addition operation is performed by considering the above carry i.e 2 + 20 + 2 = 24. So, 4 is placed in thousands place and carry = 2.

Step 5: 1 4 2
*5 2 6
7 4 6 9 2

In Step 5, 2 is multiplied by 1 i.e 1 * 5 = 5 and carry is added i.e 5 + 2 = 7. Now 7 is placed in last position. The final result obtained by multiplying 142 * 52 6 is 74692.

A Vedic Karatsuba algorithm is proposed which is further modified by the adaptive method by using Non - Linear Carry Select Adder.

II. Karatsuba Multiplication

Assume X and Y are the two inputs of 'n' bits each. The X and Y are divided into two segments say XH, YH and XL, YL. Here XH, YH are the higher-order bits and XL, YL are the lower order bits.

X Y = (2^n/2 * XH +XL) (2^n/2 * YH +YL)

= 2^n (XH YH) + 2^n/2 (XH YL + XL YH) + (XL YL)

By Karatsuba multiplier algorithm, XH YL + XL YH = (XH + XL) (YH+YL) - XH YH - XL YL

Therefore, 4 * n/2 bit multiplications is decreased to 3* n/2 bit multiplications. Time complexity of Karatsuba multiplication algorithm is O(n) = n^1.58.

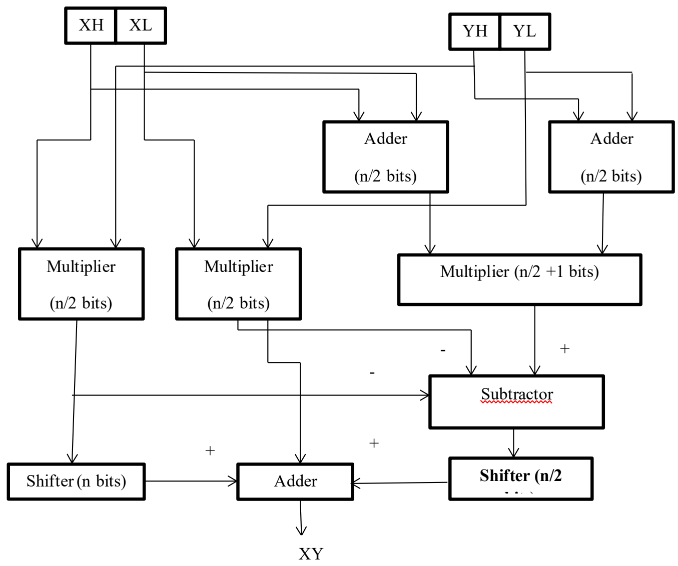


Figure1: 'n' bit Karatsuba Multiplier

A. Recursive Karatsuba Multiplier

If Karatsuba multiplier is used repeatedly at every stage when the size of the bit is high then it is known as Recursive Karatsuba Multiplier. This is Recursive Karatsuba algorithm that is used to improve the speed. The separated bits (N) are grouped into an equal number of bits (N/2) and the Karatsuba multiplication is done recursively with the separated bits.

For example, a 32 bit multiplication is divided into 16 bit multiplication which is again divided into 8 bit multiplication and it is again divided into 4 bit multiplication and at last it is divided into 2 bit multiplication which is the final step for the regular multiplication process. An adaptive Karatsuba approach is implemented at every stage for the third product term.

B. Adaptive Karatsuba Multiplication

Karatsuba algorithm is used for the calculation of the third product effectively. Let X and Y be the inputs of 'n' bits each, we have the argument of the third product of (n/2 + 1) bits. Assume P and Q are the arguments that are added by (n/2 - 1) bits at the left. The P and Q are divided into two equal parts like PH, QH and PL, QL where PH, QH are the higher-order bits and PL, QL are the lower order bits. Here, PH and QH are the carry-outs of the third product terms i.e (XH + YH) and (XL + YL) so they will be either 0 or 1.

Third product = P Q

= (2^n/2 * PH +PL) (2^n/2 * QH +QL)

= 2^n (PH QH) + 2^n/2 (PH QL + PL QH) + (PL QL)

Based on PH and QH values the above expression is evaluated as shown in the Table2.

From Table 2, it is observed that to calculate (n/2 + 1) bits of third product it requires one n/2 bits multiplication and also extra shifting, adding and multiplexing operations are needed, instead of (n/2 + 1) bit multiplier. So the Karatsuba algorithm becomes recursive.

Figure2 represents the schematic diagram of third product computation by using adaptive method.

C. Non Linear Carry Select Adder

In Non Linear Carry Select Adder, each block can be of different size. For example, a 16 bit adder can be implemented by using different bit sizes instead of using four similar block sizes. So, a 16 bit adder can be made by 2-2-3-4-5 bit blocks.

Figure 3 represents the schematic diagram of 16 bit Non Linear Carry Select Adder. Here, 'A' and 'B' are the inputs, carry-in is represented by 'Cin'. The two outputs of the non-linear carry select adder are Sum and Carry-out represented as 'S' and 'Cout' respectively.

Table2: Computation of Third Product

PH	QH	Third Product
0	0	PL QL
0	1	2^n/2 *PL + PL QL
1	0	2^n/2 *QL + PL QL
1	1	2^n + 2^n/2 (QL + PL) + PL QL

Results

A. RTL Schematic

RTL is abbreviated as Register Transfer Level. It represents the blueprint of the architecture and also used to verify the designed architecture. RTL Schematic view of Vedic Karatsuba algorithm is shown in the below Figure4. In this schematic view, the inputs are represented as X and Y of 16 bits each, and the output is represented as Product of 32 bits.

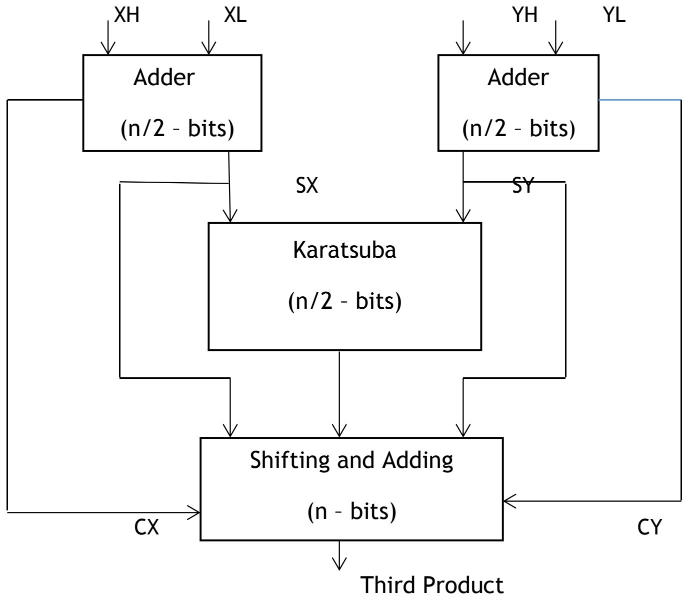


Fig. 2: Third Product Computation By Adaptive Method

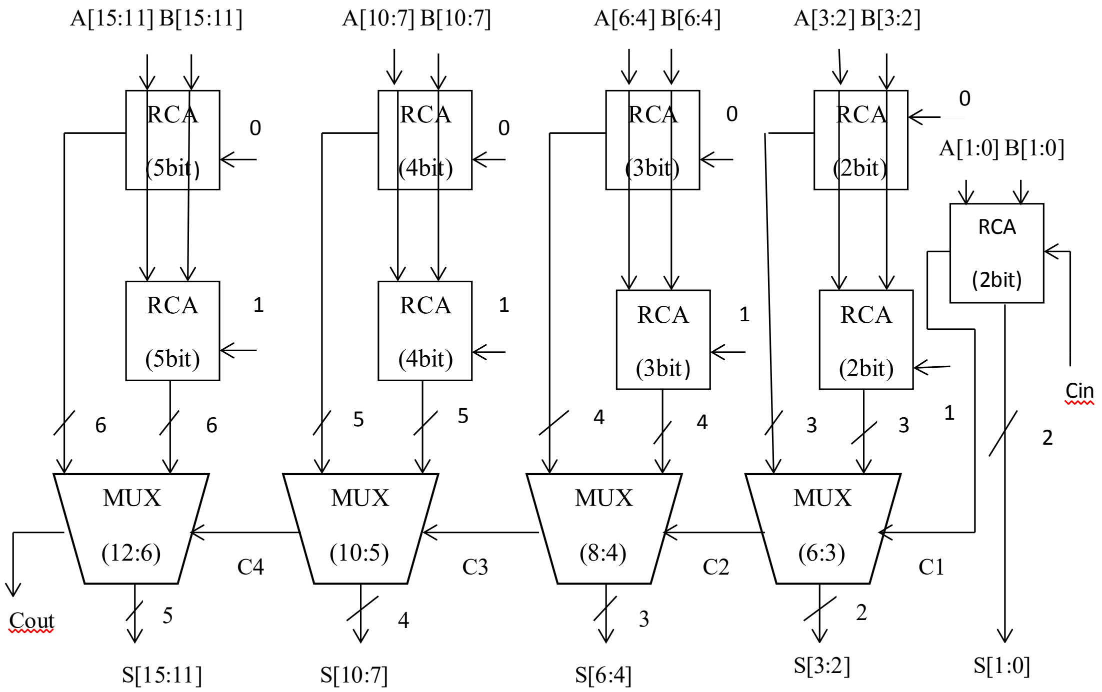


Fig. 3: Non - Linear Carry Select Adder of 16 bits

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B. Simulation

Simulation is the last step to verify the working of the algorithm whereas RTL schematic is used to verify the connections and the blocks. The output is observed in the waveforms format in the simulation window. There is a flexibility of providing different radix number systems. The below Figure5 represents the output waveforms of the Adaptive and Recursive Vedic Karatsuba algorithm using Non – Linear Carry Select Adder.

To verify the output, the inputs considered are X = 50, Y = 50 and the output obtained is Product = 2500.

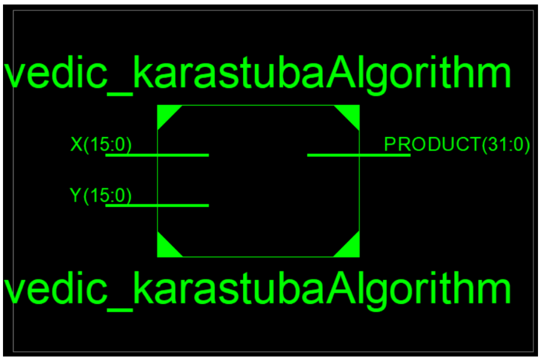

Fig. 4: Schematic View of Vedic Karatsuba Multiplier

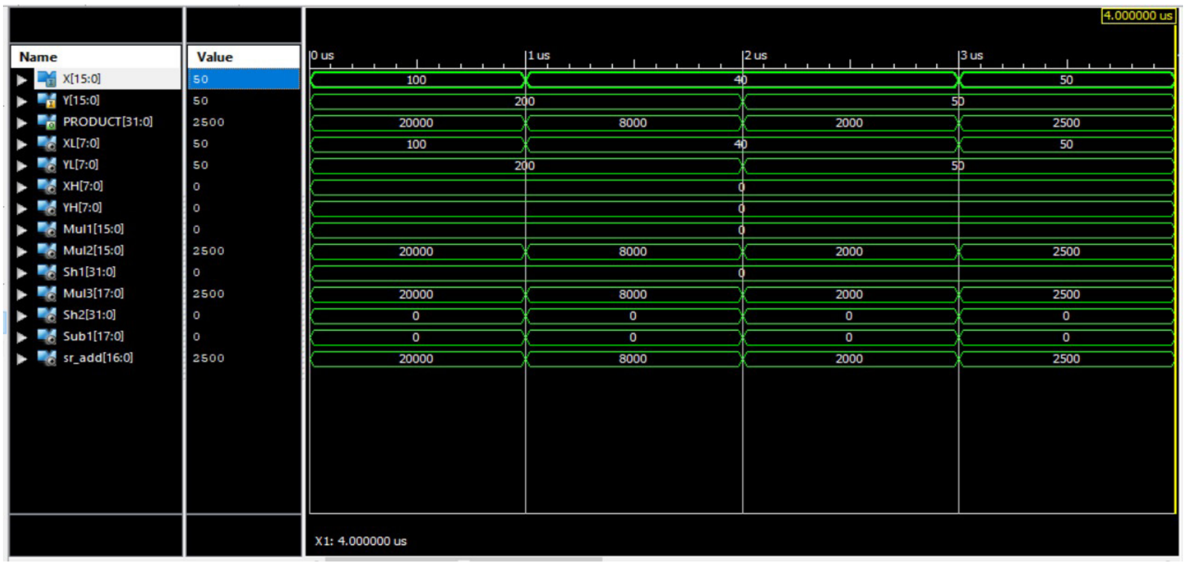

Fig. 5: Waveforms Of Adaptive And Recursive Vedic Karatsuba Multiplier

Conclusion

Vedic algorithms are used to design the functional logic so that greater speed can be achieved. The adaptive approach of karatsuba algorithm is implemented to minimize the complexity from square to logarithmic power of the bit size.

The main aim to implement the 16 * 16 bit multiplier algorithm is to minimize the delay. Less number of partial products are produced by the Vedic Karatsuba algorithm. The third product term is calculated by the adaptive method of Karatsuba algorithm for greater speed. Non – Linear Carry Select Adder is used for the improvement of the speed of the partial product terms. Therefore by using Adaptive and Recursive Karatsuba algorithm with Non – Linear Carry Select Adder, the time delay obtained is in nanoseconds which is better than other algorithms.

References

[1] Y. S. Rao, M. Kamaraju and D. V. S. Ramanjaneyulu, "An FPGA implementation of high speed and area efficient double-precision floating point multiplier using Urdhva Tiryagbhyam technique," 2015 Conference on Power, Control, Communication and Computational Technologies for Sustainable Growth (PCCCTSG), 2015, pp. 271-276, doi: 10.1109/PCCCTSG.2015.7503923.

[2] K. B. Jaiswal, Nithish Kumar V, P. Seshadri and Lakshminarayanan G, "Low power wallace tree multiplier using modified full adder," 2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN), 2015, pp. 1-4, doi: 10.1109/ICSCN.2015.7219880.

[3] Rajeev Ratna Vallabhuni, Jujavarapu Sravana, Chandra Shaker Pittala, Mikkili Divya, B.M.S.Rani, and Vallabhuni Vijcaay, "Universal Shift Register Designed at Low Supply Voltages in 20nm FinFET Using Multiplexer," In Intelligent Sustainable Systems, pp. 203-212. Springer, Singapore, 2022.

[4] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[5] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, "System and Method to Improve Performance of Amplifiers Using Bias Current," The Patent Office

Journal No. 43/2019, India. International classification: C12Q1/6869. Application No. 201941042648 A.

[6] S.V.S Prasad, Chandra Shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "Complex Filter Design for Bluetooth Receiver Application," In 2021 6th International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, July 8-10, 2021, pp. 442-446.

[7] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[8] K.H. Bindu, et al., "FINFET Technology in Biomedical-Cochlear Implant Application," *International Web Conference on Innovations in Communication and Computing, ICICC '20*, India, October 5, 2020.

[9] Chandra Shaker Pittala, et al., "Novel Architecture for Logic Test Using Single Cycle Access Structure," *Journal of VLSI Circuits And Systems*, vol. 3, iss. 1, 2021, pp. 1–6.

[10] S. P. Pohokar, R. S. Sisal, K. M. Gaikwad, M. M. Patil and R. Borse, "Design and implementation of 16 × 16 multiplier using Vedic mathematics," 2015 International Conference on Industrial Instrumentation and Control (ICIC), 2015, pp. 1174-1177, doi: 10.1109/IIC.2015.7150925.

[11] S. Arish and R. K. Sharma, "An efficient binary multiplier design for high speed applications using Karatsuba algorithm and Urdhva-Tiryagbhyam algorithm," 2015 Global Conference on Communication Technologies (GCCT), 2015, pp. 192-196, doi: 10.1109/GCCT.2015.7342650.

[12] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, P ASHOK BABU, "System to Obtain Finite Gain and Noise of an Electrocardiogram Amplifier," The Patent Office Journal No. 43/2019, India. International classification: H03F3/38. Application No. 201941042674 A.

[13] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Veerastu Sivanagaraju, Chandrashaker Pittala, "System for Minimizing Crosstalk Effects of Shells and Designing Multiwalled Carbon Nanotube Models," The Patent Office Journal No. 43/2019, India. International classification: B82Y10/00. Application No. 201941042460 A.

[14] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandrashaker Pittala, and Sonagiri China Venkateswarlu, "System for Reducing Crosstalk Delays In Electronic Devices Using A CMOS Inverter," The Patent Office Journal No. 43/2019, India. International classification: H03B5/18. Application No. 201941042515 A.

[15] Rajeev Ratna Vallabhuni, M. Saritha, Sruthi Chikkapally, Vallabhuni Vijay, Chandra Shaker Pittala, and Sadulla Shaik, "Universal Shift Register Designed at Low Supply Voltages in 15nm CNTFET Using Multiplexer," Lecture Notes in Networks and Systems, 2021.

[16] Chandra Shaker Pittala, J. Sravana, G. Ajitha, P. Saritha, Mohammad Khadir, V. Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Novel Methodology to Validate DUTs Using Single Access Structure," 5th International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech 2021), Kolkata, India, September 24-25, 2021, pp. 1-5.

[17] B. M. S. Rani, et al., "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," *Journal of Ambient Intelligence and Humanized Computing*, 2021.

[18] Ch. Srivalli, et al., "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," *National Conference on Emerging Trends in Engineering Application (NCETEA-2011)*, India, June 18, 2011, pp. 224–227.

[19] Rajeev Ratna Vallabhuni, S. Lakshmanachari, G. Avanthi, and Vallabhuni Vijay, "Smart Cart Shopping System with an RFID Interface for Human Assistance," 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS), Thoothukudi, India, 2020, pp. 165-169, doi: 10.1109/ICISS49785.2020.9316102.

[20] Chandra Shaker Pittala, et al., "Energy Efficient Decoder Circuit Using Source Biasing Technique in CNTFET Technology," *2021 Devices for Integrated Circuit (DevIC)*, Kalyani, India, May 19-20, 2021, pp. 610–615

[21] Chandra Shaker Pittala, et al., "Biasing Techniques: Validation of 3 to 8 Decoder Modules Using 18nm FinFET Nodes," *2021 2nd International Conference for Emerging Technology (INCET)*, Belagavi, India, May 21–23, 2021, pp. 1–4.

[22] Vallabhuni Rajeev Ratna, M. Saritha, Saipreethi. N, V. Vijay, P. Chandra Shaker, M. Divya, and Shaik Sadulla, "High Speed Energy Efficient Multiplier Using 20nm FinFET Technology," Proceedings of the International Conference on IoT Based Control Networks and Intelligent Systems (ICICNIS 2020), Palai, India, December 10-11, 2020, pp. 434-443. Available at SSRN: https://ssrn.com/abstract=3769235 or http://dx.doi.org/10.2139/ssrn.3769235

[23] Manchala Sreeja, and Vallabhuni Vijay, "A Unique Approach To Provide Security For Women By Using Smart Device," European Journal of Molecular & Clinical Medicine, vol. 7, iss. 1, 2020, pp. 3669-3683.

[24] S. Kakde, S. Khan, P. Dakhole and S. Badwaik, "Design of area and power aware reduced Complexity Wallace Tree multiplier," 2015 International Conference on Pervasive Computing (ICPC), 2015, pp. 1-6, doi: 10.1109/PERVASIVE.2015.7087207.

[25] V. Vijay, et al., "Energy efficient CMOS Full-Adder Designed with TSMC 0.18μm Technology," *International Conference on Technology and Management (ICTM-2011)*, Hyderabad, India, June 8-10, 2011, pp. 356–361.

[26] Ch. Srivalli, et al., "Optimal design of VLSI implemented Viterbi decoding," *National conference on Recent Advances in Communications & Energy Systems, (RACES-2011)*, Vadlamudi, India, December 5, 2011, pp. 67–71.

[27] Chandra Shaker Pittala, and Vallabhuni Vijay, "Design Of 1-Bit FinFET Sum Circuit For Computational Applications," *In International Conference on Emerging Applications of Information Technology*, pp. 590–596. Springer, Singapore, 2021.

[28] Vallabhuni Vijay, et al., "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," *International Journal of System Assurance Engineering and Management*, vol. 12, iss. 6, 2021, pp. 1173-1179.

[29] Swathi, S., et al., "A hierarchical image matting model for blood vessel segmentation in retinal images,"

International Journal of System Assurance Engineering and Management, 2021, pp. 1–9.

[30] V. Siva Nagaraju, P. Ashok Babu, Vallabhuni Rajeev Ratna, Ramya Mariserla, "Design and Implementation of Low Power 32-bit Comparator," Proceedings of the International Conference on IoT Based Control Networks and Intelligent Systems (ICICNIS 2020), Palai, India, December 10-11, 2020, pp. 459-468. Available at SSRN: https://ssrn.com/abstract=3769748 or http://dx.doi.org/10.2139/ssrn.3769748