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Research Article

High Speed and Efficient Wallace Tree Multiplier for Dsp Applications

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ABSTRACT
Multiplier is one of the key and fundamental block in the many applications such as DSP, signal processing etc. In numerous occasions multipliers plays a prominent role to decide the system performance. Out of the several multipliers wallace tree multiplier is one of reliable and occupies the minimal space in digital applications. This work describes the designing of the high performance 8 bit wallace tree multiplier using compressor technique. The multiplier were simulated and estimated its performance using the Vivado.

Keywords: High Speed, Multiplier, Applications

Introduction

Multipliers is one of the key hardware functional unit in the communications and DSP systems to perform the high speed operations. multiplication is one of the basic functions which could be performed for the several algorithms. These multipliers can be used in the many current scenarios such as portable battery operated systems, filtering ,multimedia etc. These multipliers are usually very complex and occupies huge space, and also which are operated at very high clock rate, hence it dissipates huge amount of power dissipation respectively. Already a set of multipliers are available such as array multiplier, serial multiplier, booth multiplier, bought wooley multiplier, binary multiplier etc[1-4]. Each multiplier has its own importance. Binary multiplier multiplies the two unsigned binary numbers and produces the result. The major disadvantage of this multiplier is it occupies the more area and speed of the operation is very slow. Array multiplier is another type of multiplier which consumes the more power and delay is also another major issue. During the multiplication it performs the two basic operations. one such as produces the partial products and other one is produces the partial production addition.

to introduces the multiplication operation, let us consider the two unsigned binary numbers such as X and Y. each having the M and N bit size respectively. For easy of understanding let us express in the binary representation

$$X = \Sigma\, Xi\ 2^{i} \quad i = 0 \text{ to } M$$

$$Y = \Sigma\, Yj\ 2^{j} \quad j = 0 \text{ to } N$$

The explicitly representation of the multiplication can be defined as follows.

$$\begin{aligned} Z = X \times Y &= \Sigma\, Z_k\, 2^{k} \quad k = 0 \text{ to } M + N - 1 \\ &= (\Sigma\, Xi\ 2^{i}\ i = 0 \text{ to } M)\,(\Sigma\, Yj\, 2^{j}\ j = 0 \text{ to } N) \\ &= \Sigma\,(\Sigma\, X^{i}\, Y^{j}\, 2^{i+j})\ i = 0 \text{ to } M\text{-}1,\ j = 0 \text{ to } N\text{-}1 \end{aligned}$$

In order to perform the faster operation we need to implement the multiplication in the by using the manually. For that the entire partial products can be produces the single time and it could be organised in array manner. the below figure can be illustrates the example of the manual multiplication[5].

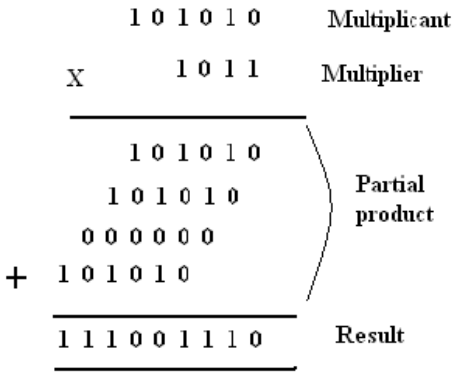

Fig.1: Example of manual multiplication.

The rest of the paper is organised as follws,section1 describes the basic introduction about the importance and applications of the multiplication, Section 2 enlists the various multipliers and corresponding advantages and disadvantages of the each multiplier. Section 3 describes the our proposed wallace tree multiplier architecture and comparison with the existed architectures. and finally last section describes the conclusion respectively.

Literature Survey

Array Multiplier

The basic architecture of the multiplier as shown in figure2. for the producing the multiplication it requires the N by M two bit AND gates. Most of the area is devoted for the adding the partial products. and it requires the N-1, M bit adders. the shifting of the data can be done through simple routing mechanism. the overall structure can be easily computed by using in a rectangle manner. it results very efficient layout respectively[6-8].

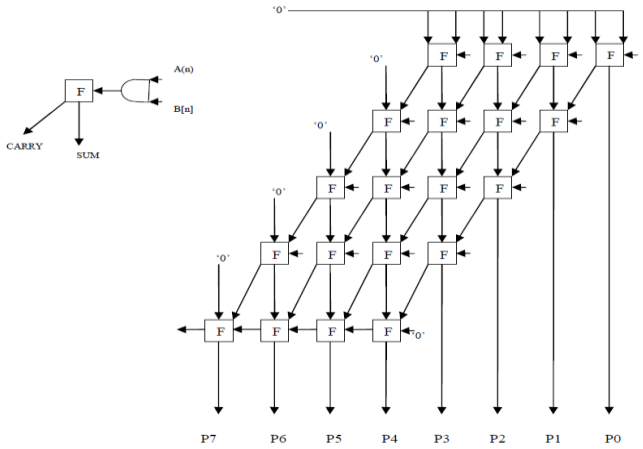

Fig.2: array multiplier

Baugh Wooley Multiplier

This algorithm mainly deals with the multiplication of the two unsigned binary multiplication. This algorithm explicitly evaluates the all possible AND gates and implemented through the a chain of half adders and full adders with carry out at each significant addition respectively. Figure 3 depicts the basic architecture of baugh wooley multiplier. by using this multiplier we can able to perform the negative operands respectively[9].

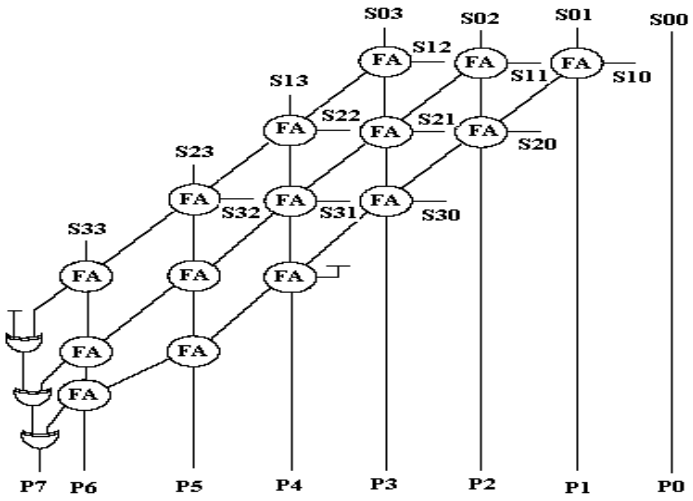

Fig.3: Baugh Wooly Multiplier Architecture

Braun Multiplier

It is one of the simple parallel type multiplier. the computation can be done in parallel manner. The computation time is limited by carry propagation adder and carry save adder. this multiplier can be highly suitable for the positive operands. the basic architecture of the braun multiplier can be shown in figure 4 respectively[10].

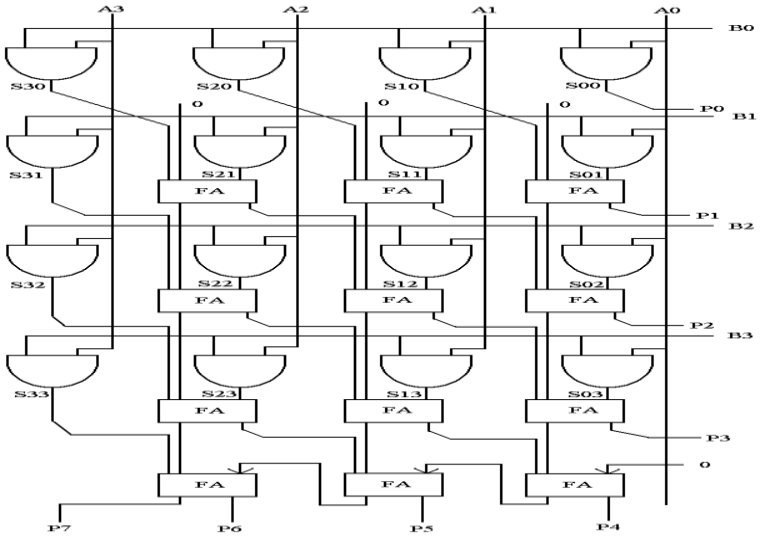

Fig.4: Braun multiplier architecture

The partial products were generated bit-by-bit, by adding operation of multiplier and multiplicand, the partial products have been reduced by using 4:2 compressor full and half adder[11]. Lastly addition of partial products have been done by kogge-stone adder.

proposed work

The partial products were generated by addition of multiplier and multiplicand, its partial products can be given by reducing the 4:2 compressor full and half adder. lastly the addition of partial products have been provided by kogg-stone adder. Its architecture can be given by figure 5 respectively.

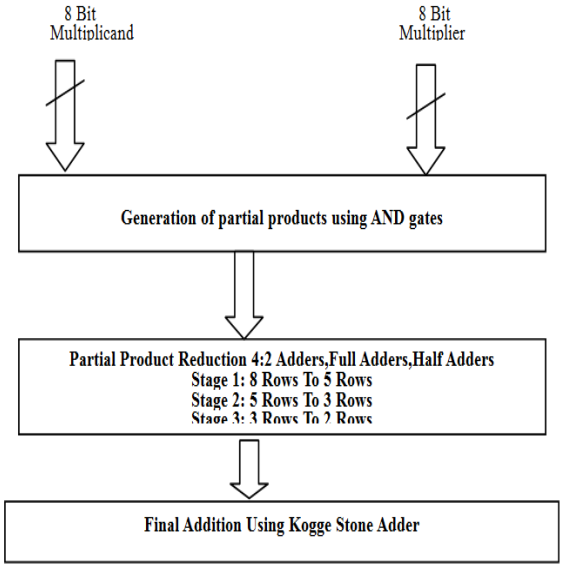

Fig.5: Architecture of Conventional Multiplier

3.1 7:2 Compressor Architecture

7:2 compressor architecture have the seven input bits and two output and carry, and also have carry-in bits and carry-out bits (cin1,cin2,cout1,cout2). Carry-in bits , out1, out2 having the rank of 0 and 1 ; carry -out bits having the rank of 1 and 2 respectively[12]. The 7:2 compressor schematic symbol and architecture are shown in Fig 6,7 respectively. Correspondingly its simulation results of 8 bit simulation results and its RTL diagram as shown in figure 8 & 9 respectively.

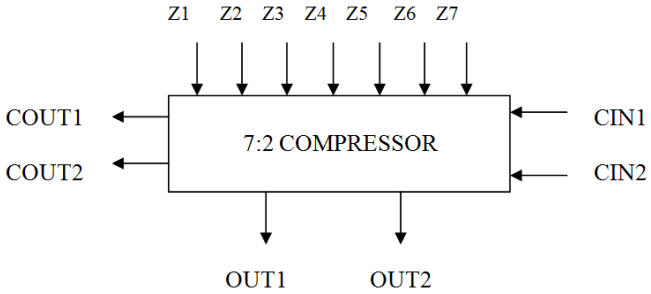

Fig.6: 7:2 Compressor schematic symbol

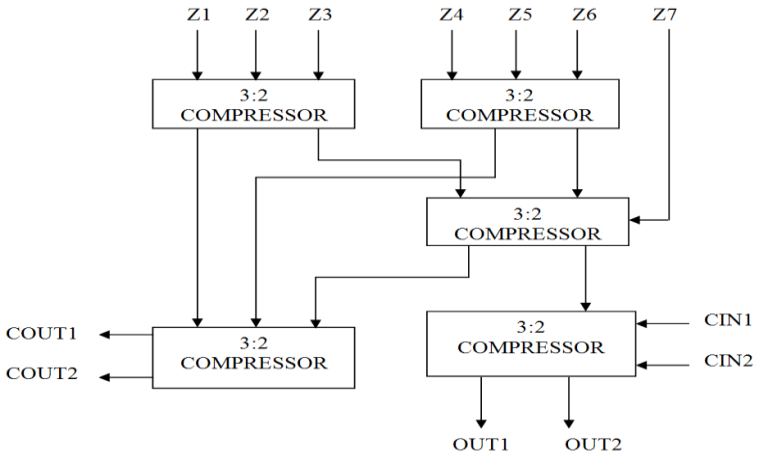

Fig.7: 7:2 Compressor Architecture

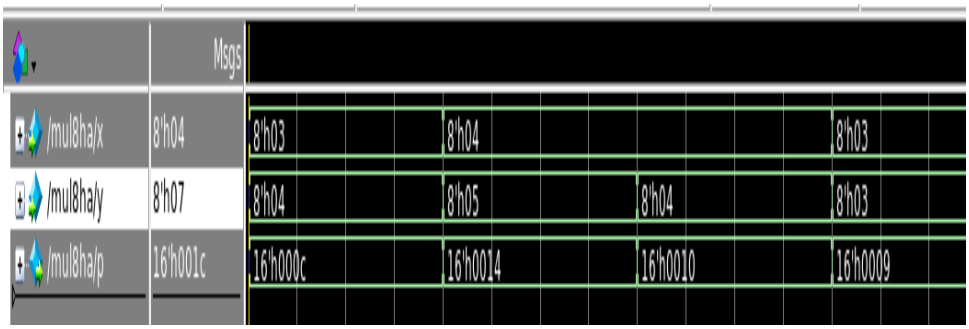

Fig.8: Simulation Result for 8-bit Multiplier.

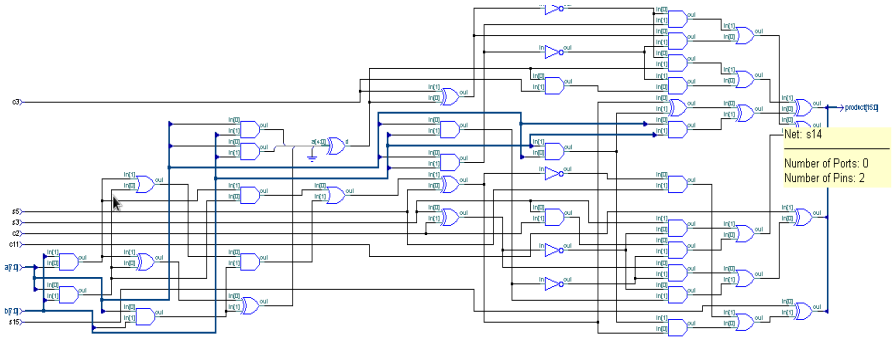

Fig.9: RTL Diagram for 8-bit Multiplier.

conclusion

The proposed 8 bit wallace tree multiplier can be solved by several problems such as delay and power dissipation. it can be increases the speed of the operation and occupies the very less space respectively. Hence for DSP and communication applications it is the best choice.

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