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Research Article

Energy Efficient and Low Power Rca Based Full Adder

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ABSTRACT
Full adders are becoming the one of the most important and fundamental digital blocks in the present-day scenario. As the day by day circuit complexity increases its very much necessary to reduce the power consumption. In this paper we proposed a novel and reliable transmission gate based full adder. which occupies less are and reduces the power significantly. Hence these types of the adders can be extensively suitable for the design of ALU in the computers to perform the high-speed operations.

keywords: Transmission gate based full adder, low-power consumption, algorithmic logic unit(ALU).

Introduction

As the day by day technology has scaling down drastically, it eventually reduces the chip area and also it decreases leakage current, decreases the gate control ,power consumption. In order to overcome these draw backs several mechanisms/ technologies has been developed such as carbon nano tube based field effect transistor(CNTFET), quantum cellular automata (QCA) etc. During current scenario full adder is one of the basic fundamental digital block in the many ALUs. it is one of the emerging and trending research area, which provides the several solutions in many applications. At present several full adders has been proposed such as pass transistor based full adder, XOR based full adder, GDI(gate diffusion input) based full adder, QCA based full adder etc. For any full adder its performance can be attributed based on three metrics such as power consumption, speed and area. figure 1 indicates the NAND based full adder. These adders can be widely used in the power density processors, server temperature inclinations, super scalar processors, and also current day (system on Chip)SoCs etc.

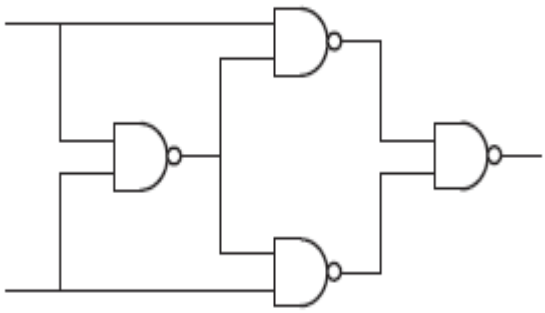

Fig.1: NAND based full adder

The rest of the paper is organised as follows such as section 1 introduces the basics overview about the full adders, section 2 demonstrates the existing full adders and its performance analysis and section 3 explains the RCA based full adder and its simulation results and finally section 4 concludes the its conclusion respectively.

Literature Survey

Even though vast majority of single bit full adders has been published in the literature survey[1-6], the basic motto is to reduce the power, area, and circuit complexity. Many authors has been published a wide variety of architectures such as shown in below figures. Figure 2 indicates the hybrid design based full adder, which consist of three modules and it produces the final output as sum and carry respectively, the internal modules such as module 1,2 and 3 can be shown in figure 5,6and7. Further to enhance it speed and to reduce the area proposed a XOR and XNOR (mux)based architecture. figure 3 depicts the Aguirre's based full adder. and authors such as Kumar's proposed a nand and mux based full adder.

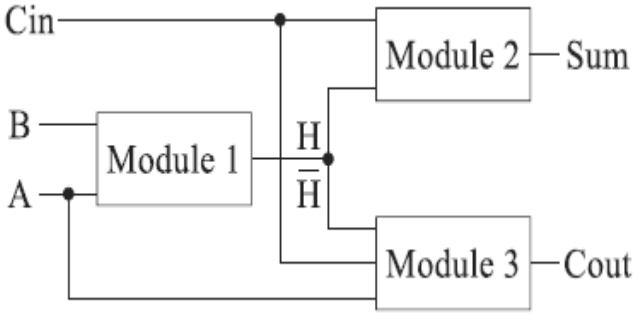

Fig.2: Hybrid design based full adder

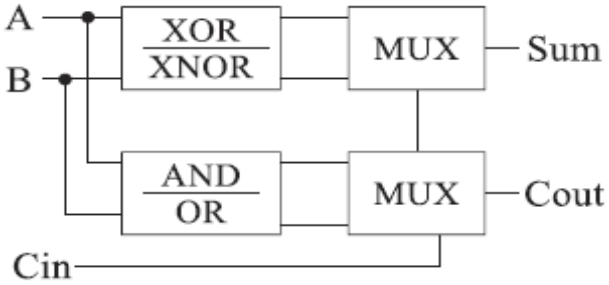

Fig.3: Aguirre's logic scheme based full adder

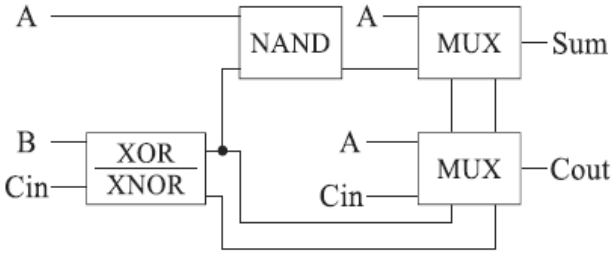

Fig.4: Kumar's logic scheme based full adder.

The final logic equations for the each architecture can be shown in below table 1.

Table:1

Structure	Logic function	
	Sum	Cout
Fig. 1(a)	$H\overline{C_{in}} + \overline{H}C_{in} = (A \oplus B) \oplus C_{in}$	$HC_{in} + \overline{H}A$
Fig. 1(b)	$H\overline{C_{in}} + \overline{H}C_{in} = (A \oplus B) \oplus C_{in}$	$\overline{C_{in}}(AB) + C_{in}(A + B)$
Fig. 1(c)	$(B \oplus C_{in})\overline{(A(B \oplus C_{in}))} + A\overline{(B \oplus C_{in})}$	$A(B \oplus C_{in}) + C_{in}\overline{(B \oplus C_{in})}$

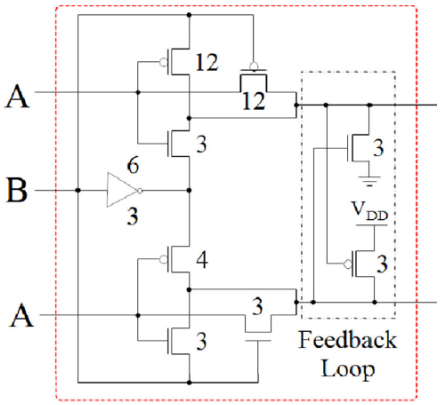

Fig.5: module 1

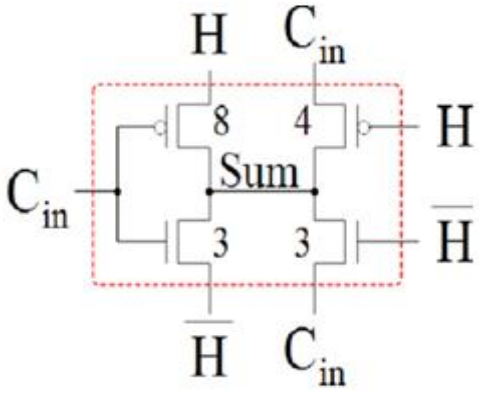

Fig.6: module 2

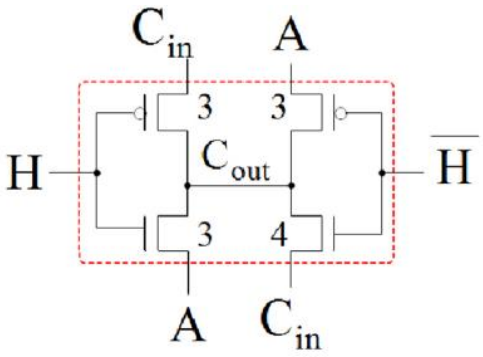

Fig.7: module 3

The basic static CMOS adder is made up of a complementary pull-up and pull down PMOS and NMOS network. the conventional design consists of 28 number of transistor, which occupies more area and also dissipates the huge amount of power. Hence to reduce the overall capacitance and to enhance the speed of operation introduces the a set of full adders such PTL based full adders.

proposed work

In the literature survey Many transmission gate based full adders have been already discussed, those TR gate based Full adders uses the chain architectures. lack of driving strength loading effect are considered to be major problem in the TR gate based architecture. Here in the TR gate based Full adder has the inputs FA0 which can directly propagates the sum and carry outputs respectively. And also this architecture can effectively eliminates the capacitive problem there by C0 and sum. The basic formula for estimating the delay can be given by the below equation.

$$t_p = 0.69 \times CR \times \frac{n(n+1)}{2}$$

C = total lumped capacitance of FA
R = total lumped resistance of FA
n = number of stages
If we consider the FAs of 4-bit RCA and multiplier

Below figure depicts the proposed architecture of the transmission gate based full adder and figure 9 depicts the corresponding layout for the proposed transmission gate respectively. And also the proposed full adder has compared with the existing adders such as 20transistors full adder, kamsani proposed full adder, low power high threshold 18 T full adder, low power high threshold 22 T full adder. And the below table1 compares the maximum delay, average power dissipation in all cases respectively.

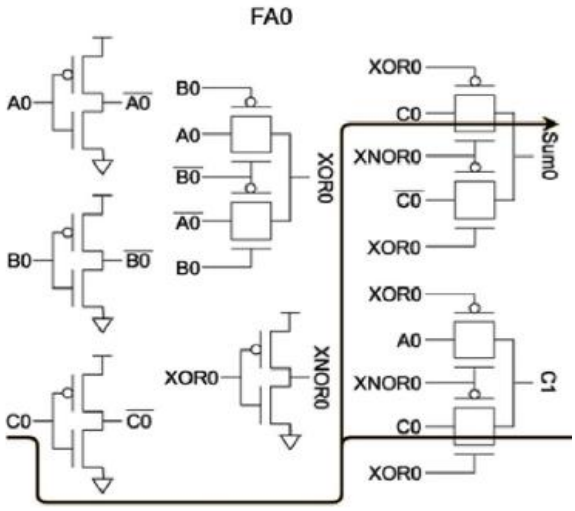

Fig.8: Transmission gate based full adder

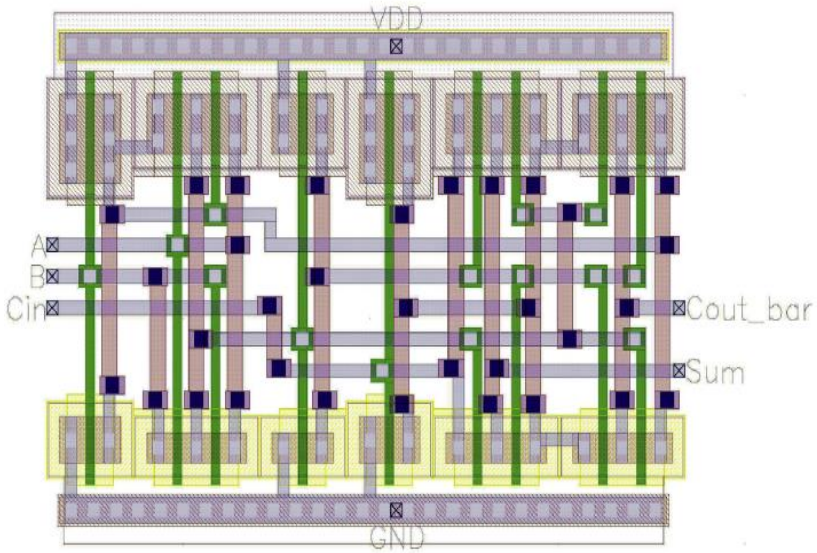

Fig.9: Layout for the transmission gate based full adder.

Table:2

Full Adder	Regular /Triplet	Max. Propagation Delay (ps)	Average Power Dissipation (uW)	PDP (fWs)
20T conventional	Regular	717	8.77	6.29
	Triplet	676	9.17	6.2
Kamsani	Regular	707	9.84	6.95
	Triplet	662	10.1	6.69
LPHS18T	Regular	752	7.97	5.99
	Triplet	686	8.34	5.72
LPHS22T	Regular	736	10.1	7.32
	Triplet	664	10.4	6.81
TFA	Regular	785	7.38	5.79
TG CMOS	Regular	745	8.77	6.53
	Triplet	688	9.06	6.24

Conclusion

Full adder is one the basic and most important fundamental digital block in the any type of the arithmetic and logical circuit. many types of the full adders have been proposed and it has been used in the several applications. but the existed adders imposes the several difficulties such as delay, are and power consumption. hence to combat the above mentioned issues proposed a high speed and low power TG based full adder.

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