Journal of VLSI Circuits and Systems, ISSN: 2582-1458 Vol. 6, No. 2, 2024 (pp. 14 -22)

WWW.VLSIJOURNAL.COM

Development of Low Power GNSS correlator in Zynq SoC for GPS and GLONSS

[1]*Arunalatha Botla, [2]G Kanaka Durga, [3]Chandrasekhar Paidimarry

[1,3]*Electronics and communication engineering, Osmania University, Telangana, India*

[2]*Electronics and communication engineering, MVSREngg college, Telangana, Telangana, India.*

KEYWORDS:
GPS,
GLONASS,
Low Power,
GNSS correlator,
Zynq SoC.

ARTICLE HISTORY:
Received 05.04.2024
Accepted 10.05.2024
Published 08.06.2024

DOI:
https://doi.org/10.31838/jvcs/06.02.02

Abstract

A low-power Global Navigation Satellite System (GNSS) correlator for GPS and GLONASS signals was developed using the Zynq System on Chip (SoC) technology. The main goal of this research was to create an efficient correlator that consumes minimal power while maintaining excellent signal processing capabilities. The proposed correlator architecture leverages the programmable logic and processing capabilities of the Zynq SoC, employing a combination of hardware and software implementations to achieve maximum power efficiency. The design of the GNSS correlator is implemented using Verilog, and the Verilog code is realized on the Zynq SoC device. To assess the resource utilization and power consumption of the proposed design, the Xilinx Vivado IDE is utilized for resource estimation and power analysis. Simulation results demonstrate the high precision of the low-power GNSS correlator in processing GPS and GLONASS signals. The findings of the study indicate significant power savings compared to conventional correlator designs. The proposed design enhances power utilization without compromising signal processing capabilities by utilizing optimizing the correlator architecture. The development of a low-power GNSS correlator facilitates the advancement of energy-efficient GNSS receiver designs, particularly for applications with limited power resources. The proposed architecture not only extends battery life but also simplifies the integration of GNSS positioning capabilities into devices with restricted power availability.

Author e-mail: gangarapu latha@gmail.com

How to cite this article: Botla A, Durga GK, Paidimarry C. Development of Low Power GNSS correlator in Zynq SoC for GPS and GLONSS, Journal of VLSI Circuits and system Vol. 6, No. 2, 2024 (pp. 14-22).

Introduction

The Global Navigation Satellite Systems (GNSS), commonly referred to as GNSS, play a vital role in providing accurate positioning, navigation, and time information to users worldwide in the field of satellite navigation systems. However, the widespread use of GNSS devices in various applications such as smartphones, wearables, and Internet of Things (IoT) devices has created a demand for more efficient and power-conscious solutions. As a result, a groundbreaking technology known as the low-power GNSS correlator has been developed.[1]

The development of the low-power GNSS correlator represents a significant advancement in satellite navigation.[24] Traditional GNSS receivers heavily rely on complex correlators that consume substantial processing resources and require significant amounts of electricity. This poses a problem in terms of battery life and overall device performance, particularly in situations where power efficiency is critical. Recognizing this need, academics and engineers have focused their efforts on designing and implementing a low-power GNSS.[2]

The primary objective of a low-power GNSS correlator is to reduce the energy consumption of the navigation system while maintaining precision and reliability. This is achieved by combining various innovative algorithms, circuit designs, and optimization strategies.[5,19] The low-power correlator efficiently extracts the relevant navigation information while minimizing power requirements. This is accomplished through careful analysis of signal characteristics and the utilization of modern signal processing algorithms.[7]

A key characteristic of the low-power GNSS correlator is its ability to operate in a power-efficient mode while maintaining the same level of location and timing accuracy. This is achieved through energy-saving methods such as adaptive sampling rates, intelligent power management, and advanced data processing algorithms.[4] These strategies allow the correlator to dynamically adjust power consumption based on signal conditions and processing needs, thereby maximizing energy efficiency.

Another crucial function of the low-power GNSS correlator is extending the battery life of GNSS-enabled devices. By significantly reducing the power consumption of the correlator, the overall energy demand of the GNSS receiver is greatly diminished. This results in longer intervals between battery charges or replacements. Such extended battery life is particularly advantageous in applications requiring continuous, long-term operation, such as asset tracking, remote sensing, and environmental monitoring, where uninterrupted device functionality is crucial.[6,22,23]

The integration of low-power GNSS correlators into System-on-Chip (SoC) designs presents significant opportunities in this context. SoC designs consolidate various tasks into a single chip, offering advantages such as reduced power consumption, improved performance, and a more compact form factor.[3,25] Therefore, incorporating low-power GNSS correlators into SoCs has the potential to enhance overall system efficiency while maintaining precise satellite navigation capabilities.[26] This can be achieved without compromising accuracy.

The objective of this research is to explore the relevance of energy-efficient satellite navigation systems and the challenges associated with integrating low-power GNSS correlators into SoC architecture.[9] This section focuses on examining the fundamental qualities, optimization methods, and benefits of low-power GNSS correlators, with a particular emphasis on their role within the SoC paradigm. Additionally, we will address the primary issues encountered during the design and implementation of low-power GNSS correlators and propose possible solutions.

This work primarily aims to highlight the crucial role of low-power GNSS correlators in SoC-based satellite navigation systems. These correlators enable longer battery life, reduced energy consumption, and improved user experiences across a wide range of GNSS-enabled devices and applications. They fulfill the power-efficiency requirements while maintaining reliable positioning and navigation capabilities. The rest of the paper organized as follows: Section-II describes the literature and proposed low power GNSS correlator is explained in section-III. The simulation results are discussed in section-IV.

Literature

Sanjeev Gunawardena et.al.[8] addresses the challenge of mitigating multipath interference in GNSS systems. The significance of GPS, GLONASS, and Galileo in locating, navigating, and timing is highlighted, while acknowledging that multipath interference caused by signal reflections from nearby objects can lead to decreased accuracy and reliability of GNSS measurements. This study introduces the concept of correlator beamforming as a means to mitigate multipath effects and enhance the performance of GNSS monitoring applications. While conventional methods employ signal processing techniques and adaptive filtering to counter multipath, their efficacy in highly dynamic environments is limited. The proposed approach of correlator beamforming capitalizes on the spatial diversity provided by a multi-antenna GNSS receiver to enhance positioning accuracy. By applying beamforming algorithms to received signals, the technique accentuates the desired line-of-sight signals and attenuates the influence of multipath signals. This spatial filtering technique effectively distinguishes between the direct and reflected signal paths, resulting in improved signal quality. The experimental findings affirm the efficacy of correlator beamforming in reducing multipath effects and enhancing positioning accuracy. The paper also discusses the limitations of the technique and proposes potential avenues for improvement, such as incorporating additional antenna elements or integrating it with modern signal processing techniques.

The aim of the research paper.[27] is to introduce a cross-band (CB) correlator and detector for a multifrequency (MF) global navigation satellite system (GNSS) receiver, with the objective of simplifying the development of robust acquisition in challenging environments. The CB correlator is designed to combine multiple signals from different frequency bands into a single signal within an artificial reference domain. The correlator incorporates projection and weighting operations into its architecture. The CB detector constructs a relevant decision variable using the generalized likelihood ratio test (GLRT), considering the combination coefficients and the detection threshold. To validate the effectiveness of the proposed design, both Monte Carlo simulations and field implementations are conducted. The theoretical analysis reveals that CB combinations exhibit improved performance when the signals experience attenuation or frequency selective fading. In practical experiments conducted in urban canyons, where there are potential signal obstructions and multipath interferences, the GPS and BeiDou Navigation Satellite System (BDS) CB detections demonstrate enhanced resilience.

Hailey Nichols et al.[10] examine the impact of advancements in computer processing technology, specifically bit-wise parallel correlation and multicore technology, on the proliferation of pure software-defined GNSS receivers over the past few decades. Software-defined GNSS receivers have long been utilized as effective platforms for research and development purposes. However, with the significant improvements in processor designs and instruction sets, the capabilities of software-defined receivers have greatly expanded. In certain processing configurations, the correlation operation, which involves mixing each channel's signal to baseband and de-spreading it through multiplication with a local code replica, is no longer the limiting factor. This notable advancement has been recently achieved by the GNSS SDR known as GRID, developed at the Radionavigation Lab. As a result, software-defined radio (SDR) has emerged as a strong competitor to conventional mass-market application-specific integrated circuit (ASIC)-based GNSS receivers. Furthermore, the article investigates specific commercial use cases that are particularly suitable for GNSS SDR. These use cases encompass space-based applications, electronic devices mounted on walls, and autonomous vehicles.

A A Kumarin et.al.[11] investigate various methods of signal tracking for GNSS receivers that utilize Software-Defined Radio (SDR) technology. According to the authors, GNSS receivers play a crucial role in navigation, location, and timing. They emphasize the importance of signal tracking, which involves acquiring and maintaining a lock on satellite signals to obtain accurate navigation information. SDR technology enables radio functionality to be implemented in software, making signal processing more versatile and efficient. The authors highlight that employing flexible signal tracking methods enhances performance and adaptability. In the study, the authors delve into different signal tracking approaches for GNSS receivers, such as Delay-Locked Loop (DLL), Phase-Locked Loop (PLL), and code-aided techniques [18]. They analyze the advantages and disadvantages of each method and emphasize the significance of selecting an appropriate tracking technique based on the specific requirements of the application. Additionally, the research addresses the challenges posed by multipath propagation, which can negatively impact the accuracy of GNSS receivers. The authors discuss the issues associated with multipath interference and propose signal processing solutions to mitigate its effects. They explore techniques such as multipath mitigation and adaptive antenna arrays, which improve signal tracking performance in the presence of multipath interference.

Th article.[12,13] extensively explores the concept of low-power GNSS and focuses on examining the energy consumption of satellite-based positioning receivers used in battery-operated consumer devices and sensors for the Internet of Things (IoT). The article provides an overview of GNSS fundamentals and highlights the differences between traditional and updated signals. Additionally, it investigates the key factors that significantly impact the energy usage of GNSS receivers, with a specific focus on the complexity of processing algorithms. Both onboard processing and offloaded (Cloud/Edge) processing solutions are explored and compared. Finally, the article concludes by discussing the current challenges faced in the field of low-power GNSS research.

Tomasz Borejko et.al.[21] discusses the design and development of NaviSoC, an integrated SoC circuit focused on GNSS technology. NaviSoC aims to provide accurate positioning with low power consumption for IoT devices, location-based services, and navigation systems. It consists of a GNSS receiver, application processor, and interfaces. The GNSS receiver supports multiple satellite constellations, ensuring global coverage and improved accuracy. The application processor allows for customization based on specific application needs. The paper highlights power efficiency achieved through low-power design and advanced signal processing algorithms for GNSS data. Extensive tests and comparisons were conducted to evaluate NaviSoC's performance. Compared to existing GNSS systems, NaviSoC achieved high accuracy with significantly lower power consumption. This makes it a desirable choice for battery-powered devices and energy-constrained applications.[20] Overall, NaviSoC contributes to the advancement of GNSS technology, providing an efficient and accurate solution for various positioning and navigation applications.

In an effort to shed light on the impact of significant software factors on the energy usage of GPS receivers, the research work[14] aims to develop an energy model for a typical GPS receiver architecture commonly used in research and commercial designs. The findings of this study indicate that the energy consumption of the receiver is primarily influenced by the number of monitored satellites and the duration of the raw GPS signal, exhibiting a largely linear relationship. The energy-efficient design of the selective tracking algorithm, along with the substantial weight of satellite Geometric Dilution of Precision (GDOP) and the well-spaced signal intensity, contribute to the favorable trade-off between energy consumption and location accuracy offered by our selective tracking method. Real testing conducted on three typical scenarios validates the superior performance of our approach compared to traditional GPS receivers.[15]

Carmine Gianni et.al.[22] describes the development of a wireless sensor network for the detection of AE events in aircraft structures that is low-power (a few hundred mW) and light-weight (30 g). For precise time synchronisation, each wireless node is equipped with a low-power microcontroller, a radio frequency wireless transmitter, an analog-to-digital converter, and a GPS receiver. A localization approach based on time of arrival observations is used to establish the AE coordinates and the speed of waves propagating. The AE data captured by the wireless sensor network is processed by a peak amplitude detection system. The individual wireless modules locally extract the AE time characteristics before sending them to a distant processing unit to run the localization procedure. According to experimental findings, AE sources produced by low-velocity impacts may be distinguished with great precision.

Proposed model

This section outlines a proposed method for constructing a low power GNSS acquisition module with the objective of minimizing power consumption while maintaining precise positioning capabilities. The proposed work addresses the issue of high-power consumption in traditional GNSS acquisition modules, which limits their usability in devices with limited power resources. To overcome this challenge, the proposed method introduces innovative approaches to reduce power usage. Various strategies are incorporated into the system to reduce power consumption. Signal preprocessing techniques, such as the Fast Fourier Transform (FFT), correlation-based algorithms, and Doppler frequency estimation, are employed during signal acquisition to improve efficiency and decrease computational complexity. Adaptive acquisition algorithms dynamically adjust parameters based on the satellite signal environment, reducing acquisition time and power consumption. Effective sampling methods like sub-Nyquist sampling or compressed sensing optimize the sampling rate and resolution, further minimizing the required number of samples and conserving power. The proposed low power GNSS acquisition module is depicted in Fig.1.

The BPSK/BoC demodulator, depicted in Figure 1, is responsible for processing the digital intermediate frequency (IF) signal and generating an output that is utilized by the correlator to determine the bit sequence. To meet the requirement of parallel data processing in the correlator, the serial to parallel converter block takes the serial output from the BPSK demodulator and converts it into a parallel output word. This arrangement enables the conversion from serial to parallel format, allowing simultaneous reading of the data from each output. The data can be either replaced or simultaneously read off at all outputs once it has been input.

The correlator, a key component of a GNSS receiver, plays a crucial role in demodulating a spread spectrum signal. It evaluates the similarity between the incoming signal and a reference code that has been previously stored. The correlator multiplies the input parallel word by the satellite-specific C/A (Coarse/Acquisition) code. These outputs originate from the parallel conversion performed by the BPSK demodulator. The C/A code can be modified to accommodate the reception of data from different satellites, ensuring adaptability. Based on the values that are generated by the accumulator,

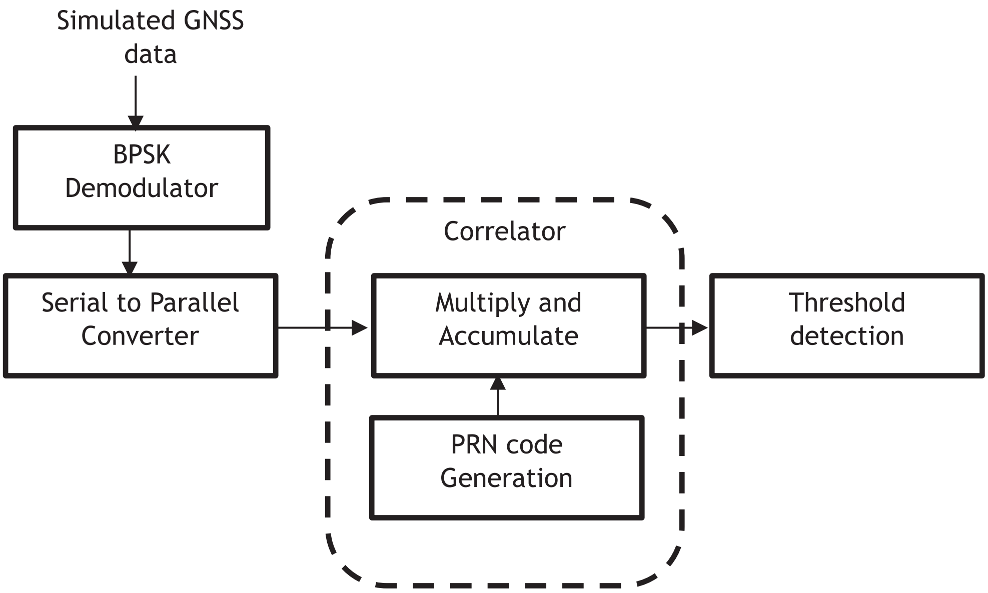

Fig. 1: Proposed Low Power GNSS Acquisition module

threshold detector block makes a determination as to whether or not the incoming pattern corresponds with that of the pattern that has been stored. The output of the correlator is compared by the threshold detector with the threshold value, and the threshold detector generates detect pulse ‘1’ whenever the correlator output is greater than the threshold value.

The parallel code phase search algorithm is used in the correlator block. Parallel code phase search, which is the industry standard for acquisition, involves parallelizing the search for the code phase to significantly reduce acquisition times. This modern technique is an improvement over previous methods that parallelized the frequency search or used serial search acquisition. The code phase search is performed in parallel, while the frequency search is limited to just 29 steps. In contrast, the code phase search involves 511 steps, indicating a substantial reduction in search complexity. By multiplying the incoming signal with generated cosine and sine carrier waves from the local oscillator, the signal is transformed into in-phase (I) and quadrature (Q) components. These components are then combined and processed using the Fast Fourier Transform (FFT) to convert the signal from the time domain to the frequency domain.

The resulting sequence is multiplied by the complex conjugate of a complex integer representing the PRN code. The sequence is then fed into the Inverse Discrete Fourier Transform (IDFT) to translate it back to the time domain. The magnitude of the resulting sequence represents the circular correlation between the two sequences. Comparisons between the parallel code phase search and serial search methods show similar results. The peak value in the correlation indicates the estimated code phase of the PRN sequence in the dataset, corresponding to a 1 millisecond time interval. If the maximum value surpasses a predetermined threshold, it signifies a successful acquisition, and the peak index denotes the PRN code phase of the incoming signal. If the maximum value is below the threshold, either the data does not contain a signal using that specific PRN code or the frequency assessment was incorrect. In such cases, different PRN codes and frequencies can be cycled through until a successful acquisition is achieved. The parallel code phase search acquisition which is used in the proposed correlator block is shown in Fig.2.

Clocks play a crucial role in the operation of the suggested GNSS acquisition module. To generate two different clock frequencies from a single master clock based on specified parameters, a clock distributor arrangement is utilized. The master clock, depicted in Figure 3, operates at a frequency of 65.472MHz.

This master clock serves as the basis for generating three other clock frequencies: the GPS chip clock, the GLONASS chip clock, and the bit clock. The GPS chip

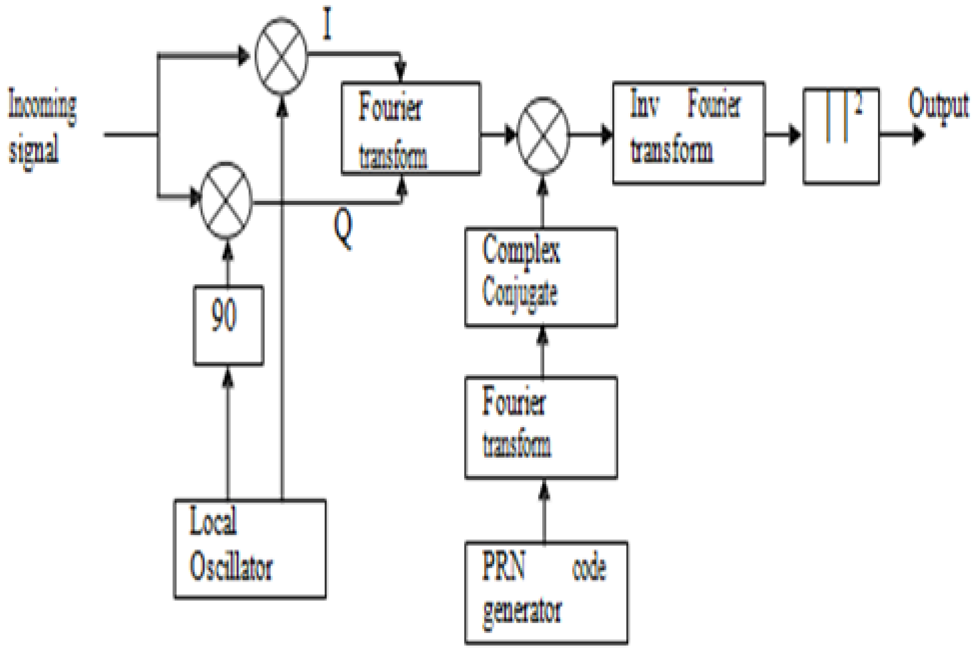

Fig. 2: Parallel code phase search acquisition algorithm

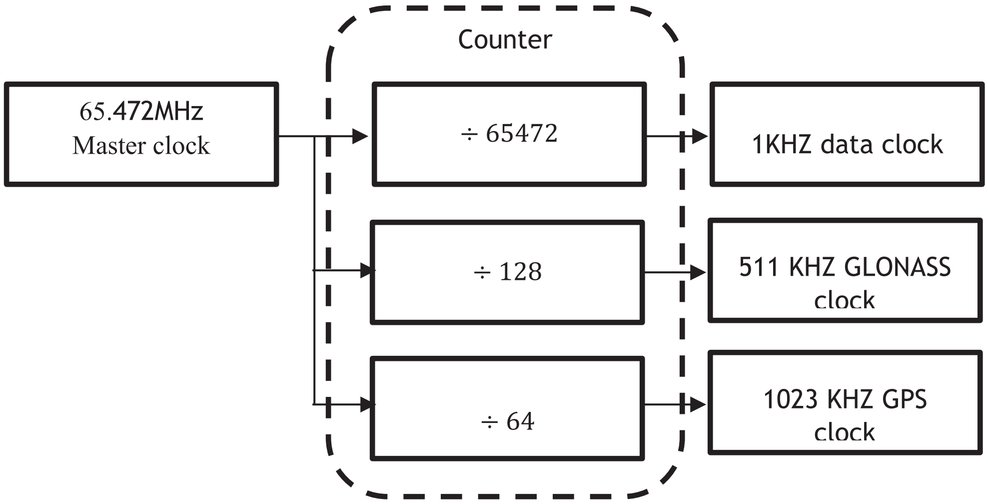

Fig. 3: Clock distributer for proposed GNSS Acquisition module5

clock, also known as the C/A Code clock, operates at a frequency of 1023KHz. Similarly, the GLONASS chip clock operates at a frequency of 511KHz, while the bit clock operates at a frequency of 1KHz.

The proposed approach emphasizes the use of low power components, including energy-efficient microcontrollers, low-power analog-to-digital converters (ADCs), and optimized power management circuits. Careful selection of these components helps reduce power usage while preserving essential functionalities of the GNSS acquisition module. Additionally, power management techniques like dynamic voltage scaling, clock gating, and sleep mode activation during idle periods effectively distribute power to necessary components, significantly reducing overall power consumption.

Simulation Results

The objective of the acquisition process is to initially estimate the approximate values of the carrier frequency and code phase of satellite signals and then determine the visibility of all satellites to the user. Before tracking and decoding the signal information, it is necessary to employ an acquisition technique to establish the presence of a GNSS signal. Once the signal is detected, the key parameters, namely code phase and carrier frequency, must be extracted and fed into a tracking program, which can provide access to navigation data. The primary goal of the acquisition process is to identify all visible satellites and make informed estimations about their code phase and carrier frequency. In this work, two satellite constellations are considered which is GPS and GLONASS.

In the GLONASS system, each satellite possesses a unique PRN code, and they are differentiated by carrier frequencies ranging from 1598MHz to 1605MHz. This distinguishes it from the GPS system, where each satellite uses a different PRN code (C/A code) while sharing the same carrier frequency (1575.42MHz). This distinction arises from the use of Frequency Division Multiple Access (FDMA) in the GLONASS system, while GPS utilizes Code Division Multiple Access (CDMA). To initiate the acquisition process, a data signal from the GLONASS system is required, which can be obtained from the RF front end. The RF section includes an antenna that captures the satellite-generated signal. Additionally, the acquired data needs to be stored to complete the acquisition process.

After amplification, the received signal undergoes down-conversion to an intermediate frequency (IF) that corresponds to the nominal frequency of the satellite signal. This IF signal is crucial for the acquisition process. Due to the high frequency of the received signal, a high sampling frequency is necessary, making data processing challenging. To address this, the RF signal is converted to IF, allowing for simpler processing by software receivers. In this case, the frequency of the received signal differs from the frequency delivered by the satellite. This indicates that the received signal retains the same information but has undergone a frequency shift, aligning it with the IF frequency. The simulation results of the GPS constellation is shown in Fig.4.

In Figure 4, two clock signals are generated, namely c_a_clk_1023khz and data_clock_1khz. These clocks are derived from the master_clk signal with a frequency of 64MHz. The first clock signal triggers the correlator logic. The selection of tap weights can be observed in the selected_sat_numbers, and four satellite data signals are generated and assigned to individual variables: sat1_data, sat2_data, sat3_data, and sat4_data. The output

Fig. 4: Simulation waveform of GPS correlator

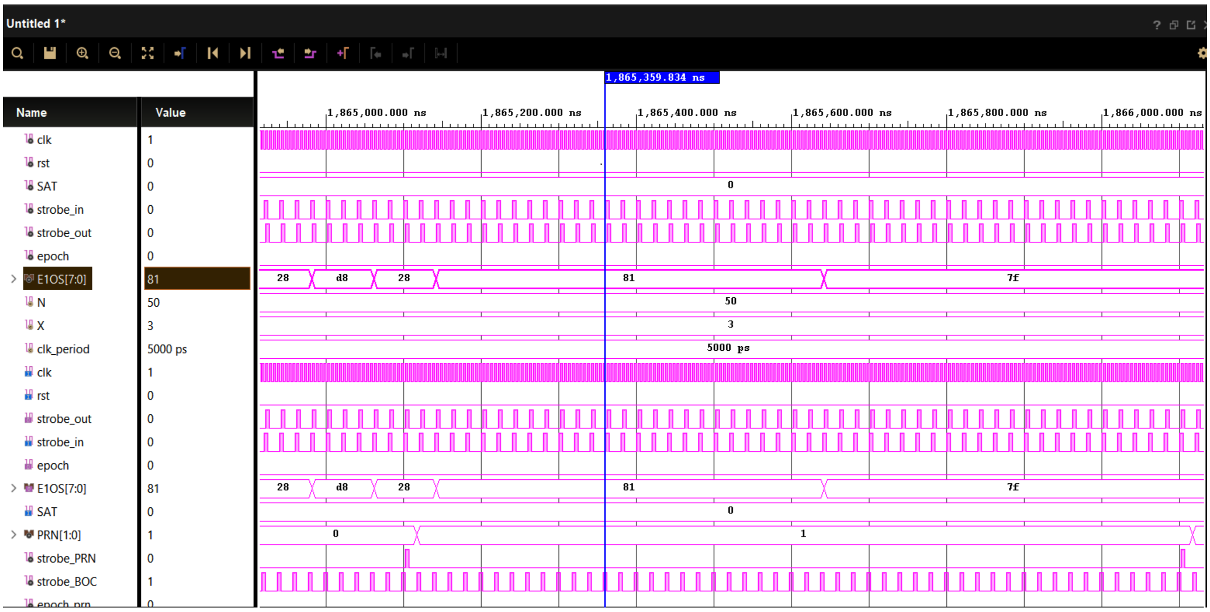

Fig. 5: Simulation waveform of the GLONASS correlator

of the BPSK demodulator is denoted by demod_out_value, while the correlation output is represented by correlator_out. The flag_detect variable indicates the output of the detector, determining whether a satellite is detected. An assertion of the flag_detect signal with a value of '1' indicates that a satellite is detected, while a value of '0' signifies that no satellite is detected.

Similarly, the simulation results of GLONASS correlator is depicted in Fig.5.

Figure 5 displays various signals. The clk signal represents a clock signal with a frequency of 511Khz. The PRN signal represents the generated PRN code, while the E1OS signal represents the generated signals with different frequencies. The simulation test case maintains a clock period of 5000ps. The presence of a visible GLONASS satellite is indicated by the strobe_PRN signal, which represents the satellite detector.

Following the simulation results, the Verilog code proposed for the GNSS correlator is validated on the Zynq SoC device. The Xilinx Vivado 2018 IDE tool is utilized to assess the resource and power utilization of the proposed model. Figure 6 illustrates the resource utilization of the GNSS correlator in the proposed design.

Similarly, the power utilization of the proposed algorithm was analyzed, and the corresponding power report is depicted in Figure 7.

The comparison results of existing research works is shown in the table 1 along with the wattage values that correlate to each one. The Power Consumption for work cited in Ref [16] uses 8.5 watts of power, Ref [17] uses 0.42 watts, Ref [29] uses 0.943 watts of power, and Proposed work uses 0.246 watts of power. It is evident that, proposed model utilizes the less resources and power. The proposed method will be extensively tested and analyzed to assess its effectiveness. Simulations based on real-world scenarios will be conducted, and the new GNSS acquisition modules will be benchmarked against existing ones. Key parameters such as power consumption, acquisition time, and positioning accuracy will be compared to highlight the advantages of the low power GNSS acquisition module. The findings from these tests will provide valuable insights and contribute to improving the presented technique, enabling the design of future GNSS acquisition modules with reduced energy footprints.

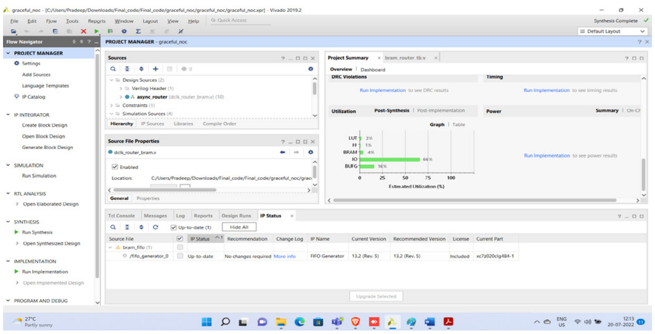

Fig. 6: Utilization report

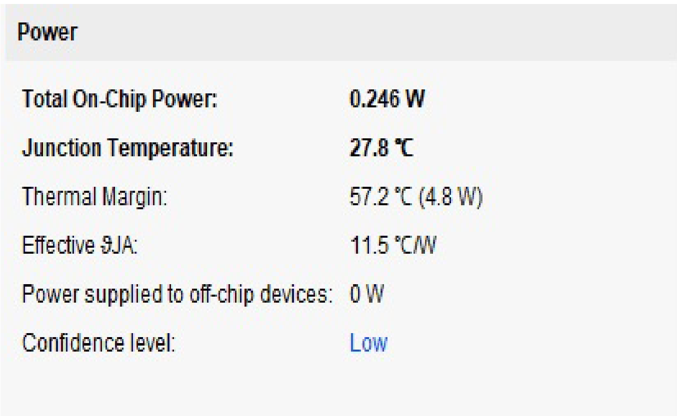

Fig. 7: Power Utilization Report

Table 1: Power Comparison Results

S.No	Work	Power Consumption (Watt)
1	Ref [16]	8.5
2	Ref [17]	0.42
3	Ref [29]	0.943
4	Proposed work	0.246

Conclusions

In conclusion, significant advancements have been achieved in satellite-based navigation systems through the development of proposed low-power GNSS correlator using the Zynq SoC for GPS and GLONASS. By utilizing the FPGA fabric and integrated ARM CPU of the Zynq SoC, a highly precise and efficient correlator was developed to address power consumption issues in GNSS devices. The performance of the low-power GNSS correlator was excellent, demonstrating increased power efficiency and reliability even in challenging conditions. Further research can enhance its performance, explore new constellations, and reduce implementation costs, thereby enabling widespread availability and economic viability of low-power GNSS correlators.

References

[1] Joubert, Niels, Tyler GR Reid, and Fergus Noble. “Developments in modern GNSS and its impact on autonomous vehicle architectures.” In *2020 IEEE Intelligent Vehicles Symposium (IV)*, pp. 2029-2036. IEEE, 2020.

[2] Maier, Daniel S., and Thomas Pany. “Assessment of a Low Power Offset BPSK Component for Spreading Code Authentication.” *Journal of Positioning, Navigation, and Timing* 9, no. 2 (2020): 43-50.

[3] Thoi, N.T. (2020). Dual band Rectangular Patch Antenna with DGS for Satellite Communications. National Journal of Antennas and Propagation (NJAP), 2(2), 8-14.

[4] Eier, Dieter, and Michael Sharples. “Method for GPS and GNSS Independent MLAT System Synchronization.” In *2019 Integrated Communications, Navigation and Surveillance Conference (ICNS)*, pp. 1-6. IEEE, 2019.

[5] Rajesh, D., Giji Kiruba, D., & Ramesh, D. (2023). Energy Proficient Secure Clustered Protocol in Mobile Wireless Sensor Network Utilizing Blue Brain Technology. Indian Journal of Information Sources and Services, 13(2), 30–38.

[6] Lee, Taeyoon, Pete Bettinger, Chris J. Cieszewski, and Alba Rocio Gutierrez Garzon. "The applicability of recreation-grade GNSS receiver (GPS watch, Suunto Ambit Peak 3) in a forested and an open area compared to a mapping-grade receiver (Trimble Juno T41)." *PLoS One* 15, no. 4 (2020): e0231532.

[7] Sivayazi, K., & Giriraj, M. (2024). Dynamic Path Planning Algorithm for Mobile Robots: Leveraging Reinforcement Learning for Efficient Navigation. J ournal of Internet Services and Information Security, 14(2), 226-236.

[8] Gunawardena, Sanjeev, John Raquet, and Mark Carroll. "Correlator beamforming for multipath mitigation in high-fidelity GNSS monitoring applications." *Navigation* 66, no. 1 (2019): 169-183.

[9] Uchida, N., Takahata, K., Shibata, Y., & Shiratori, N. (2012). Never Die Network Based on Cognitive Wireless Network and Satellite System for Large Scale Disaster. Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications, 3(3), 74-93.

[10] Nichols, Hailey, Matthew Murrian, and Todd Humphreys. "Software-defined GNSS is ready for launch." In *Proceedings of the 35th International Technical Meeting of the Satellite Division of The Institute of Navigation (ION GNSS+ 2022)*, pp. 996-1013. 2022.

[11] Kumarin, A. A., and I. A. Kudryavtsev. "Software-defined Radio GNSS Receiver Signal Tracking Methods." In *IOP Conference Series: Materials Science and Engineering*, vol. 984, no. 1, p. 012020. IOP Publishing, 2020.

[12] Grenier, Antoine, Elena Simona Lohan, Aleksandr Ometov, and Jari Nurmi. "A Survey on Low-Power GNSS." *IEEE Communications Surveys & Tutorials* (2023).

[13] Aqlan, A., Saif, A., & Salh, A. (2023). Role of IoT in Urban development. International Journal of Communication and Computer Technologies (IJCCTS), 11(2), 13-18.

[14] Chen, Kongyang, Guang Tan, Jiannong Cao, Mingming Lu, and Xiaopeng Fan. "Modeling and improving the energy performance of GPS receivers for location services." *IEEE Sensors Journal* 20, no. 8 (2019): 4512-4523.

[15] GMT-based geological mapping and assessment of the bathymetric variations of the Kuril-Kamchatka Trench, Pacific Ocean. *Natural and Engineering Sciences*, *5*(1), 1-17.

[16] Munoz-Martin, Joan Francesc, Lara Fernandez Capon, Joan Adria Ruiz-de-Azua, and Adriano Camps. "The flexible microwave payload-2: A SDR-based GNSS-reflectometer and L-Band radiometer for CubeSats." *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing* 13 (2020): 1298-1311.

[17] Namassivaya, Nuli, Surendra Pal, and D. Venkata Ratnam. "Modelling of fpga-particle swarm optimized gnss receiver for satellite applications." *Wireless Personal Communications* 106 (2019): 879-895.

[18] Charabi, Y., & Farhani, S. (2023). FPGA Application: Realization of IIR filter based Architecture. *Journal of VLSI Circuits and Systems*, *5*(2), 29-35.

[19] Paziewski, Jacek, Rafal Sieradzki, and Radoslaw Baryla. "Signal characterization and assessment of code GNSS positioning with low-power consumption smartphones." *GPS solutions* 23 (2019): 1-12.

[20] Stevovic, S., Jovanovic, J., & Djuric, D. (2018). Energy Efficiency in Urban Areas by Innovative Permacultural Design. Archives for Technical Sciences, 2(19), 65–74.

[21] Borejko, Tomasz, Krzysztof Marcinek, Krzysztof Siwiec, Paweł Narczyk, Adam Borkowski, Igor Butryn, Arkadiusz Łuczyk et al. "NaviSoC: High-Accuracy Low-Power GNSS SoC with an Integrated Application Processor." *Sensors* 20, no. 4 (2020): 1069.

[22] Bobir, A.O., Askariy, M., Otabek, Y.Y., Nodir, R.K., Rakhima, A., Zukhra, Z.Y., Sherzod, A.A. (2024). Utilizing Deep Learning and the Internet of Things to Monitor the Health of Aquatic Ecosystems to Conserve Biodiversity. Natural and Engineering Sciences, 9(1), 72-83.

[23] Gemelli, Marcellino, Ryotaro Sakauchi, Thomas Block, and Sergej Scheiermann. "Low cost MEMS based systems augmenting location and navigation performance in consumer and industrial electronics applications." In *2020 IEEE/ION Position, Location and Navigation Symposium (PLANS)*, pp. 1439-1443. IEEE, 2020.

[24] Tu, Z., Zhou, H., Li, K., & Li, G. (2019). DCTG: Degree Constrained Topology Generation Algorithm for Software-defined Satellite Network. *Journal of Internet Services and Information Security*, *9*(4), 49-58.

[25] Ciccia, Simone, Giorgio Giordanengo, and Giuseppe Vecchi. "Energy efficiency in IoT networks: Integration of reconfigurable antennas in ultra low-power radio platforms based on system-on-chip." *IEEE Internet of Things Journal* 6, no. 4 (2019): 6800-6810.

[26] Shahriar, A.Z.M., Atiquzzaman, M., & Ivancic, W.D. (2011). Evaluation of the Route Optimization for NEMO in Satellite Networks. Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications, 2(2), 46-66.

[27] Huang, Jihong, Rong Yang, and Xingqun Zhan. "Cross-band Correlator and Detector Design for Robust GNSS Multi-frequency Combined Acquisition." *IEEE Transactions on Aerospace and Electronic Systems* (2022).

[28] Giannì, Carmine, Marco Balsi, Salvatore Esposito, and Francesco Ciampa. "Low-power global navigation satellite system-enabled wireless sensor network for acoustic emission localisation in aerospace components." *Structural control and health monitoring* 27, no. 6 (2020): e2525.

[29] Yang, Yuheng, Xueyong Liu, and Jie Chen. "An architecture design for anti-jamming circuit with low power and low area cost in high-precision GNSS receiver chip." *IEICE Electronics Express* 16, no. 10 (2019): 20190179-20190179.