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Design of Novel High Speed Energy Efficient Robust 4:2 Compressor

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Abstract

Multipliers are crucial in deciding the overall efficiency of the arithmetic circuits. Compressors are one of the vital components of the multipliers. This paper presentsa new architecture for a 4:2 compressor, utilizing a novel truth table as well as internal equations. Additionally, the research investigates the methodology to incorporate a fast compressor into the XOR-XNOR circuit framework. Significantly, the suggested design has fewer transistors as compared to the existing 4:2 compressors. Four different and existing 4:2 compressors are examined closely for the comparative analysis with the proposed circuit. The suggested structure is compared with the latest ones found in modern publications, consideringthe power usage, latency as well as space optimization along with the Monte Carlo and Corner analysis. The proposed compressor has 49% lesser delay, 53% lower Power Delay Product and 76.27% lesser Energy Delay Product than the other prevailing compressor designs. Architecture simulation is performed using Cadence Virtuoso tool in 45nanometer CMOS technology with power supply of 1 volt.

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Introduction

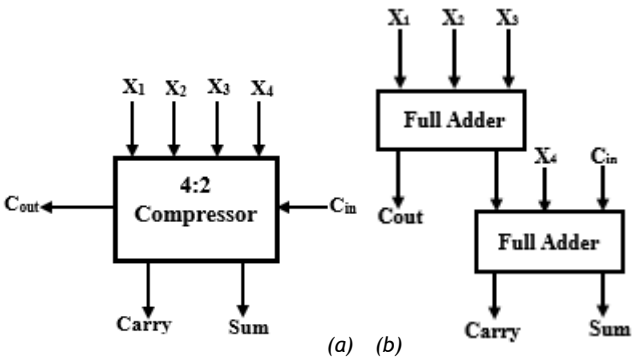
Over the past decade, the semiconductor industry has seen a significant rise in integrating complex multimedia features into the mobile gadgets. Earlier built on analog circuit approaches, the front-end communication via wireless circuitries has got shifted into the digital sphere to provide substantialpower minimizationand high-density integration through direct conversion design.[1,2] Thus, its vital to explore carefully designed deep sub-micron complementary metal oxide semiconductor (CMOS) technologies to fulfill the rigorous demand of the advanced low latency circuits with minimal power consumptionbaseddigital signal processing (DSP) devices. Within verylargescale integration (VLSI) systems,[2] fast arithmetic calculation units, including adders and multipliers, dominate as the most employed circuits. Toimplement certain algorithms for DSP applications like convolution and filtering,[3-5] microprocessors and digital signal processors rely on the effective operation of general-purpose arithmetic logic units (ALUs) and units of floating-point processors. In many applications, multipliers are now necessary components in the architecture of a circuit which manages the speed and computing complexity. Its integrated combinational circuits have great potential for enhancing the power-latency product of the multiplier during circuit construction with voltage scaling and inventive CMOS logic designs.[6,7] A quick array or tree multiplier typically consists of following three sections:

- a carry-save structured accumulator that further reduces the partial products matrix to just the addition of two operands;
- a Booth encoder, which is responsible for the generation of fewer partial products;
- a fast carry propagation adder[8] (CPA) that calculates the final binary outcome from its retained carry representation.

The subsequent stage (termed the carry-save adder (CSA) tree [9]) for accumulating the second partial product tends to be the most power-intensive and occupies a major portion of silicon area.

Also, it largely contributes to the overall delay within these sub circuits. In modern high-speed systems (including digital signal processing multipliers and processors), the 4:2 compressors are frequently used to lower the latency of the accumulation step.[8] The block diagram of a 4:2 compressor if given in Figure 1(a). Thesecompressors are mostly employed in parallel multipliers to add partial products produced by various algorithms such as the booth algorithm. The accumulation stage consists of compressors and thus it is responsible for much of the overall circuit delay. Therefore, the compressor delay reduction can cause a substantial impact on the overall latency of the system.

For high-speed processing applications, several 4:2 compressor circuits have been designed as evidenced by the literature.[10-12] Many approaches have been put forthby the scientific community for the implementing the 4:2 compressors, with a particular emphasis on minimizing power consumption.[11-13] Considerable number of transistors are required for some compressors that are intended to run at low supply voltages. On the other hand, alternate designs that use fewer transistors may struggle to function effectively at low power supply or fail to adequately drive the later stages.[14-16] As shown below in Figure 1(b), by utilizing two Full Adders in succession on the sum path,[17,18] it is possible to create a 4:2 compressor with three outputs and five inputs. Here, bits X_1, X_2 and X_3 are fed as input to the first 1-bit full adder. The output sum of this adder is fed as input to the second 1-bit adder along with X_4 and C_{in}. Final outputs of the 4:2 compressor circuit are Sum, Carry and C_{out}.



(a) (b)

Fig.1:(a) Block diagram of a 4:2 compressor [22] (b) a Conventional 4:2 Compressor [22] comprising of two full adders

Different designs and realizations of 4:2 circuits can be found, with most of them using either XOR-XNOR circuits or multiplexers (MUX) as their main components. In other words, we can say that a compressor is a combinational circuit, which is responsible for the generation of a sum bit and several carry bits at the output terminals after receiving all the inputs of same significance.[19,20] An adder differs from a compressor. The adder performs the addition of two operands having different levels of significance.However, the compressor performs addition of numerous bits of same significance.

This paper investigates new design approaches that use advanced CMOS process technology to create 4:2 compressor circuits having low power that can provide sufficient drive strength even at extremely minimal voltages. The 4:2 compressors built using XOR-XNOR cell show better efficiency in terms of power upon comparison with another similar designs. Its robustness is proven by Monte Carlo and corner analysis, which depicts its ability to withstand under worst case scenario of uncertainty and soft transient errors. Moreover, a redesigned novel truth table as well as novel equations is proposed.

The paper is structured as follows: Section II outlines the state of the art 4:2 compressor architectures. Section III introduces the proposed architecture for a 4:2 compressor. Simulation results and analysis are presented in Section IV followed by corner analysis in Section V. The layout design is discussed in Section VI. We conclude in Section VIII.

Literature Review

One of the main factors to accelerate the speed of a multiplier circuit is minimization of the partial product. Earlier,the reduction of partial products is accomplished by multi-operand adders rather than conventional adders. For designing these types of adders, a compressor and a counter is required. Gajski et al. has suggested a compressor which did the computation horizontally.[20] It can perform addition of bits having different weights. Due to this feature, it provides symmetrical architecture. Furthermore,Ciminiera et. al.[21] gives the modified version of beforehand mentioned compressor. It also provides regular architecture but having lower number of cells. But one of the major drawbacks of these types of compressors is raising of vertical paths.The Figure 1 illustrates the conventional 4:2 compressor circuit, as suggested by Nagamatsu et. al.[22] With the assistance of two full adders, the 4:2 compressor circuit was constructed. As mentioned in Figure 1 on previous page, Nagamatsu et. al. designed the compressor comprises of two full adder circuits.[22] First full adder will perform the addition of X_1, X_2 and X_3 bits, because of which two outputs will be generated as carry C_{out} and intermediate sum S_0. In the continuation of it, the second full adder task is to perform addition of S_0 generated from previous stage of the full adder, input carry C_{in} and X_4, this leads to generation of *Carry* and *Sum* as output signals.

The Figure 2 demonstrates how an addition operation is performed in a 4:2 compressor circuit. For better clarity, an example is given in which four inputs X_1, X_2, X_3, X_4 and previous input C_{in} bits are taken as "01101". S_1 is the intermediate sum which is generated in the stage 1 operation. The final outputs are *Sum* and *Carry*.

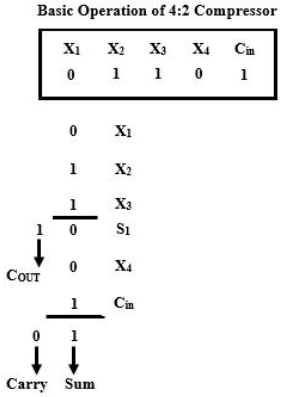


Fig.2: Example of 4:2 Compressor depicting the basic operation

The logical equation for the 4:2 compressor is stated below as equation (1) by Nagamatsu et al [22]. With the assistance of two full adders, the 4:2 compressor circuit was constructed. The logical equation for the 4:2 compressor is stated in equation (1).

$$X_1+X_2+X_3+X_4+C_{in}=Sum+2.(Carry+C_{out}) \quad (1)$$

Upon analysis of the employment of compressor in the reduction structure over traditional full adder based multiplier circuits, the conclusion was made that carry propagation latency gets minimized. This configuration has delay of four XOR logic gates. Prasad et. al.[2] suggested two 4:2 compressor based architecture which is comprised of multiplexer circuits accompanied by XOR logic gate. This structure comprises of total 48 transistors as shown in Figure 3 and Figure 4. It has latency of three XOR gates. However, this design provides complemented output and its reverse at each phase of process.

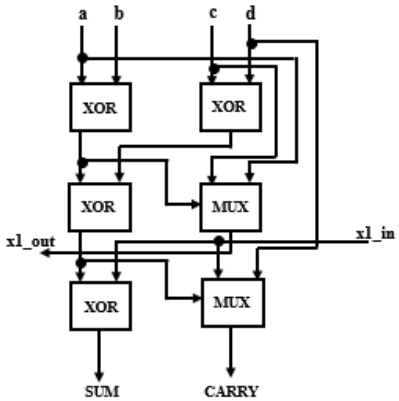


Fig. 3: A 4:2 Compressor design-I circuit by Prasad et. al. [2]

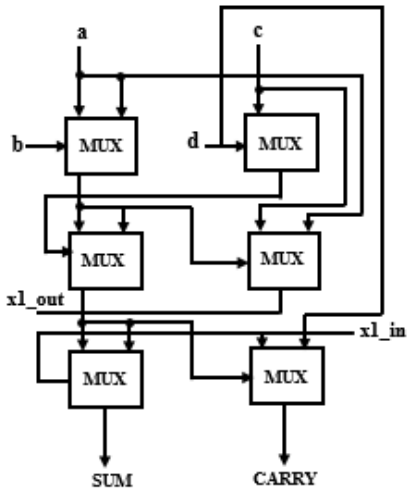


Fig.4:4:2 Compressor design-II circuit by Prasad et. al. [2]

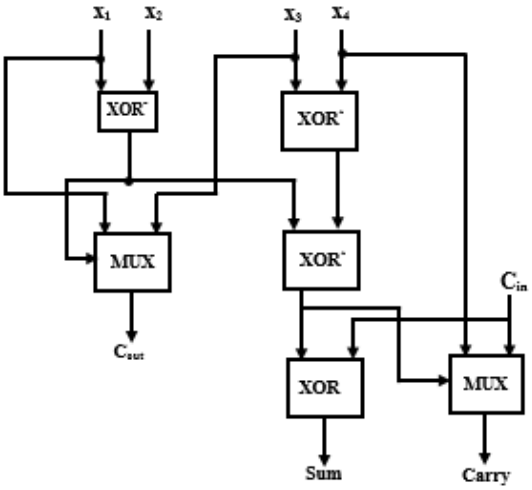


Fig.5: 4:2 Compressor circuit proposed by Chang et. al. [23]

Chang et. al. [23] suggested a new 4:2 compressor design which comprises of a total of 50 transistors as demonstrated in Figure 5, which is responsible for generation of actual and its reverse output results. Due to this approach, it leads to a consistent layout. For generation of 'Sum' output signal, an XNOR/XOR circuit (implemented with ten transistors) is utilized. With the assistance of six transistors based 2:1 multiplexer circuit, the author also incorporates the carry generator module whose task is to produce *Carry* and C_{out} output logic levels. This architecture is based on the following equations (2)-(5) proposed in:[23]

$$C_{out} = (x_1 \oplus x_2).x_3 + x_1.x_2$$
$$= (x_1 \oplus x_2).x_3 + \overline{(x_1 \oplus x_2)}.x_1 \quad (2)$$
$$s = (x_1 \oplus x_2 \oplus x_3) \quad (3)$$
$$Sum = s \oplus x_4 \oplus c_{in} = x_1 \oplus x_2 \oplus x_3 \oplus x_4 \oplus c_{in} \quad (4)$$
$$Carry = (s \oplus x_4).c_{in} + s.x_4$$
$$= (x_1 \oplus x_2 \oplus x_3 \oplus x_4) \oplus c_{in} + \overline{(x_1 \oplus x_2 \oplus x_3 \oplus x_4)} \oplus x_4 \quad (5)$$

Yuan et. al.[24] introduced two architectures of 4:2 compressor design based on pass transistor logic having 44 transistors and transmission gate logic design style consists of total 56 transistors. Pass transistor and transmission gate style is used for creating intermediate stage Multiplexers. Kumar et. al.[25] presented the circuit that incorporates total 40 transistors in its architecture. It depends on integration of design style of pass transistor logic and transmission gate logic. The formation of this circuit is as per the equations (6)-(8). The logic decomposition of this circuit is displayed in Figure 6 which has critical path delay of $\Delta_{XOR}+2*\Delta_{MUX}$.

$$Sum = (X_1 \oplus X_2).(\overline{X_3 \oplus X_4}) + (\overline{X_1 \oplus X_2}).(X_3 \oplus X_4).\overline{C_{in}} + \quad (6$$

$$\overline{(X_1 \oplus X_2).(\overline{X_3 \oplus X_4}) + (\overline{X_1 \oplus X_2}).(X_3 \oplus X_4).C_{in}} \quad (7)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4)\, C_{in} + (\overline{X_1 \oplus X_2 \oplus X_3 \oplus X_4})\, X_4 \quad (8)$$

$$C_{out} = (X_1 \oplus X_2)X_3 + (\overline{X_1 \oplus X_2})X_1$$

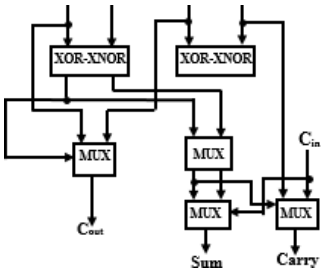


Fig.6:A 4:2 Logic decomposition of 4:2 compressor by Kumar et. al.[25]

However, Pishvaie et. al.[26] suggested the modified version of 4:2 compressor circuit, in which author decompose all the XOR gates and replaced them by AND/NAND and OR/NOR logic gates. Total 74 transistors are used by the author for constructing his circuit as mentioned in Figure 7. Complementary CMOS (CCMOS) logic design is utilized for making this architecture. Critical path delay in it is calculated as $3\Delta_{AND} + 3\Delta_{NOR}$. Furthermore,Pishvaieet. al. [29] provided another 4:2 compressor that includes XNORlogic gate rather than XOR gate because of reduced latency of CMOS designstyle. Itsdesign is displayed in Figure 8, where two designs are shown, comprises of total 60 and 70 transistors respectively having delay in critical path of $\Delta_{FA} + \Delta_{XNOR}$. The half adder and full adder circuits are constructed by using XNOR gate.

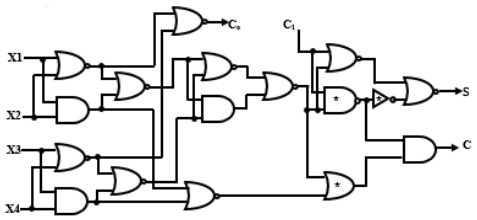


Fig.7:A 4:2 Logic decomposition of 4:2 compressor by Pishvaieet. al.[26]

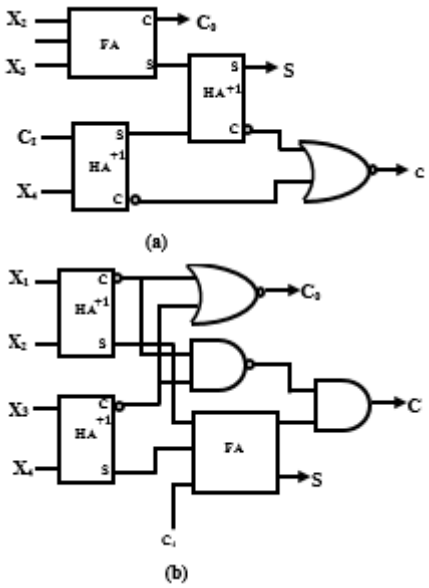


Fig. 8. (a) A 4:2 Compressor design-I (b) A 4:2 Compressor design-II proposed by Pishvaieet. al.[27]

S. Veeramachaneni[28] laid emphasis on use of Multiplexers in his 4:2 compressor design. Author implemented its circuit as per equations mentioned in equations (6)-(8). In total 66 transistors count are employed while constructing this design. Here, difference is in MUX* circuit design as depicted in Figure 9. This is inserted in intermediate stage due to its limiting driving capabilities. It is constructed by using transmission gate design. Latency of critical path in this 4:2 compressor design is $\Delta_{XOR} + 2*\Delta_{MUX}$.[28]

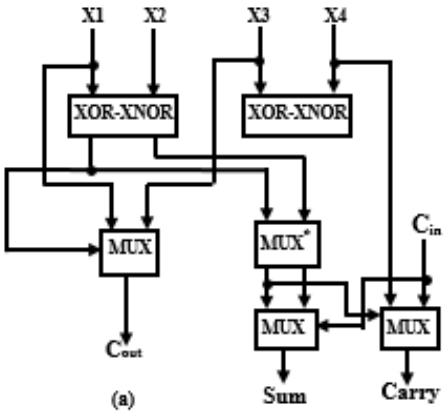


Fig. 9 (a) 4:2 Compressor proposed by S. Veeramachaneni[28]

Two new designs of enhanced 4:2 compressor was suggested by Pishvaie.[29] These designs were implemented by 62 and 60 transistors, respectively.This is based on substituting an optimized full adder for an integral part of logic circuit. The main idea is to generate the carry signal by using an already available signal in sum path. Figures 10(a) and 10(b) demonstrated these two architectural designs.

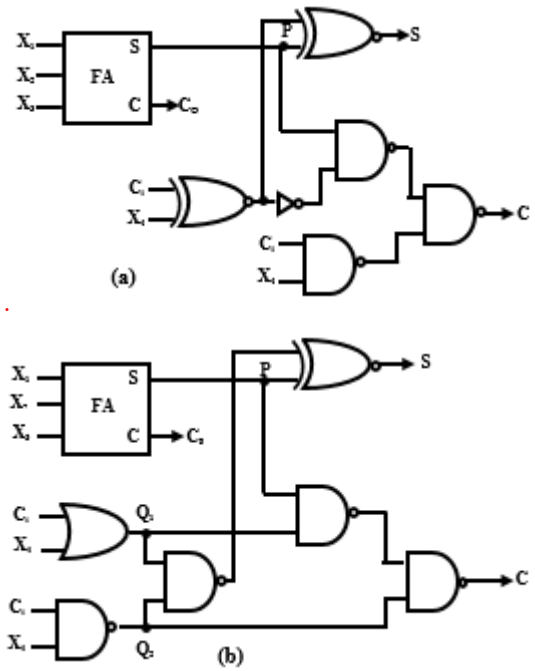


Fig. 10. 4:2 Compressor circuit proposed by Pish-vaieet. al. [29] (a) Design 1 (b) Design 2

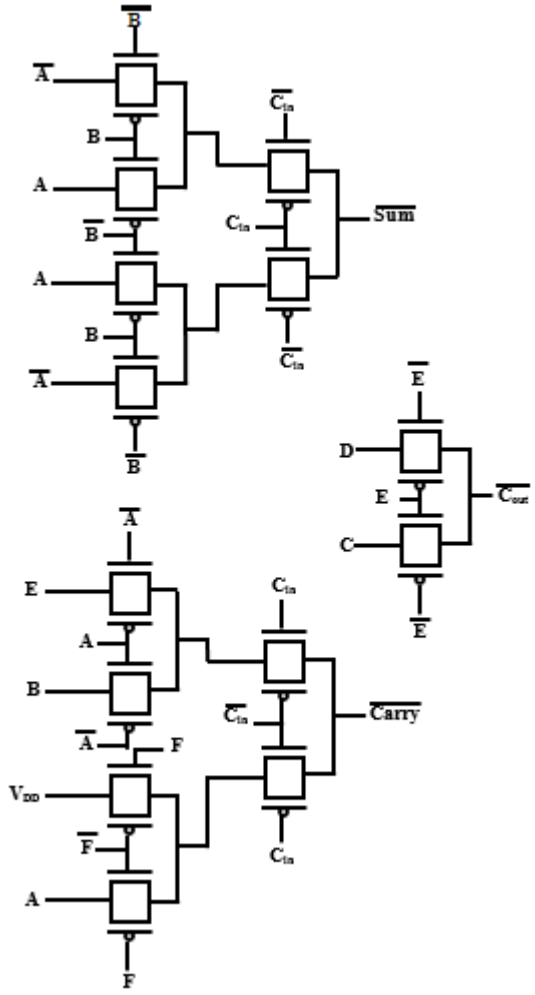


Fig.11: 4:2 Compressor Design proposed by Fathi[30]

To develop high speed arithmetic circuits, Fathi[30] proposed a novel 4:2 compressor structure which consists static CMOS and pass transistor logic. This is redrawn below in Figure 11. Further, transmission gate design style is incorporated while realizing the architecture for *Sum*, *Carry*andC_{out} logic as mentioned in Figure 11. This design is composed of 70T transistors. Researcher used the modified equation as mentioned below in (9)-(11). The overall gate level latency of this configuration can be described as $\Delta_{XOR} + 2\Delta_{TG}$.

$$Sum = I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus C_{\text{in}} \quad (9)$$

$$\overline{Carry} = (\overline{I_1 \oplus I_2}).(\overline{I_3 + I_4}) + (I_1 \oplus I_2).(I_3 \oplus I_4).\overline{C_{in}} + ((\overline{I_3 I_4}) + (I_3.I_4).(I_1 \oplus I_2)).C_{\text{in}} \quad (10)$$

$$\overline{C_{\text{out}}} = (I_3 + I_4).(\overline{I_1 + I_2}) + (\overline{I_3 + I_4})(\overline{I_1 I_2}) \quad (11)$$

M. Ghasemzadeh,[31] introduced novel arrangement having 45 transistors in it that makes use of reference voltage generator to counteract the effect of process variation. The key idea behind it is that the process of generating Cout need to be distinct from the process that generates C_{in} in order to avoid any fluctuation in signal level of C_{in} from impacting the signal values of C_{out}. A voltage generator approach serves to create C_{out}& Carry logic signals.

Proposed Work

Numerous approaches may be used to create a new compressor circuit. By rearranging the logic equations in novel way, an effective design may be achieved and creating a new idea using the truth table as a framework. The novel and creative method for creating a suitable 4:2 compressor originates from unique designing of truth table. The novel truth table is derived in this paper as mentioned in Table I. The C_{out}, Sum and Carry generating techniques represent the primary novelty of the suggested design. suggested design. The proposed equations for a new 4:2 compressor are given in equations (12)-(14):

$$C_{out} = (X_1 \oplus X_3).X_2 + (X_1 \odot X_3).X_1 \quad (12)$$

$$Carry = (X_4 \odot C_{in}).X_4 + (X_1 \odot X_3).(X_4 \oplus C_{in}).X_2 + (X_1 \oplus X_3).(X_4 \oplus C_{in}).\overline{X_2}$$

OR

$$= (X_4 \odot C_{in}).X_4 + (X_4 \oplus C_{in}).M \quad (13)$$

where, $M = (X_1 \odot X_3).X_2 + (X_1 \oplus X_3).\overline{X_2}$

$$Sum = (X_1 \odot X_3).(X_4 \oplus C_{in})\overline{X_2} + (X_1 \oplus X_3).(X_4 \oplus C_{in})X_2 + (X_1 \odot X_3).(X_4 \odot C_{in})X_2 + (X_1 \oplus X_3).(X_4 \odot C_{in})\overline{X_2}$$

OR

$$= (X_4 \oplus C_{in}).\overline{M} + (X_4 \odot C_{in}).M \quad (14)$$

From the Table I (as shown on the next page), when $(X_1 \cdot X_3)$ result is one, C_{out} will become equivalent to X_1 else it will be equal to X_2. While in case of generating Sum logic, we may deduce from Table I that there are two groups, namely,*b1* which consists of $(X_2, \overline{X_2})$ and b2 that comprises of $(\overline{X}_2, X_2)$. This information is useful for creating the Sum signal. As an example, for *b1* group, if $(X_4 \oplus C_{in})$ results in zero, then output of *Sum* will be X_2 else it will be inverse of X_2. The equation for *Sum* is mentioned in equation (16). As per Table I, in case of Carry signal if $(X_4 \oplus C_{in})$ result in zero level, then the value of output can be determined based on X_4. This means it will get independent of output result of $(X_1 \oplus X_3)$, but if $(X_4 \Theta Cin_{IN})$ gives low logic then output result will rely on X_2 or its inverse. The implementation of proposed 4:2 compressor at the gate level can be seen in Figure 12, which depicts the implementation of the truth table, shown below as Table I.

Table. I: Proposed Truth Table

X_2	X_3	X_4	C_{in}	SUM	CARRY	C_{out}
0	0	0	0	X_2	X_1	X_1
0	0	0	1	$\overline{X}_2$	X_1	X_1
0	0	1	0	$\overline{X}_2$	X_1	X_1
0	0	1	1	X_2	X_4	X_1
0	1	0	0	$\overline{X}_2$	X_4	X_1
0	1	0	1	X_2	X_3	X_1
0	1	1	0	X_2	X_3	X_1
0	1	1	1	$\overline{X}_2$	X_3	X_1
1	0	0	0	X_2	X_3	X_1
1	0	0	1	$\overline{X}_2$	X_2	X_1
1	0	1	0	$\overline{X}_2$	X_2	X_1
1	0	1	1	X_2	X_2	X_1
1	1	0	0	$\overline{X}_2$	X_1	X_2
1	1	0	1	X_2	X_1	X_2
1	1	1	0	X_2	X_1	X_2
1	1	1	1	$\overline{X}_2$	X_2	X_2

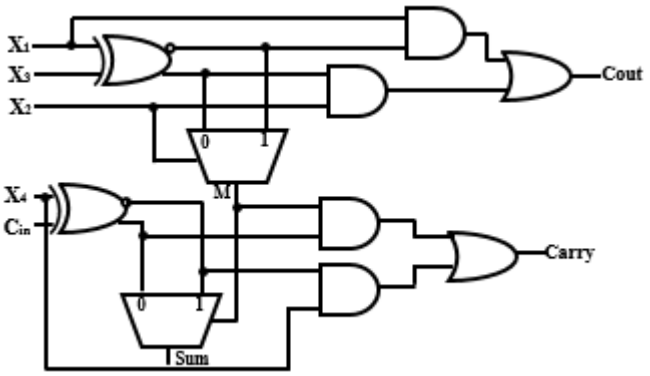


Fig.12: Gate level implementation of proposed 4:2 Compressor

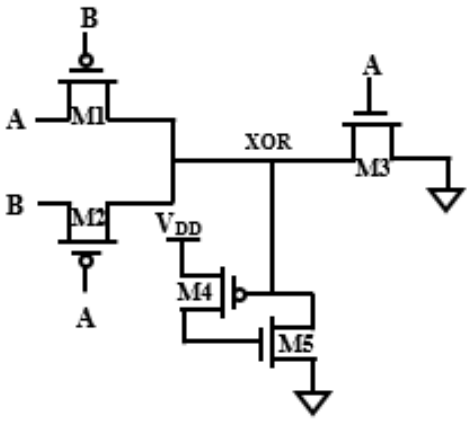


Fig.13:XOR module utilized in proposed design

The implementation of the proposed design at transistor level is depictedin Figure 14 given on the next page. The transmission gate based multiplexer design is used here. The most significant benefit of the transmission gate is reduced switching of capacitors due to reduced transistor count and route resistance.[32] The C_{in} signal is attached to the *SUM* generating network transistor gate. For full swing output of carry signal, an inverter is placed at the later stage of the circuit.

Simulation Results And Analysis

In this section, the assessment of the performance metrics of the proposed compressor circuit from multiple perspectives is carried out and compares them with prevailing designs found in the literature. The simulation of proposed 4:2 compressor circuit is carried out with Cadence Virtuoso tool in 45nm technology with supply voltage of 1V. Furthermore, for analyzing the robustness, corner analysis is carried out at different voltages along with temperature variations. This is followed by the execution of Monte Carlo analysis, which is very helpful for assessing systems that include uncertain components. The schematic diagram of proposed design is illustrated in Figure15.

While simulating the circuit, five inputs are taken X_1, X_2, X_3, X_4andC_{in} as displayed in Figure16. Three outputs are generated, namely, C_{out}, *Sum* and *Carry*. When all inputs are high, then C_{out},*Sum* and *Carry* are all at logic 1. For the input combination '01111', output *Sum* will be at low logic level, while C_{out} and *Carry* will be high. To achieve better assessment and evaluation all the earlier compressors have been entirely reconstructed and also adjusted to get better energy efficiency making use of 45nm technology in Cadence Virtuoso to figure out critical route latency, average power, energy dissipated in circuit in per switching operation i.e. power delay product (PDP), energy delay product (EDP) and equivalent output noise. The key role of calculating PDP is to demonstrate that power dissipation and speed are fundamentally traded off. Energy delay product plays pivotal role in determining tradeoff performance and power which can assist the designer in optimizing the circuit.

All these analysesare already reported in TableII. It can be derived from the Table II, that findings indicate that after doing comparison of proposed circuit with prevailing ones, the suggested 4:2 Compressor have shorter propagation delay. The reason behind this improvement is due to avoidance of frequently cascading of transmission gate through their drain contacts on critical path.

After doing analysis with former designs, the suggested structure exhibits lowest Power Delay Product (PDP) and Energy delay Product (EDP).To make the balance between energy economy and performance across many designs, it is noteworthy to calculate EDP. On the other hand, to get insightful visualization of the energy consumption and battery life of the circuit calculation of PDP is significant. The noise performance of any electronic gadget is to quantify according to the equivalent output noise. It is measurement of the noise present at output of the equipment. This allows the engineer to determine the amount of undesired signal (noise) being added to the intended signal.Lower equivalent output noise indicates better performance in terms of noise reduction. The graphical representation of all these analysis is displayed in fig.18 to 22.

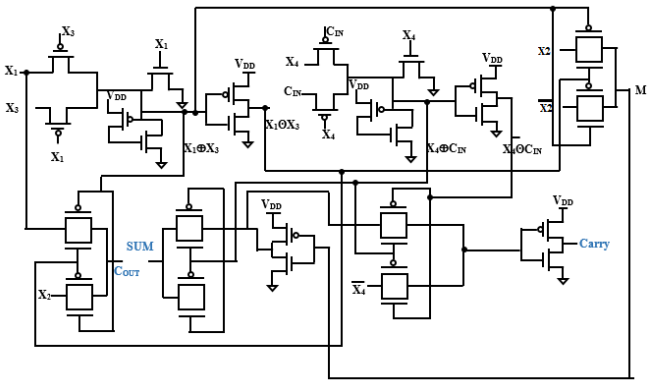


Fig.14: Transistor level implementation of proposed 4:2 Compressor

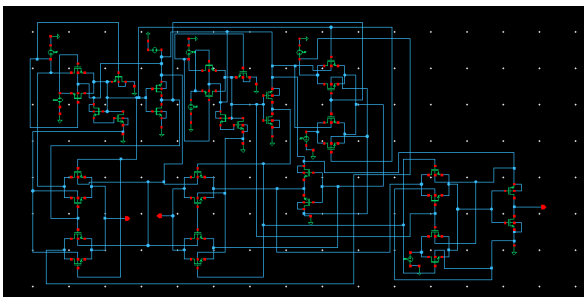


Fig.15: Schematic Diagram of suggested 4:2 Compressor

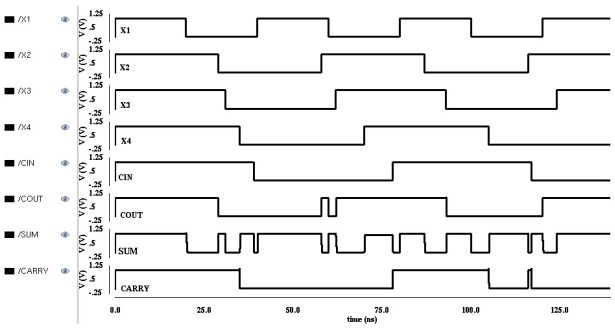


Fig.16: Simulation waveform of proposed 4:2 Compressor

Table. II: Performance Metrics of Proposed Design along with existing circuits

Temperature = 27° C						
Designs	**Transistor Count**	**Power(μw)**	**Delay(ns)**	**PDP(nJ)**	**EDP(nj*ns)**	**Equivalent Output Noise(V)**
Veeramachaneni [28]	66	55.238	42.042	23.22E-02	9.76E-02	6.65E-09
Pishvaie [29]	62	46.838	77.962	36.51E-02	28.46E-02	5.61E-13
Fathi [30]	70	67.014	49.939	33.46E-02	16.70E-02	3.09E-16
Ghasemzadeh[31]	43	41.667	39.983	16.65E-02	6.66E-02	1.78E-16
Proposed Design	34	38.699	20.206	7.82E-02	1.58E-02	1.77E-16

Table. III: Performance Parameters of Proposed Design w.r.t. Voltage & Temperature variation

Temperature = 27° C	Supply voltage variation			
Supply Voltage (V)	Power(µw)	Delay(ns)	PDP(nJ)	EDP(nj*ns)
0.8	38.683	20.204	7.81E-02	1.5779E-02
1	38.699	20.206	7.82E-02	1.5801E-02
1.2	38.71	20.21	7.82E-02	1.5804E-02
VDD = 1V		Temperature Variation		
-40° C	48.133	20.255	9.74E-02	1.97E-02
0° C	45.201	20.217	9.13E-02	1.84E-02
25° C	38.683	20.206	7.81E-02	1.57E-02
45° C	34.734	20.203	7.01E-02	1.41E-02

Performance features of the suggested design in conjunction with voltage and temperature variation is illustrated in Table III. For examination of voltage variation, three voltage levels are taken into consideration with temperature value of 27° C. The voltage values are 0.8V, 1V and 1.2V.For these three values, power consumption, delay, PDP and EDP of proposed circuits are calculated, which demonstrate the proposed circuit's ability to tolerate voltage change.For the temperature variation analysis, four temperature values are considered while maintaining Vdd at 1V. The power, delay, PDP, and EDP of the proposed design are calculated for the following temperatures: -40°C, 0°C, 25°C, and 45°C. The purpose of this investigation is to demonstrate the suggested designs' capacity to operate in various scenarios.

Corner Analysis

As we know that one of the most important CMOS transistor parameters is threshold voltage. The factors responsible for changing threshold voltage value are inconsistent doping and thin oxide thickness. In VLSI design, when an integrated circuit performance is analysed under various process, voltage and temperature (PVT) variation, it is referred as corner analysis. In this research, the circuit is simulated under various corners. Process corners express variability in the fabrication process parameters that include oxide thickness, levels of doping and size of interconnects. Slow-slow (SS), fast-fast (FF), slow-fast (SF), and fast-slow (FS) are examples of common corners, each of which represents an extreme in process variations. In each corner, first letter corresponds to NMOS transistor and later one represents PMOS transistor[31-33]

Performance of circuit is evaluated in Voltage corner while tested at various power supplies for nominal (NOM), high (HVT), and low (LVT) voltages. Behaviour of circuit under various supply voltages circumstances can be determined by these corners. Temperature Corners evaluate the operation of the circuit at various temperatures. Circuit timing and transistor properties are impacted by temperature changes. To verify the performance of architecture corner analysis is required. In both worst-case and best-case instances, it guarantees that the circuit satisfies timing, power, and functional requirements.[32] For yield prediction and optimization in manufacturing, it gives information of statistical distribution of circuit parameters across the corners. Proposed work corner analysis is stated in Table IV where TT stands for typical-typical case.

Table. IV: Corner Analysis of Proposed 4:2 Compressor

Temp = 27° C	Power variation (µw)				
Supply Voltage (V)	**FF**	**FS**	**SF**	**SS**	**TT**
0.8	56.18	41.20	33.86	24.01	38.68
1	56.19	41.22	33.88	24.03	38.69
1.2	56.21	41.23	33.89	24.04	38.71
Delay variation(ns)					
Supply Voltage (V)	**FF**	**FS**	**SF**	**SS**	**TT**
0.8	20.1361	20.7540	20.1450	20.382	20.204
1	20.1363	20.7545	20.1451	20.384	20.206
1.2	20.14	20.75	20.15	20.38	20.21

Monte Carlo Analysis

For integrated circuits to be robust, reliable, and manufacturable, Monte Carlo analysis is essential in VLSI design. It is vital for yield prediction, circuit performance validation against actual process fluctuations, and design margin optimization. Dimensions of CMOS and

threshold voltage get affected by process variations. These fluctuations can impact reliability of any device,so Gaussian distribution with a standard deviation of 3σ is employed. For this reason, calculating the worst-case latency requires the use of Monte Carlo simulation.[31-36] The suggested design is subjected to a 200-point Monte Carlo analysis in this investigation. Figure 17 shows the worst-case results from the Monte Carlo simulation, demonstrating that the compressor's operation[17-19] will satisfy acceptable performance standards after manufacturing. The worst-case latency of 18.9608ns is calculated using Monte Carlo simulation.

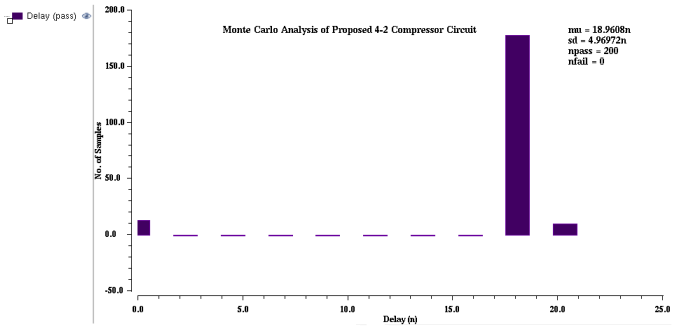


Fig.17: Monte Carlo Analysis of Proposed 4:2 Compressor for worst case delay

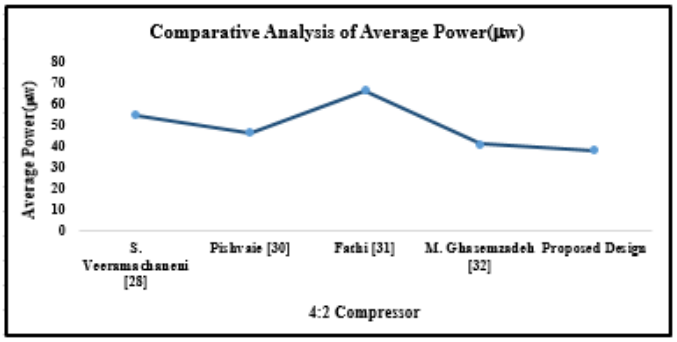


Fig.18: Average Power Analysis of 4:2 Compressor Proposed design with existing designs

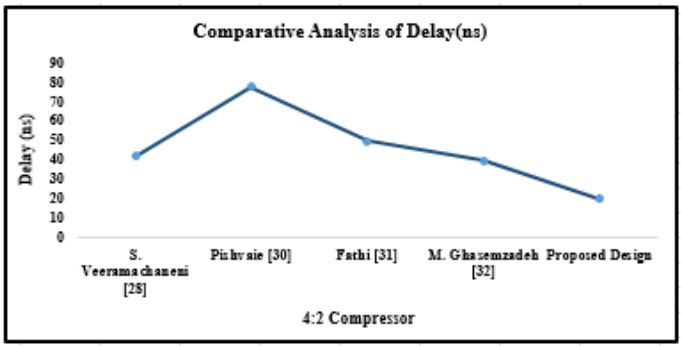


Fig.19: Delay Analysis of 4:2 Compressor Proposed design with existing architectures

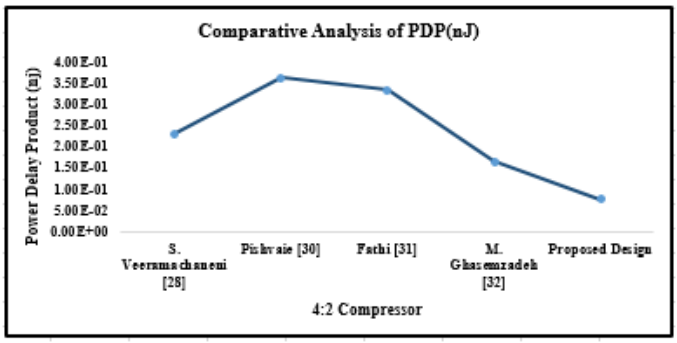


Fig.20: PDP Analysis of 4:2 Compressor Proposed design with existing architectures

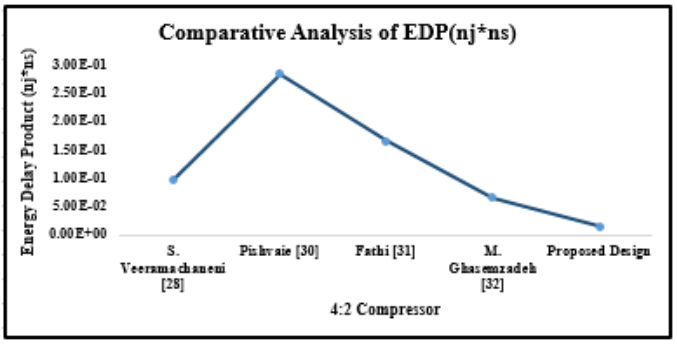


Fig.21: EDP Analysis of 4:2 Compressor Proposed design with existing architectures

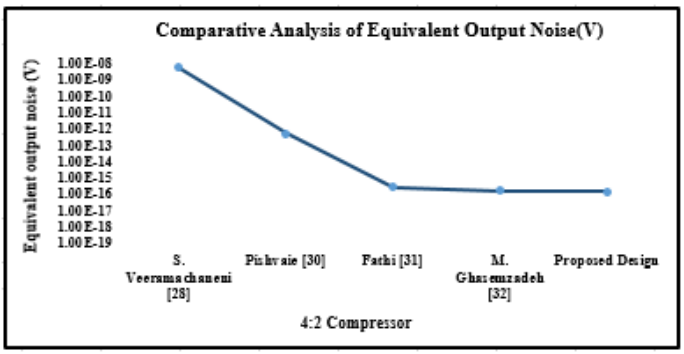


Fig.22: Analysis of equivalent output noise 4:2 Compressor Proposed design with previous designs

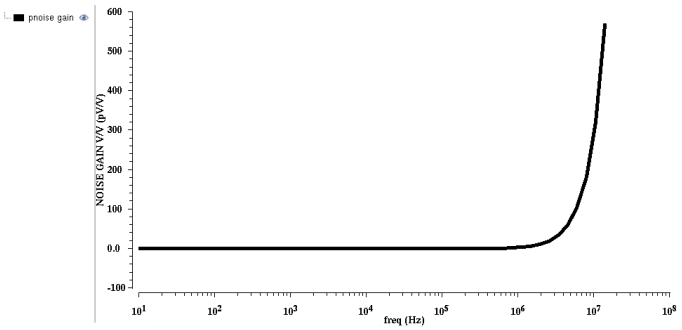


Fig.23: Noise Gain of proposed 4:2 Compressor circuit

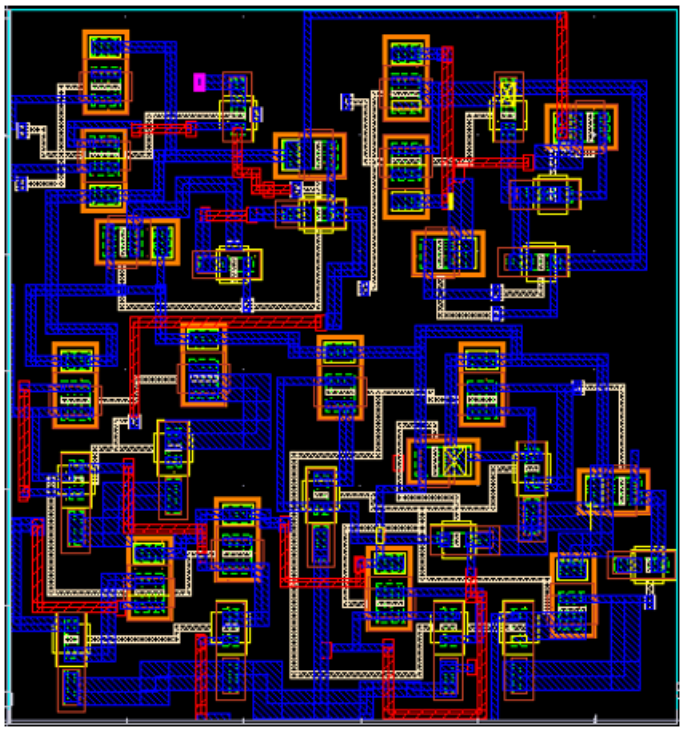


Fig.24: Layout of proposed 4:2 Compressor design

Layout

The suggested 4:2 compressor is designed by using Cadence Virtuoso tool in standard CMOS 45nm technology. Figure 24 depicts the layout of the suggested compressor part and was taken from Cadence Virtuoso. The usual λ-rules are used to estimate the area of the compressor. One poly and two metal layers are used. The recommended design's estimated area is (5.684×6.075) μm^2.

In this paper, noise gain is also calculated for the proposed design.Its significance is that it helps the circuit designer to reduce the amount of noise that affects integrity of signal by better understanding how noise spreads across the system. It is necessary to ensure that logic signals are interpreted correctly and that there are no erroneous transition. The graph of noise gain is depicted in Figure 23. At 14MHz obtained noise gain is 4.3591n. Noise gain is also important for detecting and reducing crosstalk among adjacent signal lines [37] - [40]. By keeping noise levels within constraint overall reliability of the circuit can be improved. To ensure the functionality of circuit across range of process corners, and yield improvement, calculation of noise gain is important.

Conclusion

This research present novel high-speed energy efficient robust 4:2 compressor based on novel equations. Also, these equations have been derived from novel truth table of the compressor. The key objective of this design is to minimize the area as well as increase the energy efficiency. The suggested design has a substantially lower transistor count, more compact design and noticeable higher energy efficiency. Hence, it can be further utilised in multiplier circuits, arithmetic and logic units, etc. After comparative analysis with previously constructed designs, it can be inferred that the proposed compressor has 49% lesser delay, 53% lower PDP and 76.27% lesser EDP than the other prevailing compressor designs. To prove that the recommended design can withstand the worst-case delay, Monte Carlo analysis is also performed.

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