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Review Article

A Review on Finfets from Device to Circuit

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ABSTRACT
FinFET is the multi-gate silicon transistor structure now a day's technology has changing in a brisk space people to achieve the better performance. Although several architectures has been developed in order to achieve the better performance like high speed, low power consumption etc. hence by taking these attributes in to consideration designed a novel Fin-FET technology in replacement of CMOS technology. This paper gives them a detailed art of Fin-FET technology and corresponding challenges, and future trends.

Keywords: Fin FET technology, MOSFET, leakage current.

Introduction

As the scaling down of the MOSFETs over the past five decades has enormously increased the transistor density and performance of ICs. However, continuing this trend in the nano-meter regime is very challenging due to sub threshold leakage. Due to very narrow channel lengths in deep scaled MOSFETs the drain potential begins to impacts the electrostatics of the channel and consequently loses the control over the channel. Hence which leads to increase the Ioff between drain and source. As long as thinning of the gate oxide which fundamentally limits the detraction of gate leakage and gate induced drain leakage(GDIL). on the other hand multiple gate filed effect transistors are the alternate of the MOSFETs. Earlier the MOSFETS are built by planner MOSFETs on bulk in silicon wafers(bulk MOSFETs). Fully depleted MOSFETs are avoid the extra leakage paths from the MOSFETs and SOIMOSFETS are eventually avoids the leakage path from source by getting rid from the extra substrate respectively. figure 2 and 3 depicts the structure of planner MOSFET and Fin FET respectively.

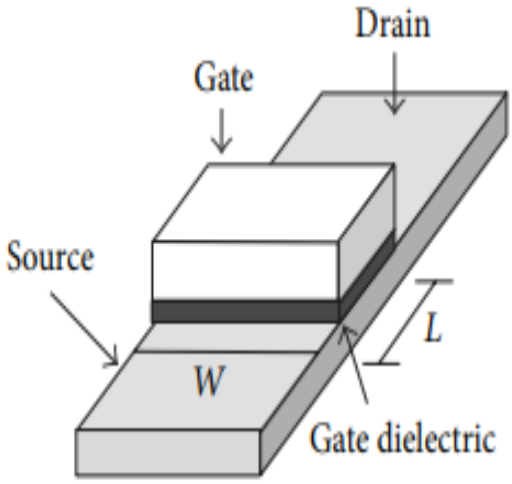

Fig.1: Structure of planner MOSFET.

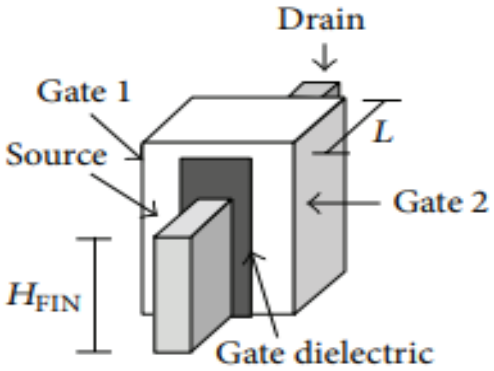

Fig.2: Structure of FinFET.

Classification of FinFET Structures

Depending upon the architectural orientation Fin FETs has been broadly classified in to two types such as independent gate fin FET and short gate Fin- FET. the basic difference between IGFET and SG FET can be given in the below section. the basic architecture of the SG Fin FET and IG fin FET are shown by figure 3 and 4 respectively.

Table: 1

IGFET	SG FET
It is having four terminal	It is having three terminals
Gates are isolated with each other	Gates are shorted to gather
It is having less current due to its isolated nature.	It is having higher ON current due to its shortage of two gates with each other
It offers the more flexibility	It offers the less flexibility

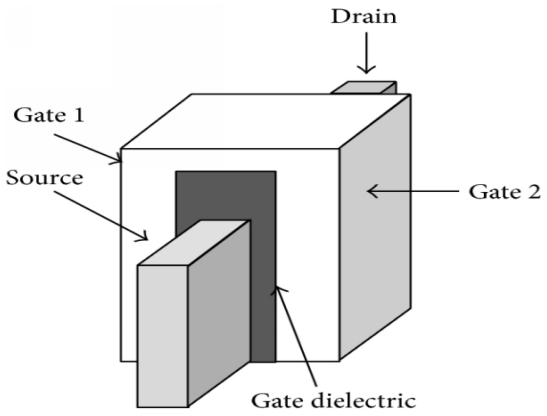

Fig.3: structure of SGF

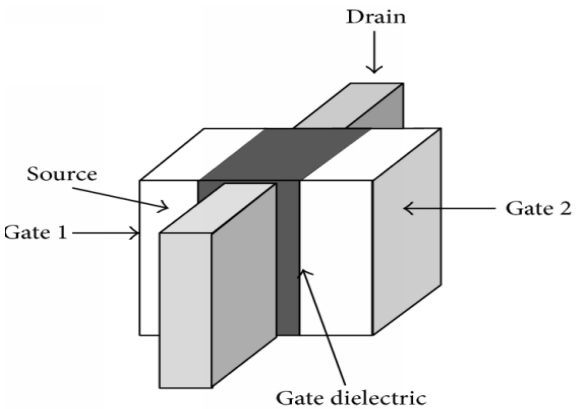

Fig.4: structure of IGF.

Challenging Parameter In Manufacturing Process Of Finfets

The moment we are shifting from the planar MOSFET to Fin FET technology we are going to face several vulnerabilities such as shape of the FIN, parasitic capacitance, doping concentration of Fin-FETs, Orientation of FINs, reliability of FINs.

Shape of the FIN

The functionality of the Finfet is Intel microprocessor 22nm technology, This could be place at 8 digress from vertical to the microprocessor. Due to its very less in size it causes the lack of immunity for causing the short channel effects and it is mainly responsible for the gate length scaling.

Parasitic capacitance

As the compared to the planar CMOS technology it will causes the more parasitics in the device. The variation in the FIN helps to reduce the parasitics of the capacitance, and the analytical model of the parasitics can be done using the conformal mapping technique.

Doping consecration of FIN FETs

An un doped channel is preferably increases the resistance of the device, this ultimately damages the shape of the device however to get better control over the leakage power, then high dopant source and drain regions are required.

Conclusion

The recent trends in Fin Fet technology helps to enhance the system performance and this paper gives a critical review of major challenges and issues while facing the Fin-FET technology.

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