

Performance Evaluation of Mesh, Spidergon, and Mesh of Spidergon (MoS) Topologies in Network-on-Chip (NoC) Architectures <u>Latin Comparator Comparator</u> Comparation
Latin Comparator in Marsh Low Offset Voltages Id mesh of spidergon (mos) repologies in

Sravani S¹, Deepak Ch¹

¹School of Electronics Engineering, VIT-AP University, Amaravati, Andhra Pradesh, India.

KEYWORDS: Latency Latency
Mesh-of-Spidergon topology meen en oproor g
Throughput Network-on-Chip YWORDS:

KEYWORDS: AND THE SERVICE OF SERVICE

Abstract

Network-on-chip (NoC) is essential for efficient data transmission in system-on-chip resolution, and resolution, and resolution integrated circuits (ICs) become increasingly (SoC) architectures, particularly as modern integrated circuits (ICs) become increasingly (see) distincts the performance, the choice of topology significantly impacts the performance, throughput, complexed the choice of topology algumeantly impacts the performance, throughput,
and latency of NoC designs. Traditional topologies, such as Mesh and Spidergon, offer and accomplex the compared mathematic perspitely compared and operations on a non-
unique benefits and limitations. This study introduces a new topology, Mesh of Spidergon matched and the interaction of the competitivity advantages of Mesh with the global routing (MoS), which integrates the local connectivity advantages of Mesh with the global routing efficiency of Spidergon. We evaluate the network diameter and average distance of the Mesh, Spidergon, and MoS topologies. The assessment focuses on throughput and latency using Transmission Control Protocol (TCP) applications, specifically analyzing File Transfer Protocol (FTP) and Constant Bit Rate (CBR) traffic patterns under varying link failure rates of 5%, 10%, and 15%. Results show that the MoS topology achieves a throughput of 26.96 Mbps, surpassing Mesh's 12.68 Mbps and Spidergon's 23.51 Mbps using FTP protocol. For the CBR protocol, MoS reaches 34 Mbps, compared to 12.68 Mbps for Mesh and 25.23 Mbps for Spidergon, while maintaining comparable latency to Spidergon at 2.37 ms, whereas Mesh exhibits higher latency with 3.78 ms. Furthermore, MoS demonstrates enhanced resilience under link failures. Overall, the MoS topology significantly improves NoC performance, **shikkumarbiswas13@gmail.com** merging the strengths of existing topologies and offering a viable solution for future SoC designs. **How to cite this article: Mukti IZ, Khan ER, Biswas KK**. 1.8-V Low Power, High-Res-

Author e-mail:deepakchenu@gmail.com, sravani.sravanam@gmail.com
——————————————————— olution, High-Speed Comparator $\mathcal{L}_{\mathcal{A}}$ is the comparator $\mathcal{L}_{\mathcal{A}}$ of $\mathcal{L}_{\mathcal{A}}$

Journal of VLSI circuits and systems, , ISSN 2582-1458 **19**

How to cite this article: Sravani S, Deepak Ch. Performance Evaluation of Mesh, Spidergon, and Mesh of Spidergon (MoS) Topologies in Network-on-Chip (NoC) Architectures, Journal of VLSI Circuits and System Vol. 6, No. 2, 2024 (pp. 130-140).

https://doi.org/10.31838/jvcs/06.02.15

ARTICLE HISTORY:

INTRODUCTION signals, basically an input analog signal with a reference signal,

IntroductIon

Received : 15.10.2024
Revised : 20.11.2024 $: 20.11.2024$ Accepted : 26.12.2024

In the world of modern microelectronics, rapid technological advancements have led to the emergence of intricate complexities and escalating demands in integrated circuit designs. As traditional monolithic approaches encounter growing obstacles related to throughput, latency, and performance, a transforming paradigm shift has materialized in the form of Networkon-Chip (NoC) architectures. NoC signifies a revolutionary strategy for interconnecting the diverse components residing within a chip, presenting an agile and efficient solution for providing evolving requirements of complex systems-on-chip (SoCs). NoC is meticulously engineered to furnish a scalable and proficient framework, thereby facilitating the seamless exchange of data and communication among various processing elements or intellectual property (IP) cores, all amalgamated onto

a solitary semiconductor chip. One conspicuous facet of a contact converter with a structure constraint and the converter of the NoC's significance manifests in its profound influence on the delineation of on-chip topologies. These topologies meticulously direct the intricate interconnections among various chip components. The integration of Transmission Control Protocol (TCP)^[1] connections within this on-chip communication framework warrants special consideration. TCP, serving as a ubiquitous transport layer protocol in the realm of computer networking, is distinguished by its commitment to reliability and its connection-oriented nature. It steadfastly ensures the orderly and error-free transmission of data between two endpoints ensconced within a network. When integrating the TCP connections within on-chip topologies, specific crucial aspects must be considered to ensure proper functionality and performance. It is a transport protocol extensively used in computer networking to guarantee reliable, ordered, and error-free data delivery between

applications running on hosts connected to the Internet. The number of hops required for data transmission Implemented in the correct order and check-sums to used in the modelling and simulation of three corrections of the correct order and check-sums to used in the modelling and simulation of three corrections of the correctio network congestion. This mechanism ensures efficient conclusion. loss and network performance degradation caused by
 Congrection Applications that require reliable data data connection is used to transfer files. Constant Bit rate. This traffic pattern is commonly employed in AQ by transmitting packets at a constant rate, regardless of a deterministic trainc pattern, which means that the size
and arrival time of each packet can be anticipated in advance. It is frequently utilized in network simulations to assess the performance of various network protocols and architectures under stable traffic conditions. The existing literature predominantly focuses on evaluating the performance of individual NoC topologies like Mesh, Torus, and Fat Tree, among others. While these studies provide valuable insights into throughput and latency, they often overlook energy fault tolerance. Additionally, there is a lack of exploration into hybrid topologies that can combine the strengths of different designs to achieve better overall performance. This paper addresses these gaps by proposing a novel hybrid topology called Mesh of Spidergon (MoS). The MoS topology integrates the Mesh topology for local connections and the Spidergon topology for global connections, aiming to enhance both performance and throughput. By leveraging the strengths of both topologies, MoS is designed to reduce congestion. Applications that require reliable data gain, transfer, such as email, file transfer, and web browsing, widely use TCP. It is also utilized as the underlying transport protocol for other protocols like FTP and CBR. **ARTICLE HISTORY:** used network protocol for transferring files between source and destination in a network. It sends packets from the source to the sink in a specified path. It uses two TCP connections, one for control and another for sending commands and receiving responses, while the It is a connection-oriented protocol, which establishes a connection between two hosts before exchanging data. It segments the data and transmits it across the network using a sliding window algorithm for flow control to prevent data overload at the receiver's end. The protocol also uses sequence numbers to ensure guarantee data is transmitted without errors. It offers a congestion control mechanism that monitors network conditions and adjusts the transmission rate to avoid utilization of network resources and prevents packet FTP, which stands for File Transfer Protocol, [1] is a widely data transfer. The control connection is responsible for Rate (CBR)^[1] is a traffic type used in computer networks to produce a continuous flow of data at a constant applications that require steady data transmissions, such as video or audio streaming, to provide smooth playback without interruptions. CBR traffic is generated the network's state or available bandwidth. This creates a deterministic traffic pattern, which means that the size

ta. It segments the data and transmits it across the work of various authors. Existing topologies, proposed to
Intervork using a sliding window algorithm for flow topologies and metrics of topologies are discussed in Example the Comparator Computer (NS 2.25). By then programming is mission rate to avoid and CBR traffic patterns. Finally, Section 6 draws the the number of hops required for data transmission, thereby improving throughput and reducing latency. This paper is organized as follows. Section 2 gives the related topologies and metrics of topologies are discussed in Network simulator (NS-2.35), Python programming is used in the modelling and simulation of three topologies using the Dijkistras algorithm. Section 5 describes the three topologies results by using TCP Protocols with FTP conclusion.

Related Work

and web browsing. Tetala Neel Kamala et al. conducted an evaluation of as the underlying different topologies^[2] in NoCand found that the Mesh $\frac{1}{\sqrt{1-\frac{1$ comparator for a highly linear 4-bit Flash A/D Converter (ADC). The outlined design Butterfly Fat Tree topologies in terms of node throughput C can operator on a non-various offset voltage was elected w rring files between analysis. Better throughput and performance consistency. k. It sends packets lincreased complexity and area utilization compared ecified path. It uses to Mesh. In their proposal, B Joshi et al., suggested \overline{r} and another for that Hypercube and Torus topologies^[1] with 16 cores of and another for and outperformed Fat Tree, Mesh, Mesh of Tree (MOT), King $\frac{1}{2}$ in is responsible for the comparator in the comparator is 12.3 $\frac{1}{2}$. esponses, while the \blacksquare Mesh, M Mesh, Ring, and Star topologies. Additionally, data at a constant other topologies evaluated. According to the proposal by data transmissions, an engapat performance compared to the mesn, emesn,
to provide smooth and Fat Tree topologies. JenitaPriya et al. proposed that to provide smooth and racince topologies. Jerman rija et al. proposed in the comparative Implemented in the comparative Implemented in the comparative Implemented in the comparative Implemented in the comparative Implement traffic is generated $\frac{R}{L}$ Ring topology^[4] occupies less area utilization than Mesh when packet size was varied. However, in terms of delay, CBR traffic outperformed FTP traffic. As the queue size increased, FTP demonstrated better throughput results than CBR traffic, but both traffic types experienced higher delays. Panem et al. proposed that using the XY routing algorithm^[6] for 2D and 3D Mesh topologies yields better throughput and latency results. The FTP traffic pattern obtains better throughput than the CBR traffic pattern. According to KusumKardam et al., research, the Torus topology^[7] yielded superior throughput results compared to the Mesh topology. Additionally, when using the TCP protocol for the FTP traffic pattern, the results were found to be more favorable than when using the User Datagram Protocol (UDP) for the CBR traffic pattern. K. Balamurugan et al., summarize NoC types and associated tools.^[8] The Author suggests the use of NS2 and NS3 for NoC routing and performance evaluation, including speed and power consumption analysis. the paper demonstrated that a 64-core MOT topology produced superior throughput results compared to the A Q Ansari et al., the Torus topology^[3] exhibits superior throughput performance compared to the Mesh, Cmesh, and Torus topologies. CharnarurPanem et al. proposed that on the performance of Mesh topology $[5]$ at various sizes, FTP achieved superior throughput results than CBR

TOPOLOGIES was increased to four times of the nominal \mathbf{C}

The topology^[9] significantly influences the performance, me teperegy engineesing inneeneed the performance, on Chip (NoC). To ensure optimal system design, communication latency, bandwidth, fault tolerance, and throughput when designing the NoC topology. $[10]$ Therefore, a well-designed NoC topology plays a critical role in determining the overall system's effectiveness. The design methodology for a topology is shown in Figure 1. In Network-on-Chip (NoC) design, Mesh topology^[11] is a widely used network architecture as shown in Figure 2. It involves connecting processing nodes in a grid-like pattern, where each node is linked to its neighboringnodes directly. Depending on the $\overline{\text{complexity}}$ of the network, the Mesh topology can be either two-dimensional (2D) or three-dimensional (3D). In a 2D Mesh topology, each node is connected to its four adjacent nodes, whereas in a 3D Mesh topology, each node is connected to its six adjacent nodes. The direct connection between nodes results in lowlatency communication and high bandwidth. It provides flexibility in network design, as nodes can be added or removed with ease without affecting the overall network performance. Spidergon topology^[12] is utilized in the design of Network-on-Chip (NoC) as shown in v_{c} and v_{c} and v_{c} power performance of the theorem performance of Comparator. The comparator design given in this paper is it is essential to carefully consider factors like Figure 3.

Fig. 1: Designing methodology of a topology.

Fig. 2: A 30 node Mesh topology.

It is based on a Mesh network that connects processing nodes using a combination of vertical and horizontal links. The nodes in the Spidergon topology are organized in a grid-like fashion, similar to a Mesh topology. The key difference between Spidergon and traditional Mesh topologies lies in adding diagonal links. These links create a spider-like pattern, giving the topology its name. Using diagonal links improves the connectivity of the network and reduces communication latency between nodes. It also provides benefits such as increased bandwidth, reduced latency, and improved fault tolerance.

Fig. 3: A 32 node Spidergon topology.

Mesh topology for local connections and the Spidergon topology for global connections. In this hybrid topology, Mesh and Spidergon are two topologies commonly used in network-on-chip (NoC) design. The Mesh topology is a well-known topology in which nodes are arranged in a regular two-dimensional grid, and each node is directly connected to its four adjacent nodes as shown in Figure 4. In contrast, the Spidergon topology is a newer approach that provides certain advantages over the Mesh topology. Hence Mesh is integrated with Spidergon topology. This integration entails using the

nodes are placed in a two-dimensional Mesh but are $\qquad \bullet$ A lower average network diameter generally the number of hops necessary to reach the destination
node. This integration of Mesh and Spidergon topologies • Average Network Diameter of Mesh is 3.6 mn Comparator The Integration of Integration of the precision topicols of the Spidergon is 4.61 mm and MoS is 5 i
Comparator Comparator Comparator (Comparator Comparator Comparator Comparator Comparator Comparator Comparator
 nodes are placed in a two-dimensional Mesh but are also linked to other nodes in the Spidergon hierarchy, allowing for a more efficient routing system and reducing node. This integration of Mesh and Spidergon topologies energy efficiency.

Fig. 4: A 32 node MoS topology.

been implemented, and the area of the comparator is 12.3 × 15.75 . The reare key performance metrics that play a pivotal role in In the realm of Network-on-Chip (NoC) topologies, there assessing network efficiency and scalability. Let's discuss these metrics and delve into the values attributed to the provided topologies:

1.1 **Network Diameter (N.D)**

- for the utmost number of hops or links between • Network diameter serves as a crucial element any two nodes (or routers) within the network.
- **IntroductIon** It serves as an indicator of the worst-case latency experienced during communication between any pair of nodes in the network.
- A smaller network diameter is highly desirable, as it signifies reduced latency for communication. For the respective topologies:
- Network Diameter of Mesh is 9 mm, Spidergon is 8 mm and MoS is 5 mm.

The notural diameter is calculated in our constigue ℓ The network diameter is calculated using equation 1.

 $D[neighbor] = min (D[neighbor], D[current])$ $+W$ (current, neighbor)) (1)

Where D is Distance W is weight.

$\mathbf{1}_{\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{2}}\mathbf{1}_{\mathbf{3}}\mathbf{1}_{\mathbf{3}}\mathbf{1}_{\mathbf{4}}\mathbf{1}_{\mathbf{5}}\mathbf{1}_{\mathbf{6}}\mathbf{1}_{\mathbf{7}}\mathbf{1}_{\mathbf{8}}\mathbf{1}_{\mathbf{9}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{1}}\mathbf{1}_{\mathbf{$ **3.2 Average Network Diameter (A.N.D)**

• Average network diameter calculates the mean distance (in hops or links) between all pairs of nodes situated within the network.

- signals superior communication efficiency. For the provided topologies:
- Average Network Diameter of Mesh is 3.6 mm, Spidergon is 4.61 mm and MoS is 5 mm.

 $\begin{array}{c}\n\text{Equation:} \\
\text{topology emerges as having the smallest value, implying} \\
\text{the smallest value, implying}\n\end{array}$ $\begin{array}{l} \hline \text{H} \rightarrow \text{H} \text{I} \end{array}$ the selection of a NoC topology hinges upon the precise **T** \bigcap **f** The Periodic University of our application: Examining the average network diameter, the Mesh that it is potentially more efficient, on average, for communication between pairs of nodes. In summation,

- as the favored choice due to its petite network \overrightarrow{a} resolution, and rapid speed. The diameter. • If minimizing latency for all-to-all communication is of paramount importance, MoS presents itself
- technology and runs 4.2 samples per second at nominal voltage. It is a custom-made $\sqrt{2\pi}$ • Should the emphasis be on average-case $\sqrt{\frac{1}{\sqrt{3}}}$ communication efficiency, the Mesh topology $\sqrt{}$ may be the preferred option, given its lower average network diameter. \leftrightarrow 28 \leftrightarrow 27 \leftrightarrow 27

Table 1 shows the network diameter, number of routers, pology. The comparator is and number of links calculated for three topologies.

Ly topologies, there
Invisinizatel role in in this paper, Mesh, Spidergon, and MoS topologies es attributed to the with link failures the topologies were evaluated. The importance of NS-2.35 in the design of various performance of various topologies. So the metrics can $\frac{1}{2}$ be evolved by using Dijkistra's algorithm^[13] in Python. a crucial element These are described in the design setup as follows. are evaluated under throughput and latency and also topologies and metrics plays a vital role in assessing the

Table 1: Network diameter calculation in three topologies

between implemented. In this comparator, super low thresholder, super low thresholder, super low thresholder, **DESIGN SETUP EXISTENTION**

 $NS-2.35$ ^[14] is a well-known network simulator that is open-source and mainly used for simulating wireless and wired networks, as well as Network-on-Chip (NoC). and three metholds, as non as necessary on emp (need).
This simulator is based on discrete event simulation and operates on a packet-by-packet basis, enabling and operates on a packet by packet basis, chapting
network designers and researchers to evaluate network reducing a better will be a better the conductor in a simulated environment. to have a generation and processes in a simulated simulation, The proposed topology MoSwas designed in the NS-2.35 large proposed to potagy missing all the MOSFETS in the MOSFET simulator. NS-2.35 is a flexible simulator used to model saturation. The line is a result of most contracted the performance and behavior of various NoC topologies novel topologies. The design of these topologies is accomplished using TCL scripts, which allow for the specification of network nodes, links, routing protocols **relAted work** is executed, AWK scripts are employed to analyze the results, extracting key performance metrics such as throughput and latency as shown in Figure 1. Finally, the evaluated results are saved for further analysis, providing valuable insights into the NoCs performance $\mathsf{U}\mathsf{a}\mathsf{U}\mathsf{b}\mathsf{I}\mathsf{b}\mathsf{I}$ (such as TCP), and traffic patterns. Once the simulation evaluation.

Python with NetworkX is a versatile and powerful set of tools for working with networking graphs. Different scenarios were considered in three different topologies and comparative analysis was done in them.In Python import networkx^[15] as nx statement serves to bring the NetworkX library into the codebase and assign it as not have gone the designer and the design of the theory of the new state of the design of the new state of the functions and and the shot and conditions of a comparator was changed and classes from NetworkX more succinctly. realized in a 22 nm FDS of the 22 nm FDS of the 0.8V supply.

NetworkX is a robust library designed for the generation, examination, and depiction of intricate networks, often represented as graphs. This practice enhances code readability and ease of use when working with network-related operations and matplotlib. pyplot is a widely used Python module for crafting diverse visualizations such as charts, plots, and graphs. With its capabilities, it allows users to create clear and insightful representations of nodes, edges, and their interconnections within a network. The nodes and **ArchItecture of compArAtor** Dijkstra's algorithm stands as a widely adopted method for determining the shortest paths within a weighted graph. The procedural steps of this algorithm can be as follows: Initialization: Assign the source node distance as zero and the remaining node distances as infinity. Establish a priority queue (or min-heap) to manage the provisional distances emercing. Explore reignbors. from the priority queue. For each neighboring node: Compute the tentative distance from the starting node to the neighbor through the current node. If this calculated distance is smaller than the presently recorded distance for the neighbor, update the distance. Termination: Conclude the algorithm when all nodes have been visited or the destination node edges are created as topology as shown in Figure 5. provisional distances efficiently. Explore Neighbors: has been reached. Outcome: The ultimate recorded distance values convey the shortest distances from the initial node to every other node in the graph. Utilizing Dijkstra's algorithm facilitates the computation of the shortest path. Subsequently, by utilizing this the metrics such as average network distance and network diameter can be derived.

Fig. 5: Dijkstra's algorithm in a topology's flow chart.

Results

This section introduces the concepts of throughput[2] and latency in NoC [16] topologies performance along with link failures at 5%, 10% and 15%.

5.1 Throughput

source to destination is throughput. A simplified formula for computing throughput is expressed as equation 2. The time taken to transfer packets efficiently from

Throughput Datapackets successfully transmitted ⁼ Time taken for transmission **(2)**

to have a lower throughput than MoS and Spidergon This equation essentially evaluates the volume of data successfully transmitted within a specified time interval. It's imperative to acknowledge that in NoC systems, throughput may fluctuate based on parameters such as packet size, and network topology. Consequently, a comprehensive analysis of NoC throughput performance necessitates the holistic consideration of these factors. As shown in figure 6, the results of throughput in TCP using the FTP traffic pattern in three topologies. The MoS topology was found to have higher throughput than the other two topologies. Spidergon topology was found next to MoS topology, and Mesh topology seemed topologies.

5.2 Latency

The time delay experienced by the data packets to be transferred from source to destination is known as latency.

Latency = (Et- St), if packets are received at the node
$$
(r^2 = 0, \text{ then } r^2 = 0
$$

\n (3)

ISHRAT AND AND ARRESTS AND MUKHAM2. The Much packets are mode at the source node. If packets are received at the destination node 'r', then the latency is calculated as $\frac{1}{2}$ ²⁵⁰⁰⁰ time S_t. Conversely, if no packets are received at 'r', the latency is considered as zero which was shown in \mathbb{E} $\mathbb{E$ equation 3. The topologies with nodes, and links are set $\frac{1}{2}$ with bandwidth. Then, the connections between traffic $\begin{bmatrix} 1 & 1 \end{bmatrix}$ $\begin{bmatrix}$ $\overline{\text{a}$ spide of the outline of the outlined design $\overline{\text{a}}$ and FTP traffic patterns are established. All these are written in TCL scripts. Network Distance $\frac{0}{0}$ $\frac{1}{500}$ $\frac{1}{1000}$ $\frac{1}{1500}$ $\frac{2000}{2000}$ $\frac{2500}{2500}$ was calculated with Dijkstra's algorithm using Python. **The offset voltage, we follow the offset voltage, we followed a decent voltage, we follow the packet size (Kbytes)** in NS-2.35 and analyzing the topologies using Dijkstra's are are shown. Then is, but a shown in the result of the research and NetworkX can streamline this analysis, providing a the difference between the arrival time E_t and the start Received xxxxxxxxxxxx Throughput and latency are key performance metrics for network topologies. By simulating different scenarios **DOI:** distance affects these metrics. Using tools like Python In this equation, the latency is computed as the time elapsed between the last packet being received at the destination node and the transmission of the first packet algorithm can gain insights into how means network clear picture of network topology performance.

ITHE research is carried out by considering the bandwidth lowe **How to 50 Mbps. The propagation time is 10 milliseconds.** The state of the sta $\begin{array}{|c|c|c|c|c|}\hline \text{N} & \text{CDF} \end{array}$ and $\begin{array}{|c|c|c|c|c|}\hline \text{N} & \text{CDF} \end{array}$ and $\begin{array}{|c|c|c|c|c|}\hline \text{N} & \text{CDF} \end{array}$ and $\begin{array}{|c|c|c|c|c|}\hline \text{N} & \text{CDF} \end{array}$ observed in three topologies are shown in Table 2. Mesh $\frac{35}{20}$ topology throughput using FTP traffic scenario diminishes as compared to Spidergon and MoS topologies. With 1187.698 Kbytes and MoS topology at 1627.577 Kbytes. However, MoS topology outclasses Mesh and Spidergon topology as packet size increases. The MoS topology gives a higher throughput than the remaining two topologies. MoS topology gives a higher throughput of 112.57% than Mesh topology and throughput of 14.64% than Spidergon topology at 2048 Kbytes was observed using the FTP traffic scenario. Mesh topology produces comparable results using CBR traffic patterns. It generates similar results by utilizing FTP and CBR traffic patterns. Spidergon and MoStopologies generate nearly equivalent results up to 16000 bytes of packet size. However, from 32 Kbytes to 2048 Kbytes, MoS topology throughput increased quite gradually than Spidergon and Mesh topologies. MoS topology gives a higher throughput of 168.08% than Mesh topology and throughput of34.75% than Spidergon topology at 2048 Kbytes was observed as packet size increases from 1000 bytes to 2048Kbytes improved results, Spidergon topology was observed at

5.2 Latency **Example 28 Tanach ARTICLE WAS SEARCH ARTIC** with using the FTP traffic scenario. Overall, three topologies utilizing both FTP and CBR patterns are demonstrated.

transferred from source to destination is known as a all Especially when we observe Spidergon and MoS topologies by using FTP and CBR patterns, Spidergon and interncy. y = (Et- St), if packets arereceived (3) MoS topologies are observed with low throughput using
the pode 'r' = 0, therwise (3) CBR up to 16000 bytes. But later these topologies yield at the hode $1 - 0$, therwise
higher throughput results using CBR traffic patterns.
ation, the latency is computed as the time Especially when we observe Spidergon and MoS MoS topologies are observed with low throughput using

approximating the circuits.
The code of the circuits. The code of the circuits of the Circuits. The original to 250 traffic **The designed comparator has a unity comparator has a unity of 72 at 12 at 12** the gives us a considerable gives us a considerable state of authority. The different scenarios values of authori

ow means network and shown in figure 6, the results of throughput in TCP g tools like Python using the FTP traffic pattern in three topologies. The rformance. **Each inclust the other two topologies. Spidergon topology was found** MoS topology was found to have higher throughput than next to MoS topology, and Mesh topology seemed to have lower throughput than MoS and Spidergon topologies.

Fig. 7: latency in TCP using FTP traffic pattern in
three tenalsgies structure, the gate capacitance tends to show a higher capacitance tends to show a higher capacitance tends to **three topologies.**

Figure 7 depicts the graph with the latency of all three topologies using an FTP traffic pattern. Mesh topology has been uncovered to have a higher latency than MoS and Spidergon topologies. The results of Spidergon and MoS topologies are comparable. In addition, MoS topology was reported to have lower latency than Spidergon $topology.$ topology.

The graph in figure 8 depicts the throughput of all three topologies using the CBR traffic pattern.^[8]

Mesh topology throughput spiked once, then decreased precipitously. MoS and Spidergon topologies have comparable throughput, and MoS topology generated even better results.

based comparator. The comparator of the design of the Fig. 8: Throughput in TCP using CBR traffic pattern in **Fig. 8 three topologies.**

realized in a 22nm FDSO process with a 22nm FDSO process with a 0.8V supply. The 0.8V supply. The 0.8V supply. The latency of all three topologies using the CBR traffic pattern in the TCP protocol is shown in figure 9. Mesh topology outperforms MoS and Spidergon topologies in terms of latency. However, at 2048 Kbytes of packet size, all topologies generate similar results. Figure 9 shows the latency in TCP using CBR traffic pattern. The MoS

topology's higher throughput can be efficient to transmit more packets per unit of time. However, the higher latency indicates that these packets are taking longer to reach their destination. As bandwidth increases, the MoS topology maintains high throughput, but latency
... decreases. This suggests that with more available bandwidth, the network can handle the higher data rate more efficiently, reducing delays Mesh topology offers redundancy but at the cost of higher latency and lower throughput.

Fig. 9: Latency in TCP using CBR traffic pattern.

Packet size (P.S)	Mesh FTP	Spidergon FTP	MoS FTP	Mesh CBR	Spidergon CBR	MoS CBR
(Kbytes)	(Kbps)	(Kbps)	(Kbps)	(Kbps)	(Kbps)	(Kbps)
1	457.023	1187.698	1627.577	457.023	1047.864	1048.033
2	886.170	2303.485	3157.397	886.170	2053.462	2054.123
4	1716.463	4462.256	6062.397	1716.463	4059.807	4062.419
8	3273.218	8509.838	11374.645	3273.218	8053.205	8063.543
16	4491.351	14832.306	19974.757	4491.351	15251.714	16004.469
32	7833.460	23605.968	33157.419	7833.460	26639.307	31645.385
64	7456.644	29425.636	35243.652	7456.644	36971.365	39748.254
128	11595.927	30693.722	37083.725	11595.927	41797.346	44101.528
256	10143.357	17852.719	23450.079	10143.357	33904.563	40381.478
512	8432.360	21734.216	26791.258	8432.360	30496.227	38635.123
1024	10006.977	18012.558	29454.562	10006.977	26876.366	33529.541
2048	12987.680	24081.222	27608.379	12987.680	25838.689	34817.735

Table 2: Throughput using TCP protocol with FTP and CBR traffic scenario in three topologies

as latency increased as packet size spiked in Table 3. packet size, the latency increases in all three topologies in all Kbytes of packet size than MoS and Mesh topologies by of packet size, MoS topology had lower latency than topology was higher than MoS topology with 59% and Spidergon topology with 14% than MoS topology at 2048 Kbytes. The latency of the three topologies was observed to be comparable up to 16 Kbytes of packet size using the CBR traffic pattern. However, for Spidergon and MoS topologies, latency increases. After 512 Kbytes of packet size is applied, the latency of the Mesh topology also increases. However, at 2048 Kbytes, the MoS topology's latency drops to 3.764601ms. The latency of Mesh topology was higher than MoS topology with 0.53% and Spidergon topology with 1.06% than MoS topology at 2048 Kbytes. Overall, the latency is higher for all three CBR traffic pattern topologies. Table 4 depicts the throughput of three topologies with 5%, 10%, and 15% random link failures using the FTP traffic pattern. Even when the packet size is increased, the results remain comparable in Mesh topology. It was observed that the Spidergon improves on these slightly with a lower network diameter but has longer average paths. MoS topology provides the best performance in terms of both **ARTICLE HISTORY:** high interconnectivity, minimizing both the longest and average path lengths. It was reported in Table 3 with latency using TCP protocol with FTP and CBR traffic scenarios in three topologies: Mesh, Spidergon, and MoS. throughput increased as packet size increased, as well throughput and latency due to its efficient structure and The bandwidth was set to 50 Mbps. As shown in Table 2, It was noticed that in Table 3 the latency of Mesh topology initially was less. However, with an increase in using the FTP traffic pattern. Mesh topology had the highest latency of 3.784608 ms.Spidergon topology was observed with a lower latency of 2.721523 ms at 2048 using FTP traffic pattern in TCP protocol. At 2048 Kbytes Mesh topology, with 2.721523 ms. The latency of Mesh

 $\ddot{}$

htly with a lower throughput increases constantly. However, at 15% link iverage paths. MoS failure, the throughput suddenly dropped after 512 technology paths. The run state is a conditional voltage per second in the second at the second in the second i
aco in terms of both in I V hutes in the ETD scenario. The results of ETD tru comparator for a highly linear 4-bit Flash A/D Converter (ADC). The outlined design Kbytes in the FTP scenario. The results of FTP traffic icient structure and youtterns are constant from 1024 Kbytes of packet size. oth the longest and however, in the first simulation analysis, the links in the ted in Table 3 with Spidergon topology failed at random up to 5%, 10% and TP and CBR traffic 15% random link failures are performed and simulated. In this case, which are the considerable measure of all the distributions.
Spidergon, and MoS. Even with random link failures, the throughput of the phuergon, and most α even with random this ratures, the throughput or α the comparator α As shown in Table 2, Spidergon topology was changed and reduced by using 13.75 . The re-: increased, as well the FTP traffic pattern. The throughput of MoS topology **Authority of the second is and the computer of the second in the second is also shown in the computation** with an increase in It was noticed that the throughput constantly increased topology had the obtained. Overall MoS topology yields better output than ergon topology was the remaining two topologies even with all link failures. with link failures 5%, 10%, and 15% are observed with the FTP traffic scenario and the results are shown in Table 4. in all three link failure cases and the same results were

721523 ms at 2048
Mesh tenelegies by Table 5 shows the throughput with link failures in a Mesh topology. However, by using CBR traffic patterns, the throughput remained constant despite all random link failures in the Spidergon topology. CBR throughput was consistent at 2048 Kbytes of packet size despite a 15% link failure. For all cases in CBR, the throughput observed was at 2048 Kbytes in the Spidergon topology. At 2048 Kbytes the throughput drops in the CBR scenario, the throughput suddenly drops to zero in MoS topology. And, even with link failure rates, the throughput of the MoS topology is higher than that of the other two to pologies. One of the techniques to obtain a super low \mathcal{L} TCP by CBR traffic scenario. In CBR traffic patterns, increasing packet size caused a spike in throughput for

> Table 6 demonstrates the latency of three topologies using TCP protocol by FTP traffic scenarios with link failures. The latency was the same with all link failures in Mesh topology. The latency results of Spidergon topology with FTP traffic patterns with link failures of 5%, 10%, and 15% are shown. The latency of Spidergon topology varies after 64 Kbytes packet size. The latency result

of an MoS topology with TCP protocol using FTP traffic patterns is demonstrated. As seen in the FTP results up to 64 Kbytes of packet size, the result with 2.286243 ms **related** in the attend with the members of the same in the same is the same in the same in the same is also seen obtained in all link failures 5%, 10% and 15%. When compared to the FTP traffic pattern Spidergon topology was observed with lower latency results than the other two topologies. is the same. The latency was then reduced to 2.311870

Table 7 demonstrates the latency of three topologies concentrated on the improvement of the concentration of the contract of the sensitivity and the sensitivity of the sensiti using TCP protocol by CBR traffic pattern with all link

failures. Mesh topology was observed with higher latency I CSULLS AND IT IS CONSTANT IN ALL INN TAILOR CASES. IT WAS observed that CBR scenario the latency is 4.397218 ms across all link failures and packet sizes. Spidergon topology was observed to have lower latency results than mesh topology. The results are observed uniformly and drop to zero at 2048 kbytes. The latency result of the MoS topology was lower when compared with the remaining two topologies. Overall, MoS topology was in all link failures. results and it is constant in all link failure cases. It was observed to have lower latency using CBR traffic patterns

Table 4: Throughput of three topologies using FTP traffic scenarios with link failure

1 depicts the block diagram of the proposed comparator. Comparator **Table 5: Throughput of three topologies using CBR traffic scenarios with link failures**

Sravani S and Deepak Ch: Performance Evaluation of Mesh, Spidergon, and Mesh of Spidergon (MoS) Topologies in Network-on-Chip (NoC) Architectures

can operate on a nominal supply on a nominal supply of 1.8 V. The comparator of the following Table 7: Latency of three topologies in a TCP protocol by CBR traffic scenarios link failures **The Contact of the U**

- The primary contributions of this study are as follows: Innovative Topology Design: The integration of Mesh and Spidergon topologies into a unified Mesh of Spidergon (MoS) architecture represents a novel approach in NoC design. This hybrid topology leverages the local efficiency of Mesh and the global routing advantages of Spidergon, creating a more balanced and efficient network structure.
- Performance Evaluation: The study provides a comprehensive evaluation of the MoS topology against traditional Mesh and Spidergon topologies. Metrics such as network diameter, average network distance, throughput, and latency are analyzed using TCP applications with

File Transmission Protocol (FTP) and Constant Bit Rate (CBR) traffic patterns.

• Resilience Analysis: The performance of the MoS topology is assessed under varying link failure scenarios at rates of 5%, 10%, and 15%. This structure at each capacitance of the gate tends to show a higher tends to show a higher tends to show a higher tends of the MoS analysis inginights are researned on the most threshold of the MOSFETS tends to the MOSFETS tends to the MOSFE to be higher. One of the techniques to obtain a super low comparable latency compared to its counterparts External of Moster with the MoSFETS is to the MOSFETS with the MOSFET lower gate capacitance. As the gate capacitance is lower

in the two types of MOSFETS, the threshold voltage will be the threshol

Network-on-Chip (NoC) is a communication architecture to the fitting the great increases the system on-Chip (SoC). Improject in the exception of system in single computers in Topologies play a pivotal role in the design of NoC. stripting the length of the length of the length of the length of the Mesh, Spidergon, and MoS topologies of NoC

with network diameter were analyzed using Python programming in the paper. The throughput and latency of these topologies were evaluated under TCP applications *relate* the contribution passesses were also evaluated for throughput and latency, with link failures at 5%, 10%, and 15%. Ultimately, the MoS topology was found to yield better results in terms of throughput. The MoS and Spidergon topologies exhibit comparable latency, and the Mesh topology is observed to have higher latency. The MoS topology can be used at the NoC architectural level, and the results can be used to assess NoC Quality of Service. with FTP and CBR traffic patterns. The three topologies

three-stage CMOS comparator with a high-speed operation to gain a lower static and a lower dissipation and a lower dissipation and a set of α and a lower dissipation and a lower distinction and a lower distinction and a lower distinction and a lower distinction and a lower d

- [1] Joshi,B.Thakur, M.K.(2018). Performance evaluation of various on-chip topologies, *Journal of Theoretical and* Applied Information Technology, 96 (15), 4883-4893.
- [2] T. N. Kamal Reddy, A. K. Swain, J. K. Singh, and K. K. Mahapatra (2014). Performance assessment of different Networkon-Chip topologies, 2nd International Conference on Devices, *Circuits and Systems (ICDCS)*, Coimbatore, India, 1-5.
- [3] A. Q. Ansari, M. R. Ansari, and M. A. Khan (2015). Performance evaluation of various parameters of Network-on-Chip (NoC) for different topologies, 2015 Annual IEEE India
Conference, Gujarat, India,1-4. Conference, Gujarat, India, 1-4.
- [4] JenitaPriyaRajamanickamManokaran, Mohammed A.S. Khalid (2017). Experimental evaluation and comparison Khalid (2017). Experimental evaluation and comparison
of two recent Network-on-Chip routers for FPGAs, designed that can be used with flash ADC. *Microprocessors and Microsystems*, 51, 134-141.
- **Architecture II, March St. Comparently, C. A. S., Naik, G. M. (2017). Performance** analysis of 16x16, 32x32, 64x64 2-D mesh topologies for network on chip application of MIMO, 1757-1764. [5] Charanarur, P., Rane, U. V., Gad, V. R., Kovendan, A. K. P.,
- [6] Panem, Charanarur, Udaysingh V. Rane, and Rajendra S. Gad (2017). Network on chip performance analysis over 2-D and 3D mesh topologies for CBR and FTP applications, India. *National Symposium VLSI and Embedded System*, Goa,
- [7] KusumKardam, Akanksha Singh (2016). A Review on Comparison on Network on Chip(NOC) Using Simulation Tool
NGC International Issued of Computer Science and Infor is performed. Then the buffer stage further amplifies to *mation Technologies*, 7 (3), 1486-1489. \mathcal{G} as strengthen the OTA OUTPUT signal NS2, *International Journal of Computer Science and Infor-*
- **A. Operational Transconductance Amplifier** [8] K Balamurugan, S Umamaheswaran, TadeleMamo, S Nagangan and Earstmand Ras hamamata (2022). Rodding for machine learning based network-on-chip (M/L NoC) technalong circuits with the linear input-output characteristics. The characteristics of *Physics Communications*, IOPscience, 6, 1-15. rajan and Lakshmana Rao Namamula (2022). Roadmap for
- [9] Chen, Jie and Li, Cheng and Gillard, Paul (2011). Networkon-chip (NoC) topologies and performance: a review, *Pro*ceedings of the 2011 Newfoundland Electrical and Computer Engineering Conference (NECEC), 1-6.
- [10] A. Alimi, Romil K. Patel, OluyomiAboderin, Abdelgader M. Abdalla, Ramoni A. Gbadamosi, Nelson J. Muga, Armando N. Pinto and António L. Teixeira (2021). Network-on-Advances and Research Direction, *Network-on-Chip - Ar*chitecture, Optimization, and Design Explorations. IntechOpen. We make the OTA stage by connecting \sim Chip Topologies: Potentials, Technical Challenges, Recent
- [11] L. Bononi and N. Concer (2006). Simulation and analysis of network on chip architectures: ring, spidergon and 2D mesh, *Proceedings of the Design Automation & Test in Europe Conference*, Munich*,* Germany.
- [12] Umamaheswari, S., RajapaulPerinbam, J.,Monisha, K., Jahir Ali, J. (2011). Comparing the Performance Parameters of Network on Chip with Regular and Irregular Topologies. *Trends in Network and Communications*, Vol 197. 177-186.
- [13] Al-Yateem, Nabeel, et al. "A Comprehensive Analysis on Semiconductor Devices and Circuits." *Progress in Electronics and Communication Engineering*, vol. 2, no. 1, Mar. 2025, pp. 1-15.
- [14] Kavitha, M. "Embedded System Architectures for Autonomous Vehicle Navigation and Control." *SCCTS Journal of Embedded Systems Design and Applications*, vol. 1, no. 1, 2024, pp. 25-28.
- NetworkX, Proceedings of the 7th Python in Science Conference (Scipy2008)GäelVaroquaux, Travis Vaught, and Jar-[15] Aric A. Hagberg, Daniel A. Schult and Pieter J. Swart (2008). Exploring network structure, dynamics, and function using rod Millman (Eds), Pasadena, CAUSA, 11-15.
- [16] Zhang, Wang and Hou, Ligang and Zuo, Lei and Peng, Zhenyu and Wu, Wuchen (2010). A Network on Chip Architecture and Performance Evaluation, *2010 Second International Conference on Networks Security, Wireless Communications and Trusted Computing*, Hubei, China, Vol 1, 370-373.