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Research Article

Design And Analysis Of 1-Bit Full Adder Using Cntfets

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ABSTRACT
As the technology is scales down beyond the certain limit it is going to be affect the performance of the system in terms of power, speed and etc. Hence in order to overcome the above issues researchers proposed a novel transistor such as carbon nano tube field effect transistors in the place of CMOS technology. In this paper we proposed a novel CNTFET based full adder circuits for digital application. this full adder circuit has been implemented using the 32 nm technology using the CNTFET model files. the proposed full adder circuit we have measured the delay, power and PDP by varying the output load (capacitance) and voltage respectively.

keywords: Low leakage power, Carbon nanaotube field effect transistors, full adders, cadence virtuoso.

Introduction

As the advancement of technology day by day this eventually leads to shrinking of the length of the transistor. Hence it is very much necessary to accommodate the more number of transistors on single silicon chip. now current day cutting edge technologies are mainly focuses on the reduction of the power and leakage current respectively. But beyond scaling the 45nm nm technology and further CMOS devices are vulnerable to the several effects such as band to band tunnelling leakage, sub threshold leakage etc. Hence in order to overcome these above vulnerabilities researchers proposed a several new technologies such as carbon nanotube filed effect transistors(CNTFET),single electron transistor, fin field effect transistor etc. Among these transistors CNTFETs are one of the promising technology and which offers the high performance, low power designs etc[1-5].

The classification of the CNTFETs has been described in several ways and The basic architecture of the CNTFETs as shown in the figure 1 and 2 respectively.

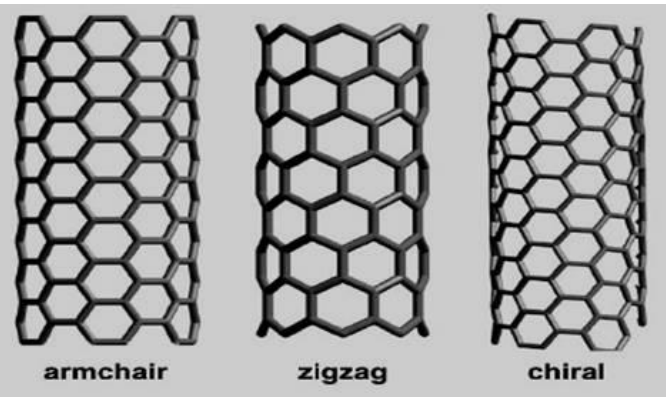

Fig.1: Different structures of CNTFETs

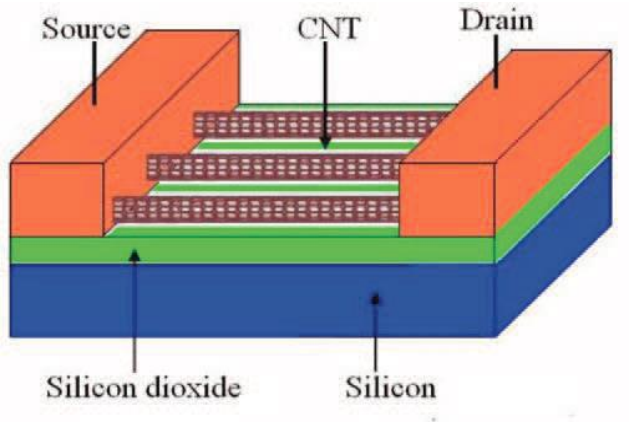

Fig.2: Transistor level structure of CNTFETs.

CNTFETEs are an allotropes of the graphite and which can be available in several forms such as single wall or multiwallCNT etc. The single wall CNT having only one wall of cylinder and where as MWCNT having multiple number of CNTs. The width of the CNTFET can be calculated by equation 1 .

$$W_{gate} \approx Min(W_{min}, N \times Pitch)$$

where W_{min} is the minimum width of the gate and N is the nano-tube under gate. the I-V characteristics of the MOSFET and CNTFET are similar with each other respectively[6-8].

The threshold voltage of the CNTFET can be calculated as the half band gap and it can be calculated as the below equation 2.

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)}$$

Unlike MOSFETs the CNTFETs can be well suitable for the ultra high performance digital applications. And this type of FETs are also called as the band to band tunnelling CNTFETs. The following section describes the operation of the proposed single bit CNTFET based full adder.

Design and analysis of CNTFET based full adders

Full adder is one the basic digital block in the many digital systems. This can be mainly used to perform the arithmetic and logical functional operations. It acts as the one of the key component in the all the Micro processor, DSP architecture and data processing system respectively. The logic function of the 1-bit full adder having inputs A,B, C and its outputs should be sum and carry. mathematically it can be represented by the equation 4 and 5[9-10].

$$Sum = XOR(A,B,C_{in}) = A.B.C_{in} + A.\overline{B}.\overline{C_{in}} + \overline{A}.B.\overline{C_{in}} + \overline{A}.\overline{B}.C_{in}$$
$$= A.(B \odot C) + B.(A \odot C) + C.(A \odot B)$$

$$C_{out} = Majority(A,B,C_{in}) = A.B + A.C_{in} + B.C_{in}$$

The proposed full adder circuit as shown in the figure 3 it consist of the two individual CNT pass transistor configuration ,which can used to implement the sum and carry. The first network is a 3 input XOR circuit and it can produce the sum output and followed circuit is the carry circuit which can be generates the carry output respectively.

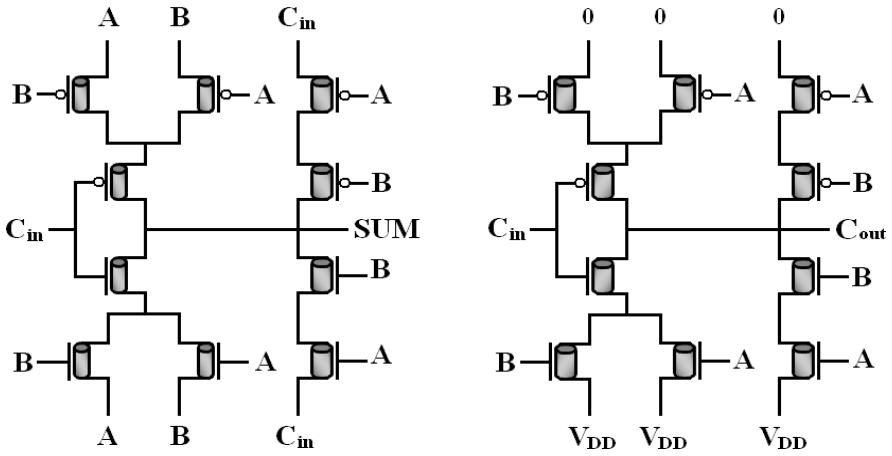

Fig.3: Proposed CNTFET based full adder.

The proposed CNTFET are comprehensively designed by 32 nm CNTFET technology using model files and its operation can be simulated using the cadence virtuoso. The circuit can be evaluated more precisely by varying the circuit load capacitor and power supply voltage. from the obtained results calculated the circuit delay and power. for the experimental setup we changed the capacitor load from the 1.5fF to 5.7fF. As the capacitor load increases then the circuit consumes the more power and load capacitance is increases. the voltage being varied from the 0.8v to the 0.4 v respectively. The table 1 indicates the estimation of the delay, power and PDP of the proposed 1 bit CNTFET based full adder. and the figure 4 depicts the variation of output power with respect to the voltage and load capacitance.

Table:1

Parameter	value
Delay	41.258ps
Power	2.02585w
Power Delay Product	1.25828j

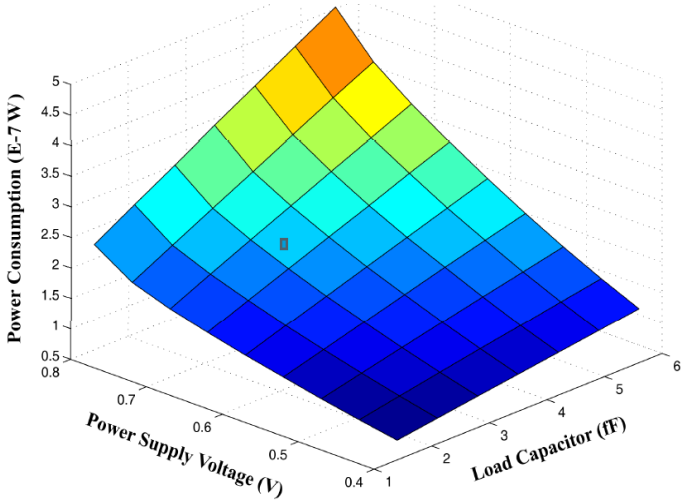

Fig.4: variation of power consumption with respect to the supply voltage and load capacitance

Conclusion

This paper investigates the high speed and high performance single bit full adder using the CNTFET based full adder. The sum and carry generator of the full adder can be symmetrical and have the hardware configuration. The CNTFET provides the better performance inters of the speed, area and power dissipation . The state of the art in 32 nm CNTFET based full adder is well suitable for the high speed digital applications.

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