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Research Article

Different Casues For Reduction Of Lekage Current In Sram:A State Of The Art

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ABSTRACT
As the semiconductor devices are increases the very fast speed ,the size of the portable devices are shrinking down drastically. Hence which results demand for the long battery life for the electronic devices which we are using our day to day life. Memory in electronic device plays a critical role in order to processing the data as well as to store the data. But over the past decade the memory devices(SRAM and DRAM) suffers for the various factors due to leakage power, current etc. In this paper we are going to describe the a detailed study of various techniques to overcome the leakage factors affecting the SARAM devices. out of the several techniques differential leakage power technique has been one of the primary technique to overcome the leakage current in CMOS devices.

keywords: CMOS technology, leakage current, reverse body bias.

Introduction

Last few years the length of the CMOS devices are shrinking down drastically to reduce the size of the transistor, therefore to achieve the high speed, low power and to integrate large number of transistors in a single chip. But minimization of these features largely effects the leakage current and power dissipation etc. This power dissipation could be either static or dynamic respectively[1-5]. hence to overcome these problems and to reduce the leakage current in CMOS devices several techniques has been proposed such as sleep transistor technique, forced stack technique, sleepy stack technique, lector technique etc. These techniques eventually reduces the leakage current by controlling the path between pull up and pull down transistors respectively. The figure 1 depicts the normalized power dissipation over the 1995-2020 with respect to channel shrinking.

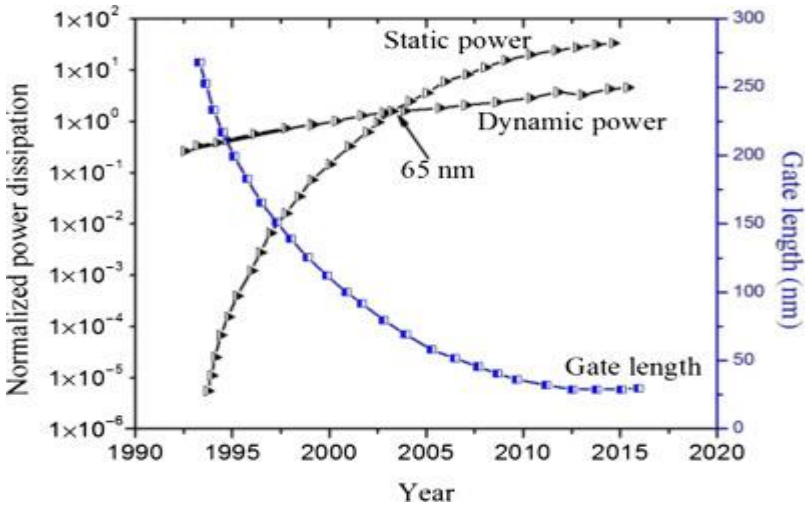

Fig.1: Power dissipation based on technology nodes.

Major leakage currents in CMOS based SRAM devices

In a CMOS transistors its working can be defined in two ways such as conducting and non-conducting and the set of available ways of leakage currents can be defined as gate induced drain leakage, sub threshold leakage and punch through current and

corresponding leakage current of each one can be explained in a detailed way in the following section.

Drain induced barrier lowering(DIBL)

As long as high voltage being applied to the drain terminal then the depletion region of drain start interfacing with the source terminal. due to this potential the drain and source is lowered. hence the leakage current stars flow between source and drain. and its impact could be more in linear region. figure 2 depicts the structural representation of DIBL.

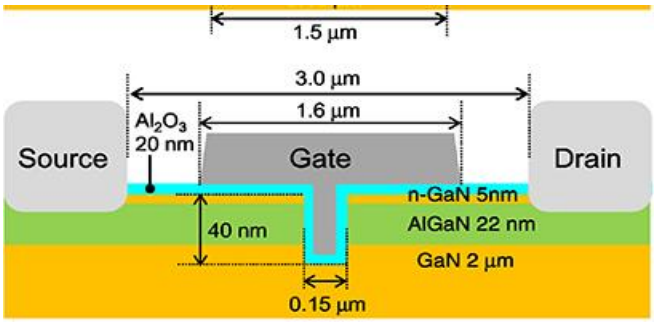

Fig.2: Effect of DIBL in CMOS devices.

Junction reverse leakage current

It is usually happens the at drain to body as well as source to body terminal. these terminals are reverse biased and due to which PN junction reverse leakage current flows. figure 3 depicts the junction reverse leakage current in CMOS devices.

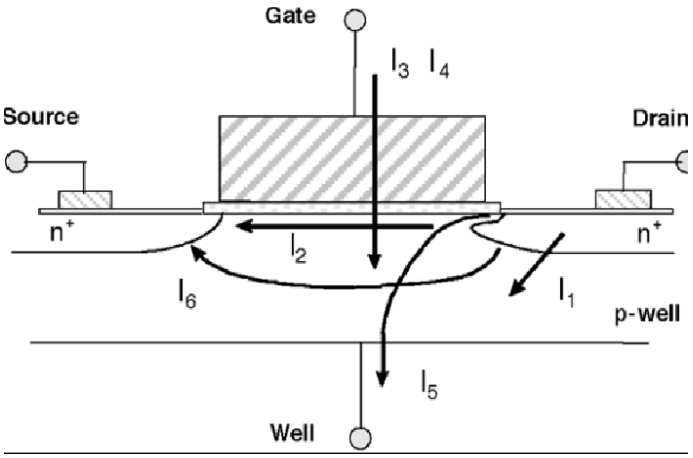

Fig.3: Effect of Junction reverse leakage current in CMOS devices.

Sub threshold Leakage Current (Weak inversion)

It is one of the major contributor for responsible of the total leakage current from the source to drain. This is usually present between source and drain when the transistor in week inversion region. as long as scaling the device the sub threshold leakage current will be increased. and this current can be varies with respect to Vgs and Vth respectively. this phenomenon can b e seen in figure 4 respectively.

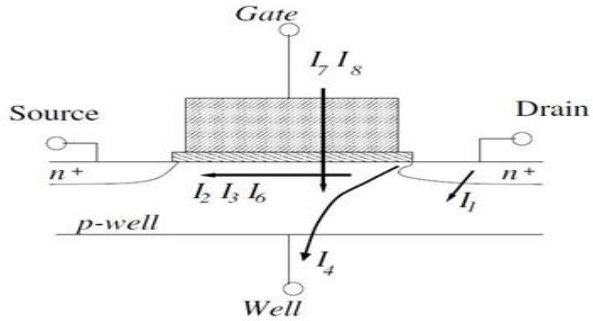

Fig.4: subthreshold leakage current representation in CMOS devices.

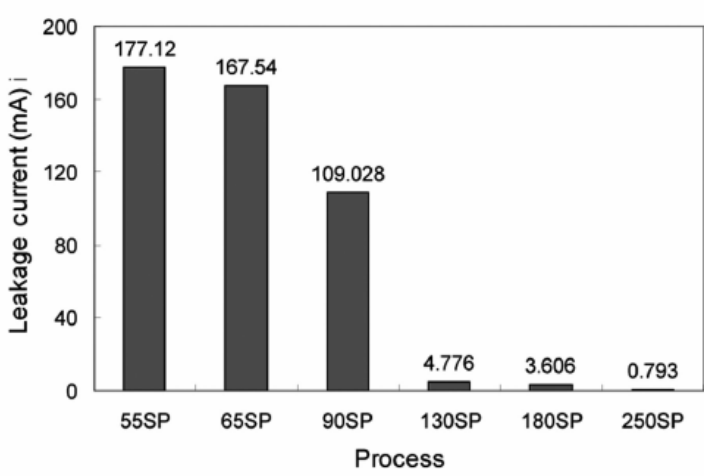

Fig.5: Leakage current with respect to process variations.

As long as the technology is keep on increases which results increase in the power dissipation. Figure 5 depicts the incenses of the power over the period of time respectively.

Conclusion

This paper gives the a quantities survey of different types of SRAM leakage methodologies and different leakage problems in current day modern digital systems. From the above survey it is mentioned that the above factors are greatly responsible for the causes of leakage current in the SRAM devices.

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