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Design and Performance Analysis of Adiabatic Logic Circuits Using FinFET Technology

Anas A. Salameh[1*], Othman Mohamed[2]

[1]Associate Professor, Department of Management Information Systems, College of Business Administration, Prince Sattam Bin Abdulaziz University, 165 Al-Kharj 11942, Saudi Arabia.
[2]Department of Quantity Surveying, Faculty of Built Environment, Universiti Malaya, Malaysia.

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Abstract

Power dissipation is now a major concern in large-scale integration (VLSI) design, particularly in high-performance, low-power applications, as semiconductor technology shrinks. Because of its reputation for energy harvesting, adiabatic logic provides a practical means of reducing the dynamic power consumption of integrated circuits. Unlike conventional planar MOSFETs, FinFET technology offers better electrostatic control, lower losses, and greater scalability. This paper proposes the design and performance analysis of adiabatic logic circuits using FinFET technology. The study applies FinFET technology at 22 nm and 14 nm process nodes to implement important adiabatic logic families such as adiabatic positive feedback logic (PFAL) and energy recovery logic (ECRL). The circuits are designed in a simulated manner and their performance is evaluated in terms of latency, power efficiency, and power dissipation in a standard Cadence environment. To demonstrate the benefits of FinFET-based adiabatic designs to achieve lower power consumption, a comparative analysis with conventional CMOS circuits is also depicted. FinFET-based adiabatic circuits are especially well-suited for low-power VLSI systems, as demonstrated by the considerable reductions in power dissipation and energy per operation found in the simulation results.

Author's e-mail: a.salameh@psau.edu.sa, othmanmohamed@um.edu.my

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1. Introduction

Recent years have seen a tremendous advancement in transistor technology, leading to increased integration density and performance. Concurrently, the main obstacle preventing VLSI circuit design from progressing further is the steadily rising power. Static power and dynamic power are the two components that make up power consumption. Static power results from intrinsic device leakage when the circuit is in the off state, whereas dynamic power is the result of switching activity throughout the charging and discharging operation. Therefore, when designing a low-power VLSI circuit, it is necessary to consider both dynamic and static power. Dynamic power used to be the primary factor in power usage in the early era. To lower dynamic power, numerous innovative circuit technologies have been invented, including adiabatic circuits, sub-threshold circuits, and multi-threshold circuits. Among these is adiabatic logic, a revolutionary low-power circuit topology that recycles circuit energy by using an AC voltage supply instead of a DC voltage source.

Because of the forced synchronisation between the node voltage and the power supply, the node capacitance only stores 0.5 CV2, preventing heat dissipation during the charging and discharging phases.[1] Moreover, when the voltage supply returns to zero, t he stored energy can return to it. Theoretically, adiabatic logic can achieve zero power usage without taking leakage power into account. Up until recently, dynamic power was the main factor in power usage. Adiabatic logic is a unique low-power circuit layout that recycles circuit energy using an AC supply rather than a constant DC one. Other low-power design concepts including sub-threshold, multi-threshold, and adiabatic logic have also been proposed to minimise dynamic power.

In theory, the adiabatic logic can attain zero power usage even in the absence of leaking power. Recent years have seen a significant amount of study on low power adiabatic logic.

Power saving is the primary design criterion in the field of VLSI (Very Large Scale Integration) circuit design since a circuit's capacity to optimise power has a significant impact on its overall performance.

The ALU is the central component of microprocessors, microcontrollers, and digital computers, handling all calculations and operations. Over the past few years, there has been a sharp rise in the need for low-power, lightweight, non-portable devices. The unavoidable and intolerable short channel effects were encountered when scaling MOS transistors down to the nanoscale.[2] Furthermore, adiabatic design method has a lower power loss than typical CMOS design topology. On the other hand, a FinFET-based circuit's power consumption can be significantly decreased. In the case of the standard CMOS inverter seen in Figure 1.1, the total energy extracted from the supply voltage when the PMOS transistor is turned on.

The goal of this work is to employ adiabatic logic to create an ALU circuit based on FinFETs. The results indicate a promising reduction in power consumption, which can be attributed to the combined impacts of adiabatic design and device technology (FinFET). The findings also demonstrate that a typical MOSFET inverter uses about 40 nW of power at frequencies of 100 MHz, 200 MHz, and 500 MHz. At the same frequencies, a typical FinFET inverter consumes roughly 0.578 nW, 1.32 nW, and 6.25 nW of power, whereas the same frequencies used in the proposed design consume approximately 24.19 pW, 37 pW, and 140.4 pW of power, respectively. Consequently, the FinFET-based adiabatic logic design technique offers superior power utilisation and suppression at all frequencies. Additionally, a unique 16-bit ALU design

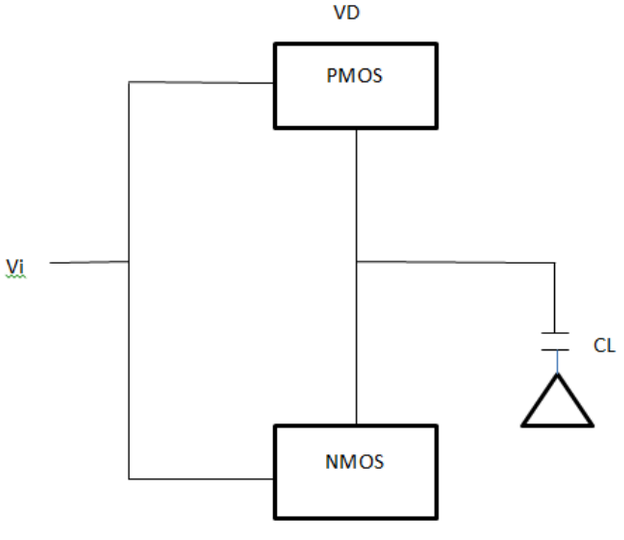

Fig. 1.1: Diagram of a CMOS Inverter

that combines the adiabatic switching principle with FinFET technology is shown. It performs better in terms of delay and power optimisation. It was suggested to use a 32x32 register file based on dual transmission gate adiabatic logic in a bigger memory in order to lower the energy dissipation. An adiabatic 5T SRAM with great density and energy efficiency was proposed by Samson and Mandavalli.

The study focusses on ultralow-power adiabatic sequential circuits, such as D, JK, and T flip-flops. Differential Power Analysis (DPA) resistance of the adiabatic logic families is reportedly higher than that of the traditional CMOS logic.[3] However, there is a noticeable increase in leakage current due to the constant scaling of threshold voltage and device technology, which accounts for a large portion of power usage. Therefore, high leakage currents make the realisation of effective bulk CMOS adiabatic logic circuits difficult.

Therefore, investigating new gadgets is necessary to lower the leakage power. FinFET is suggested as a good substitute among them to deal with the issues brought on by the ongoing scaling. This gadget operates with low power consumption and excellent performance. It has the ability to reduce both the gate-dielectric leakage current and Short-Channel Effects (SCEs).

The remainder of the paper is indicated by the following. Basic knowledge about subthreshold adiabatic 1ogic and FinFET is given in Section 2. Our recommended design for the basic 1ogic gates is described in Section 3. Section 4 presents the installation of different gates, along with the experiment results, comparison of our chosen design, and correlation with the data presented in Section 5.

2. Related Works

When the nodes are discharged from their charged state—the recovery phase of the adiabatic circuits—they recover the energy. Thus, this reasoning aids in lowering the circuits' overall power and energy dissipation.[4] In high density systems, the memory cell design that incorporates such adiabatic logic will result in significant power savings. In the literature, a number of adiabatic logic circuits driven by trapezoidal power clocks have been reported. The four distinct phases of the commonly used power clocks are evaluated, hold, recover, and wait or idle phase.

The digital system is seeing a growing demand for 10w power applications, such as MobiLink, BMI, space engineering, etc. The key concern for these applications is 10w energy consumption at the performance rate.

Circuits employ the leakage current as the operating current and operate at a voltage lower than the threshold voltage.[5] One of the circuit design methods used to create secure and energy-efficient hardware is adiabatic 10%. It is possible to produce a key for cryptographic systems using adiabatic 10gic. In a survey contributing survey that evaluates a board range of comparator measurements and examines their applicability for ultra-10w power amplifiers, concluding that adiabatic 10gic is one of the most promising methods for designing secure and energy-efficient electronics.

Power is lost in pull-up and pull-down MOS devices in conventional CMOS circuits while the nodal capacitance is being charged and discharged.[6] When running at high frequencies, this causes CMOS circuitry to dissipate more power. These drawbacks suggest a novel, current logic known as "Adiabatic Logic" or "Energy Recovery Logic." This is achieved by recovering a significant amount of the energy utilised in the nodal capacitances, and using that recovered energy in the ensuing calculations. Technology scaling increases leaky power dissipation. Leakage power can be attributed to various major reasons, including sub-threshold leakage current resulting from low threshold voltage and gate leakage current caused by thin gate-oxide material.

However, side-channel attacks can be used to get the confidential or private data that is transmitted and stored by these Internet of Things devices.[7] Differential Power Analysis (DPA) attack is one of the most potent side-channel attacks to extract confidential data from protected devices among the many side-channel attacks documented in the literature. Over time, a number of hardware-related DPA countermeasures have been created. However, none of these countermeasures are appropriate for use in gadgets where power consumption is limited.

One such technology that allows for transistor length reductions of up to 5 nm is FinFET. This aids in lowering the necessary die area. Different adiabatic logic has led to the proposal of several SRAM architectures. Based on the reduced power dissipation factor, it was determined that Modified Cascode Pre-resolve Logic [MCPL] was one of the adiabatic logic design styles.[8] The structure was compared to alternative non-adiabatic logic structures that utilised FinFET 32nm technology. Another creative method that was created and put into use was the SRAM cell based on ECRL. It was created with the goal of using less power to create an effective SRAM memory cell arrangement. This method used less electricity and increased speed.

The semiconductor industry has worked very hard over the last few decades to make progress in the ongoing decrease of the size of electron devices. From a technical perspective, scaling is still one of the biggest issues of today. Field Effect Transistors (FETs) now have channel lengths in the tens of nanometres range instead of micrometres. In order to boost performance while reducing the active area of integrated circuits, transistor size must be lowered. But there are issues with scaling that need to be resolved for every technological node.[9] Innovative transistor architectures need to be explored in order to address the scaling issues that have been shown. Using FinFET is one of the most popular methods out there.

The scaling of technology leads to threshold voltage lowering and concomitant increase in leakage current. This will affect the adiabatic logic circuits' ability to recover energy when subjected to CMOS and DPA attacks. This means that in order to be helpful for these applications, new low-power and secure devices must be investigated. FinFET stands out among the various devices offered as having a lower leakage current.[10] Although there are several DPA attack defences in the literature, power consumption is the main design restriction, and hence these countermeasures cannot be implemented in devices. Due to its energy recovery approach, adiabatic logic is one of the low-power and secures design techniques.

3 Methods and Materials

3.1 Grouping of ADIABATIC LOGIC

Adiabatic circuits fall mostly into two categories:

i) Reversible logic and

ii) energy/charge recovery logic.

- Recovering Energy/Charge Due to the irreversible energy used to operate the circuit, logic only recovers a portion of the energy lost accidentally.
- Reversible logic allows the utilisation of the output states since it recovers the input vector uniquely from the output vector in a one-to-one correlation.

Numerous findings indicate that the amount of information used directly correlates with the least energy needed. Therefore, in theory, the energy needed to run such a circuit could be 0 if a design method could be developed without resulting in any information loss. Through reversible computation, IBM's Bennett and Landauer proved that there can never be information loss, and so, theoretically, no energy could be needed. When there is no information loss throughout a system's transformation, it is referred to as reversible. A detailed description and illustration of the further classification of Energy/Charge Recovery Logic are provided in Figure 3.1.[11]

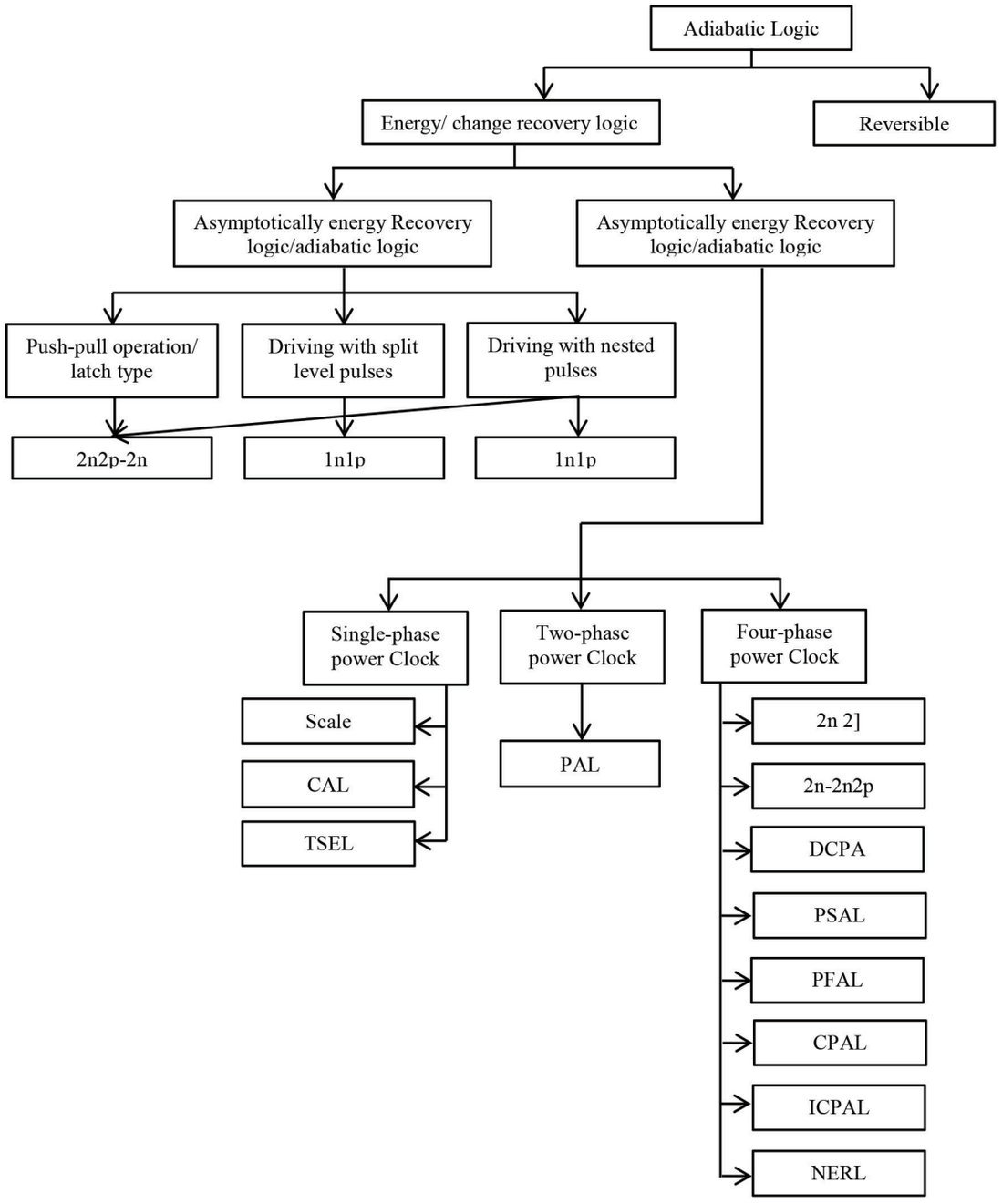

Fig. 3.1: Adiabatic Logic Classifications

3.2 The inverter's design

With just one input and one output, this is the most basic kind of gate. If the input is "0," it generates a "1" output, and vice versa. In other words, the output generates an inverted copy of the input. Its other name, Inverter, stems from this.[12]

Researchers have tried numerous approaches to boost integrated circuit speed and performance. As a result, according to the well-known Moore's law, the number of transistors per integrated circuit or chip increases by

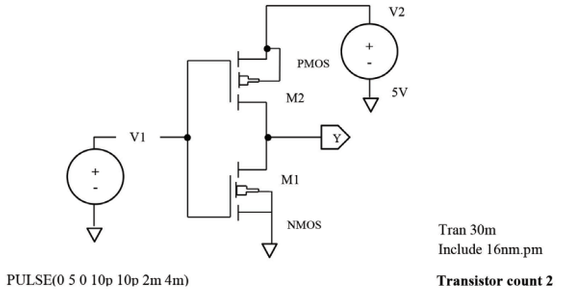

Fig. 3.2: Utilising CMOS logic, inverter

two times year. Either enlarging the chip or reducing the size of the transistors has allowed for this increase in the number of transistors (see Figure 3.2).

However, the primary driver of higher chip density is the reduction of transistor size.

It is evident that when the size of the gadget is reduced to 28 nanometres, numerous obstacles concerning its construction and features arise for the researchers. Short channel effects have an impact on transistor performance at that small dimension. Even when the device is turned off, the short channel effect leads to an exponential increase in leakage current between the source and drain terminal, which makes the gate lose control over the channel to the point where it is unable to shut it off entirely. Alternative transistor designs were pursued by researchers due to these and other technological difficulties.

Because FinFET technology allows transistors to be shrunk down into the sub-20nm region, it was created to solve the issue of SCE.[13]

The short channel effect (SCE) becomes a major worry as MOSFET (Metal Oxide Semiconductor Field Effect Transistor) dimensions drop. This increases leakage current, which in turn increases power dissipation. A novel approach to designing logical devices has been put forth: FinFET technology. This technology reduces leakage current and, consequently, power dissipation. Both CMOS and FinFET technologies have been used in the design of numerous devices, such as inverters, adders, and MUXes, to compare different factors such power dissipation, delay, and power delay product. Here in this research, we have tried to construct these circuits at channel length of 16nm using spice program. So, this article compares FinFET technology with CMOS technology (see Figure 3.3).

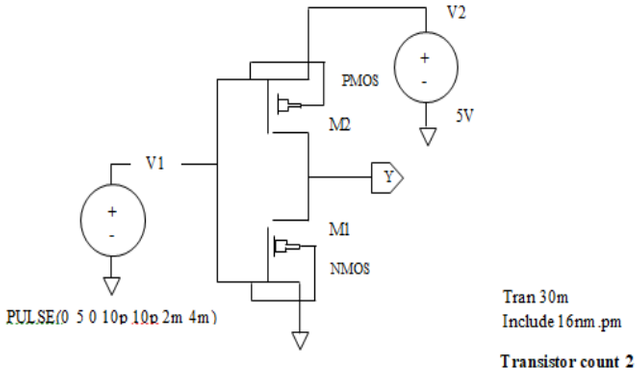

Fig. 3.3: Using FinFET technologies in an inverter

4. Implementation and Experimental Results

With the same power supply as stated in tables 1 and 2,[14] the output voltage fluctuation with respect to time is shown in figure 4.1. This information helps us determine the average power dissipation and time delay at 16 nm channel length.

Table 1: Comparing the Power Dissipation of FinFETs and MOSFETs

DEVICE	MOSFET	FINFET
INVENTER	1.991µ	1.969 µ
NAND	1.893 µ	1.256 µ
NOR	1.783 µ	2.323 µ
Half Adder	2.003 µ	1.895 µ
Full Adder	3.752 µ	2.677 µ
2:1 MUX	2.656 µ	1.323 µ

The power dissipation and time delay comparison between circuits based on MOSFET and FinFET technology is clearly shown in the following graphs. Here, the power dissipation and time delay in each circuit based on CMOS and FinFET technologies are clearly related. CMOS-based circuits use more power than FinFET-based circuits because they dissipate more power in former than the latter. Additionally, CMOS circuits have a greater time delay measured in microseconds than FinFET circuits.

Table 2: A comparisons of the FinFET and MOSFET's time delays

DEVICE	MOSFET TECHNOLOGY	FINFET TECHNOLOGY
INVENTER	434.428n	527.4349f
NAND	0.098µ	0.0075µ
NOR	0.083µ	0.0071µ
Half Adder	0.28875µ	126.7p
Full Adder	0.0641µ	85.1239p
2:1 MUX	402.38n	9.9n

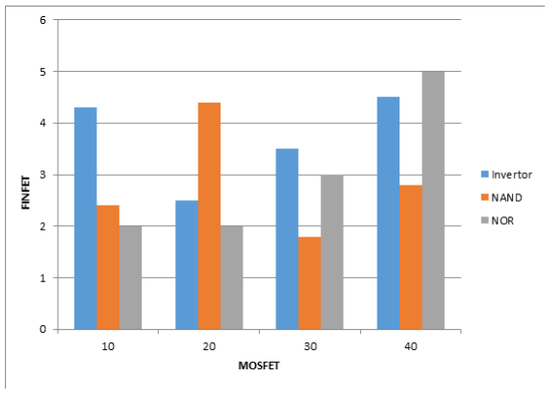

Fig. 4.1: Power Dissipation of the NAND gate, NOR gate, and inverter

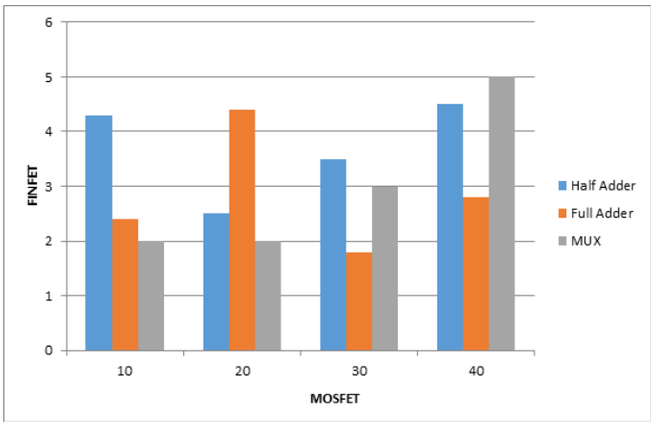

Figure 4.2: Power Dissipation of 2:1 MUX, whole adder, and half adder.

The relationship between power dissipation in each circuit developed with both CMOS and FinFET technology is shown in the Figure 4.2 and the time delay of each circuit designed with both technologies is shown in the last six numbers.

The gate wraps the channel 1 of the FinFET in three directions, forming the three dimensions of the FinFET device. FinFETs offer a stable gate circuit over a single channel.

Compared to M0SFETs, strong gate transistors lower the threshold current, gate-die1 electric leakage current, and the shadow-channe1 effects. Superior gate conductance in FinFETs compared to MOSFETs leads to increase on-state current, lower leakage, and quicker switching. The multiple-gate topology of FinFET provides 110w for various working modes of FinFET.

Comparing implemented circuits in a planned structure to those in a ventricle results in energy savings.[15] The logic circuits based on FinFETs are presented in this paper. Following implementation, we observed appreciable progress in lowering power and area of adiabatic linear circuits in comparison to convective linear circuits. This reduction in power and size in 32nm technology opens up new possibilities for effective FinFET-based design performance. Further applications of the deployed technology include energy-efficient and energy-saving gadgets that require ultralow power consumption.

5. Conclusion

In |the first section, this article presents a general introduction to adiabatic logic and compares the performance of circuits created with FinFET devices to those designed with CMOS devices. The significant power consumption reduction in the quasi-adiabatic circuits under discussion validates the benefit of employing FinFETs over CMOS. This is because of the FinFET devices' capacity to block leakage currents and short-channel effects.

FinFETs provide significantly better outcomes than conventional MOSFETs, as demonstrated by the work presented in this thesis. The FinFET-based circuits' power dissipation and time delays have been significantly reduced. When evaluating the performance of a digital circuit, power consumption and time delays are among the most crucial factors, particularly for portable devices that depend on batteries for operation, which run on batteries and are portable.

FinFET devices have the potential to supersede conventional transistors under the technological node of 16nm and beyond, based on the designs space they offer. FinFETs are becoming more and more popular as a great alternative to traditional transistors because of their superior performance and simplicity of manufacture. The FinFET fabrication method is nearly identical to that of conventional transistors. Intel has already declared that the tri-gate FinFET is its preferred technology for producing processors at the 7nm technology node.

In this research project, FinFET semiconductors of the short gate type are used to construct digital arithmetic circuits. Because it allows us to separately regulate the two gates and more effectively manage the channel, the other form of FinFET device, known as an independent gate, also offers a variety of design alternatives resulting in more creative design approaches, but at the expense of additional space because the front and rear gates need to be connected twice.

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