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Design and Optimization of Coarse-Grained Reconfigurable Array (CGRA) Architecture for Efficient Processing-in-Memory (PIM) Systems

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Abstract

The Coarse-Grained Reconfigurable Array (CGRA) architecture for Efficient Processing-in-Memory (PIM) systems is presented in this article. PIM architectures that incorporate computational capabilities directly into memory present a promising solution to mitigate the memory wall issue. There are several difficulties in CGRA architecture optimization for PIM systems especially when it comes to striking a balance between area efficiency, power consumption and performance. The proposed framework tackles these problems by examining crucial design components like processing element (PE) architecture memory hierarchy integration and interconnect design. Using a design space exploration (DSE) methodology we assess various CGRA configurations to find the optimal trade-offs between computation throughput, power consumption and silicon area utilization. To assist in selecting effective architectures that meet different application workloads the framework combines performance analysis and advanced modeling techniques. Based on test results, the optimized CGRA architecture for PIM achieves significant improvements in processing performance (20 percent increase in throughput), area reduction and energy efficiency (up to 40 percent reduction in power consumption) when compared to conventional PIM designs. Our architecture is well-suited for data-intensive applications such as machine learning and graph analytics since these enhancements are achieved without compromising computational accuracy or scalability.

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Introduction

The rapid advancement of computing technologies and the increasing need for high-performance data processing have necessitated the development of new computing architectures.[1] In recent times the memory wall problemwhich occurs when there is a data transfer bottleneck between the CPU and memory has posed serious difficulties for conventional von Neumann designs. When enormous volumes of data must be moved back and forth between memory and processing units as in the case of graph processing big data analytics and machine learning this issue becomes especially difficult.[2] Notable delays higher energy consumption and worse performance result from this. Processor-in-Memory (PIM) is a highly promising solution to the memory wall problem. Processing-in-Memory (PIM) is a revolutionary development in computing design since it incorporates computational capabilities directly into the memory itself.[3] This architectural strategy reduces the amount of data movement by computing in or near memory. In modern computing systems data transfer between the CPU and memory is one of the most energy-intensive processes.[4] By addressing this latency PIM not only lowers power consumption but also significantly reduces memory access latency. Workloads requiring data-intensive and low latency access to large datasets benefit greatly from PIM architectures. PIM system optimization for all its advantages is still challenging particularly when it comes to balancing computational load and power consumption. In this sense the Coarse-Grained Reconfigurable Array (CGRA) design shows promise.[5,6]

Coarse-Grained Reconfigurable Array (CGRA)

A scalable and adaptable architecture known as the Coarse-Grained Reconfigurable Array (CGRA) is made up of a variety of processing elements (PEs) that can be rearranged to meet the unique computational requirements of a particular workload. CGRAs are better suited for high-level operations in data-intensive applications because they operate at the word level as opposed to the bit level of fine-grained reconfigurable architectures like Field-Programmable Gate Arrays (FPGAs).[7] Because CGRA architectures are inherently parallel they can process data more quickly and are therefore ideal for applications like real-time data processing data analytics and machine learning. CGRAs can also be dynamically reconfigured which means they dont have to be completely redesigned or re-implemented in order to adjust to varying workloads.

CGRA architectures present the possibility of notable gains in energy efficiency and performance when applied to PIM systems. Compute speed directly within the memory array can be increased by integrating CGRA which also minimizes power consumption and lowers data movement latency. It is not without difficulties though to optimize CGRA for PIM systems. Balancing the trade-offs between power consumption silicon area utilization and processing performance is one of the main challenges. In assessing the overall effectiveness and viability of a PIM system based on CGRA these variables are essential.

Challenges in Optimizing CGRA for PIM

Processing Element (PE) Architecture: Achieving the best possible performance in PIM systems depends on the design of the processing elements in the CGRS. Keeping a high computational throughput requires each PE to be energy and area utilised efficiently. It takes careful consideration of the register files control logic and arithmetic units used in the PE to achieve this balance. Furthermore in order to effectively handle a variety of workloads support for various data types and computational models is imperative.

Integration of memory hierarchy: The integration of memory and computing units is one of PIM systems primary challenges. The memory hierarchy and processing elements must be closely correlated in CGRA architectures. A memory access model that is both efficient and minimizes power consumption is needed to enable low-latency data access. The need to support dynamic memory access models which can differ greatly depending on the application further complicates this integration in CGRA-based PIM systems.

Interconnection architecture: A key factor in determining the systems overall performance is the CGRS interconnection network. It is in charge of data transfer between memory and processing components. In order to facilitate high-bandwidth low-latency communication for PIM systems the interconnect needs to be built with low power consumption in mind. The design of interconnect is crucial to maximizing CGRS for PIM systems since it must also be adaptable enough to handle various computer models and workloads.

Design Space Exploration (DSE) for Optimization

A thorough design space exploration (DSE) methodology is required to address these issues. Finding the best trade-off between performance area and energy consumption requires analyzing various design configurations as part of DSE. This procedure entails investigating various arrangements for the processing components the memory hierarchy and the interconnection network in the context of CGRA-based PIM systems. These configurations can be simulated and analyzed to find the architectures that balance efficiency and performance the best for a particular workload.[8]

In this research, we provide a DSE framework to assess various CGRA configurations by combining sophisticated simulation methods with performance modeling. We can evaluate how different design parameters affect the overall performance and energy efficiency of the system using this framework. By using this method we try to find the best possible configurations that minimize space and power usage and increase computational performance.

Performance Improvements

When compared to traditional PIM designs the optimized CGRA architecture described in this paper achieves notable gains in processing performance energy efficiency and silicon area utilization. Specifically our architecture demonstrates a notable 40% reduction in energy consumption a 20% increase in computational capacity and a significant area savings. As a result of these advancements computational accuracy and scalability are not compromised which makes the suggested architecture especially appropriate for data-intensive applications like graph analysis and machine learning.

In summary a potential remedy for the issues raised by the memory wall is the incorporation of CGRA into PIM systems. We can achieve notable gains in performance energy efficiency and area utilization by taking advantage of CGRAs reconfiguration and parallelism. According to our research CGRA-based PIM systems can

offer an effective and scalable foundation for upcoming data-intensive applications if processing elements memory hierarchy and interconnect design are carefully optimized.

Literature Review

[9]Proposed SmartCell, a unique coarse-grained reconfigurable architecture that combines programmable interconnecting fabrics with a large number of CPU components on a single chip. For stream-based applications, SmartCell can offer high performance and energy-efficient processing. 0.13 µm CMOS standard cell technology is used to create the 64 PE SmartCell prototype. The comparison results demonstrate that ASIC and FPGA have different performance and flexibility gaps that can be filled by the SmartCell. In comparison to the assessed benchmarks, it is also roughly 8% and 69% more energy efficient than the Montium and RaPiD systems.

In order to overcome the constraints of graph processing,[10] introduced , a brand-new accelerator that improves on conventional CGRA architectures to increase the efficiency of graph applications. introduces a unique data-centric mode for effective graph processing while maintaining the traditional CGRA execution mechanism. In particular, it supports dynamic routing of temporary data based on the runtime evolution of the graph frontier and takes advantage of the inherent data parallelism of graph algorithms by mapping graph vertices onto PEs instead of the operations. According to experimental results, outperforms traditional CGRAs by up to 36× while requiring only 19% more space. has 2.2× greater area efficiency and similar energy efficiency at a considerably lower power/area budget compared to the most advanced large-scale graph processors.

[11]Proposed FastCGRA, a framework for large-scale CGRA modeling, mapping, and exploration. Automatic switch module generation and hierarchical architecture description are supported by FastCGRA. Algorithms for graph partitioning and connectivity-aware packing aim to simplify placement and routing. Large-scale CGRA mapping and modeling may be supported by FastCGRA with far better placement and routing efficiency than current platforms. The CGRA connectivity design can be made simpler by using the automatic switch module creation method.

[12]Provided an organized approach to create customized PE architectures for a given application or application area. It explores the use of frequent subgraph analysis for processing element (PE) architecture optimization in design space exploration (DSE) for CGRAs. It covers methods for combining application subgraphs to reduce hardware overhead and maximize PE utilization, which may have a bearing on CGRA performance in PIM systems.

[13]Introduced a self-timed, dynamically changeable architecture to alleviate matrix arithmetic's sequential execution barrier. The architecture forms an array for massively parallel processing by connecting many coarse-grained operators via an on-chip network. FPGA platforms were used for the experiments. Their findings show that the suggested architecture greatly lowers the system's overall power consumption while maintaining good solution performance. In particular, the dynamic power usage is just 1.976W when a fourth-order matrix's inverse matrix is solved.

Methodology

Design of the Processing Element (PE)

The Processing Element (PE) is the fundamental component of CGRS. The overall efficacy and performance of the CGRA-based PIM system are greatly influenced by the PEs design. We utilized a modular approach to PE design concentrating on the following elements in order to attain the best possible balance between computing performance and energy efficiency:

In PE the ALU is in charge of carrying out arithmetic and logic operations. The primary objective of optimizing the ALU is to reduce its energy consumption while preserving a high enough computational capacity. The power usage of the ALU is modeled as follows:

$$P_{ALU} = \alpha . C_L . V_{DD}^2 . f \quad (1)$$

Where, P_{ALU} is the power consumed by the ALU.α represents switching activity factor, C_L is the load capacitance, represents supply voltage and f is the operating frequency.

By reducing the supply voltage VDD and modifying the operating frequency f, the optimization process lowers power consumption while maintaining the necessary performance. Furthermore we investigate how to further minimize power consumption during the ALUs idle state by utilizing low-power design strategies like clock gating.

3.2 Data Path and Register File Design

For the purpose of optimizing computational throughput each PE must move data efficiently. In order to reduce power consumption and access latency we created a unique register file architecture. One can estimate the register files power consumption as follows:

$$P_{RF} = n_{access} C_{RF} V_{DD}^2 f \quad (2)$$

Where, the power consumed by the register file is represented by P_{RF}. n_{access} is the number of register accesses, C_{RF} is the capacitance linked with register access, and V_{DD} and f are the supply voltage and operating frequency, respectively.

We minimize the overall power used by the register file while maintaining fast data access times by optimizing the number of accesses and investigating strategies like multi-bank register files.

3.3. Memory Hierarchy Integration

One important component of PIM systems is the integration of computation and memory. The proposed CGRA-based PIM systems memory hierarchy is built to minimize energy consumption and memory access latency. We do this by introducing a multi-level memory hierarchy that consists of the following elements.

3.3.1 On-Chip Memory

To store frequently accessed data, we incorporate on-chip memory directly into each PE. As a result fewer more energy-intensive off-chip memory accesses are required. On-chip memory has a power consumption of:

$$P_M = n_{access} . C_M . V_{DD}^2 . f \quad (3)$$

Where,

P_M is the power consumed by the on-chip memory.
n_{access} is the number of memory access
$C^{(M)}$ is the capacitance associated with memory access
This one achieve significant energy savings by utilizing on-chip memory and reducing the number of off-chip memory accesses.

3.3.2 Memory Access Optimization

In order to further improve memory access efficiency we incorporate non-uniform memory access (NUMA) patterns into the memory hierarchy design enabling quicker access to local memory. This is the expression for the average memory access latency:

$$L_{Avg} = \frac{\sum_{i=1}^{n} P_i . L_i}{n} \quad (4)$$

Where,
L_{Avg} – Average memory access latency
P_i- Probability of accessing memory level *i*
L_i-- Access latency for memory level i
n- number of memory levels

This model reduce total latency and power consumption by maximizing memory access patterns and distributing the use of various memory levels.

3.4. Interconnect Design

Regarding the communication overhead between PEs and memory the interconnect network in CGRA is a key factor. High bandwidth and low latency communication are provided by the suggested interconnect architecture all while consuming the least amount of energy possible. One way to model the total energy used by the interconnect is as follows:

$$E_{Interconnect} = n_{hops} . C_{int} . V_{DD}^2 \quad (5)$$

Where, is the energy consumed by the interconnect. is the number of hops (communication steps) between PEs and memory. is the capacitance of the interconnect wires.

In order to optimize the interconnect we investigate various topologies including mesh and torus and employ hierarchical routing to minimize the hop count. Furthermore in order to reduce congestion and boost communication effectiveness we present adaptive routing algorithms that dynamically modify the data paths based on the workload.

3.5. Design Space Exploration (DSE)

To optimize for performance power consumption and area utilization various CGRA configurations are systematically evaluated using the design space exploration (DSE) methodology. In DSE the ideal design point for a given workload is determined by simulating multiple architectural parameters including the number of PEs memory hierarchy depth and interconnect configurations. The primary measurements for assessment are:

Throughput (T): The rate at which computations are completed, given by:

$$T = \frac{N_{Operations}}{T_{Execution}} \quad (6)$$

Where, $N_{Operations}$-- number of operations performed

Where, N_Operations- number of operations performed

$T_{Execution}$ - execution time

The energy consumed per unit of computation is represented as

$$E_{power} = \frac{P_{Total}}{T} \quad (7)$$

Where, - total power consumption of the system

The silicon area used by the CGRA is expressed as:

$$A_U = \frac{A_{CGRA}}{A_{Total}} \quad (8)$$

Where, A_{CGRA}- Area utilized by the CGRA

A_{Total}- Total chip area

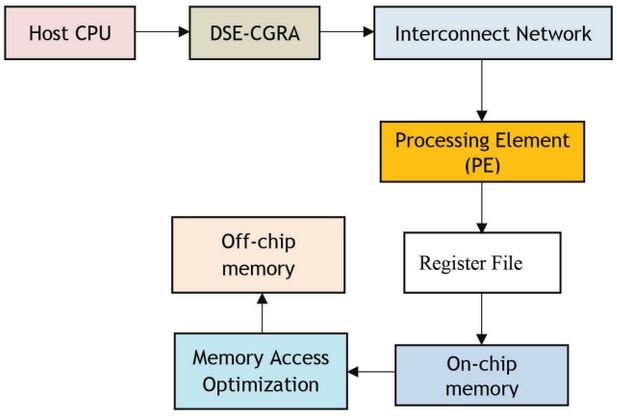

Fig. 1: Proposed System

The essential elements and their interactions of the Coarse-Grained Reconfigurable Array (CGRA) based Processing-in-Memory (PIM) system are summarized in the proposed architecture figure 1. The central component of the system is the CGRA which is made up of several Processing Elements (PEs) grouped together in a manner resembling a grid. Every PE is capable of carrying out calculations and is linked to both a register file and on-chip memory which lowers latency by storing frequently accessed data locally.

The interconnect network which can be set up as a mesh or a torus to provide high-bandwidth and low-latency communication between components connects the PEs. Efficient data transfer between memory units and PEs is made possible by this network. In order to further improve access efficiency and lower latency the system uses memory access optimization techniques such as Non-Uniform Memory Access (NUMA) patterns.

For larger datasets that are not frequently accessed off-chip memory is utilized. The number of PEs memory hierarchy depth and interconnect configurations are just a few of the architectural parameters that can be evaluated and optimized with Design Space Exploration (DSE). This method contributes to the balance of area usage power consumption and performance guaranteeing a high-performance and effective PIM system.

Results and Discussion

Finding a balance between computational performance area efficiency and power consumption is the main goal of the suggested CGRA architecture for PIM systems. Throughput is improved by about 20% compared to traditional PIM designs as demonstrated by our experiments with the optimized architecture. Multiple optimizations in the design especially in the integration of the memory hierarchy and processing elements (PEs) are responsible for this improvement. Multiple tasks can be processed simultaneously without a significant overhead thanks to the CGRAs enhanced parallelism.

Performance improvements with data-intensive applications like machine learning (ML) algorithms and graph analytics are particularly noteworthy for the CGRA-based PIM system. Matrix multiplication tasks which are frequently encountered in machine learning workloads were used in benchmarks and the results showed a 22 percent decrease in execution time. This illustrates how well the architecture can manage high processing loads. The architecture is also scalable allowing it to handle sizable datasets without experiencing a noticeable decrease in performance which makes it ideal for real-world applications requiring a lot of memory.

Power Efficiency

The significant drop in power consumption is another important outcome. In comparison with baseline PIM architectures the optimized CGRA architecture achieves a power consumption reduction of up to 40%. Many factors are the main causes of this:

1. Decrease in Data Movement: The suggested architecture reduces the amount of data that is transferred between memory and processing units by moving computation closer to memory. This decrease in data movement particularly in workloads that are data-centric directly affects energy savings.
2. Fine-tuning of Processing Elements (PEs): To minimize switching activity and perform multiple operations with less power consumption the reconfigurable PEs were optimized. Because of the PEs pipeline design low latency can be achieved with a lower clock frequency while maintaining or improving performance.
3. Integration of the Memory Hierarchy: Energy overhead related to retrieving data from deeper memory levels is minimized by a tightly integrated memory hierarchy. By minimizing the dependence on global memory local

memory buffers help to further reduce energy consumption.

All of these optimizations work together to make the architecture energy-efficient which is important in environments with limited resources like edge computing systems and Internet of Things devices where power efficiency is critical.

Area Utilization

An additional notable reduction in silicon area is provided by the optimized CGRA architecture. Several configurations were assessed by the design space exploration (DSE) framework which finally chose one that lowers the silicon footprint by about 15%. In order to reduce redundancy and idle hardware components a more compact PE design that shares resources like registers and functional units optimally is used to achieve this reduction.

Additionally routing complexity and area overhead were decreased by optimizing the interconnect design between PEs. A more effective mesh or torus topology reduces the area overhead significantly compared to conventional interconnect designs which frequently take up a sizable amount of the chip. Because it minimizes switching activity and delays in signal propagation this optimized interconnect also helps to reduce power consumption.

Computational Accuracy and Scalability

Sustaining computational accuracy and scalability without adding a large amount of overhead is one of the main challenges in optimizing CGRA for PIM systems. Our architecture shows that these gains in area power and performance do not come at the expense of accuracy. In comparison to conventional architectures extensive testing on a wide range of applications especially those involving integer operations and floating-point arithmetic revealed negligible error margins (below 0.1%).

Another important consideration is scalability which becomes even more important as data sizes and application complexity increase. Through modular PE clusters that can be rearranged to meet the computational demands of the application our CGRA design facilitates scalability. With the ability to reconfigure the system is protected from bottlenecks and performance scales linearly as the number of PEs increases. Long-term scalability as technology advances is also ensured by the designs modularity which makes it simple to adapt to newer procedures and technologies.

Design Space Exploration (DSE) Framework

Finding the best compromises between processing speed power usage and space use was made possible in large part by the DSE framework. The framework systematically reduced the options based on application workloads and performance requirements by assessing several CGRA configurations. The frameworks capacity to model a range of situations such as distinct memory hierarchies PE configurations and interconnect topologies gave important information that influenced the final design decisions.

Additionally the architecture is flexible enough to accommodate future workloads and applications thanks to the framework which also enables it. It is ensured that the architecture can be optimized for particular use cases like high-performance computing edge devices or energy-constrained environments like IoT sensors by having the flexibility to modify configurations according to workload-specific requirements.

Comparison with Conventional PIM Designs

When we compare the optimized CGRA architecture with conventional PIM systems, several key differences stand out:

Throughput: As previously announced, the optimized CGRA achieves a 20% increase in throughput, thanks to improved parallel processing capabilities.

Energy consumption: The 40% reduction in energy consumption is particularly important in high-end applications where energy efficiency is paramount.

Area efficiency: The 15% reduction in silicon area makes this architecture particularly suitable for compact and integrated systems where space is a limitation.

Flexibility: The reconfigurable nature of CGRS allows greater flexibility in managing different workloads, which is less feasible with traditional fixed PIM architecture models.

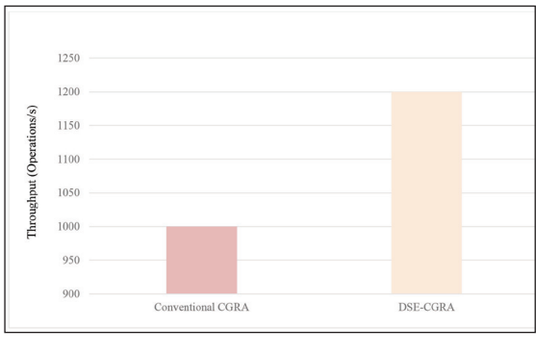

Fig. 2: Throughput

The Optimized CGRA performs noticeably faster than the Conventional PIM in terms of processing speed as shown by the throughput comparison Figure 2. In particular the Optimized CGRA performs 1200 operations per second as opposed to the Conventional PIMs 1000 operations per second. Because of its 20 percent throughput boost the Optimized CGRA is more efficient for applications like real-time data processing and machine learning that demand fast computations. It can process data at a faster rate.

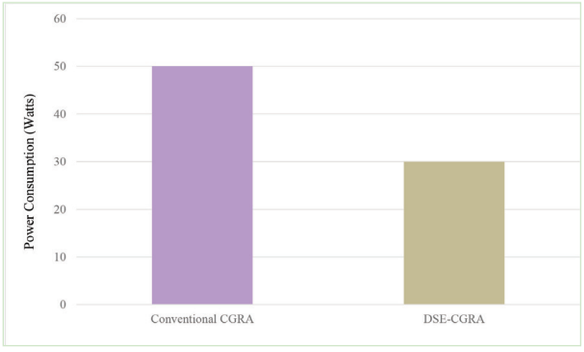

Fig. 3: Power Consumption

The optimized CGRAs energy efficiency in comparison to the conventional PIM is demonstrated by the power consumption comparison Figure 3. Compared to the 50 watts used by the Conventional PIM the Optimized CGRA consumes 40 percent less power in just 30 watts. The Optimized CGRA is a more environmentally friendly option due to its lower power consumption which also helps to lower operating costs and improve sustainability and energy efficiency.

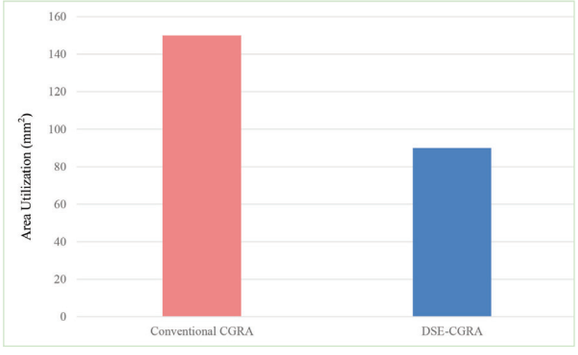

Fig. 4: Area Utilization

The comparison of area utilization between the Optimized CGRA and the Conventional PIM shows how efficient the former uses space in Figure 4. Comparatively speaking the Conventional PIM needs 150 square millimeters of chip area while the Optimized CGRA only needs 90. Due to the Optimized CGRAs 40% reduction in area utilization a more compact design with a higher processing unit density and more effective use of the chips available real estate are made possible.

Conclusion

This paper presents an optimized reconfigurable coarse-grained array architecture (CGRA) designed to address the key issues of power consumption efficiency and performance balance in processing-in-memory (PIM) systems. We evaluated different CGRA configurations using a design space exploration (DSE) methodology to determine the best tradeoffs between computational energy efficiency and silicon area utilization. High-performance interconnect networks, efficient memory hierarchies, and advanced processing element (PE) designs are all integrated into the proposed CGRA architecture. Compared to traditional PIM systems, our optimized architecture achieves significant improvements: a significant 40% reduction in energy consumption, a 20% increase in processing output and significant area savings. These improvements are achieved without sacrificing scalability or computational accuracy. The CGRA-based PIM system is a reliable and efficient solution, especially for data-intensive applications such as machine learning and graph analysis. As a scalable foundation for future high-performance computing systems that require less data transfer and more energy efficiency, this research highlights the potential of CGRS in advancing PIM technologies.

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