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Research Article

Analysis of Reliability for Flash Type Analog to Digital Converter

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ABSTRACT
Analog to digital converters plays a prominent role in the all the electronic devices to convert the continuous data in to digital data. During the conversion of the data a wide number techniques as already developed such as wallc tree, Fat tree etc. In this paper we proposed a novel 3-bit encoder which is produce the results with the high speed and less power dissipation respectively.

Keywords: digital converter

Introduction

A to D converters plays a one of the prominent role in the current day high end electronic systems. These can be acts as the functional blocks many of the current day applications such as system on chip(SOC),data conversion, signal processing, mixed signal design etc. already we have a multiple number of the A to D architectures are available like flash type A to D, ramp type, comparator type, successive approximate type etc. number of architectures are available. Figure 1 indicates the conventional type of A to D architecture.

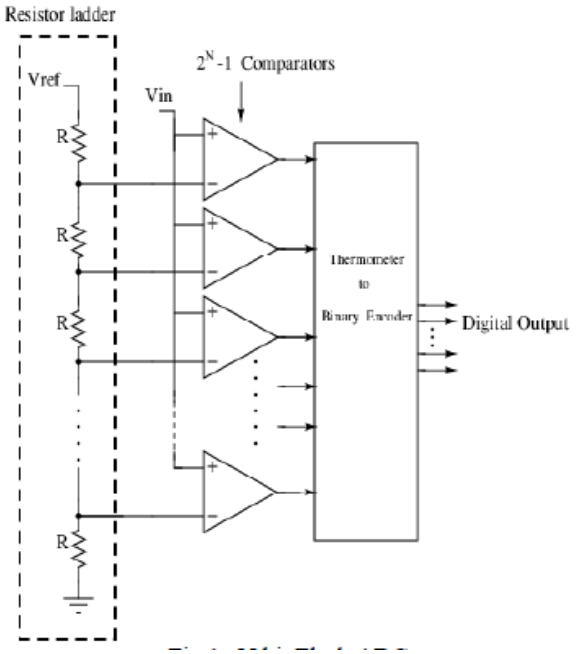

Fig:1

The flash type converts the Analog input (continuous in amplitude and continuous in time) and it finally converts the in to digital value(either 0 or 1) respectively.

The rest of the paper is organised as follows: section 2 introduces the basic information different types of encoders, proposed 3 bit encoder respectively.

Background

Various types of encoders are already available such as wallc tree encoder, multiplexer type encoder, fast tree type encoder etc. these types of encoders are quit commonly used in the different types of A to D

converters in order to convert the Analog data in to digital data[1-3].

Wallc tree multiplier

It is one type of encoder which basically counts the number of 0s and 1s. Figure 2 shows the wallc tree encoder[4-8]. This type of topology can be can be used in the A to D converters and major disadvantage of the technique could be large delay and more power dissipation.

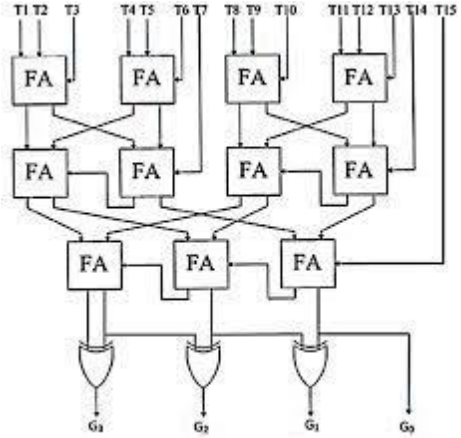

Fig.2: Wallace tree encoder.

Fat-Tree Based Encoder

Fat tree encoder has the less delay and area when compared to the conventional ROM type encoder and Wallace type encoder. Figure 3 depicts the 15 to4 bit fat tree encoder respectively[9-10].

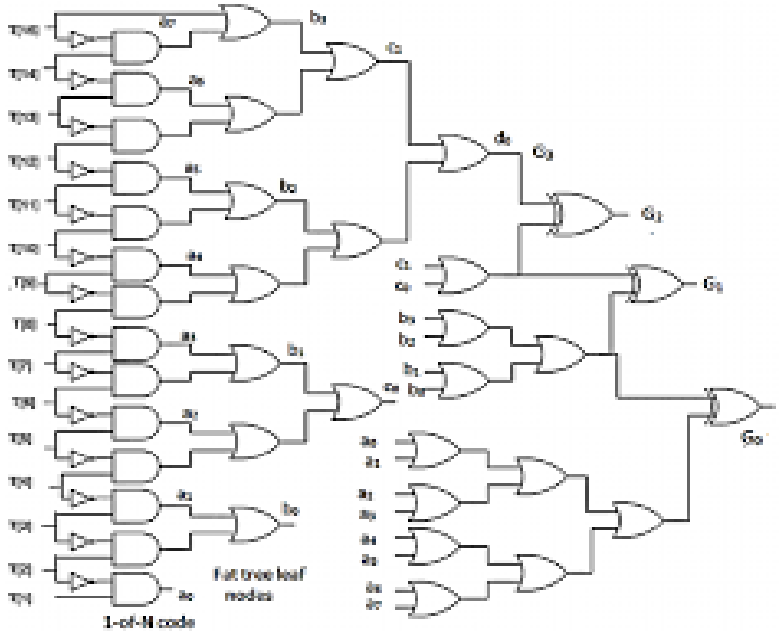

Fig.3: Fat tree encoder.

Proposed Encoder

The proposed architecture using the 3 bit encoder as shown in figure 4. And it can be designed using the set of multiplexers. The proposed architecture consists of the three multiplexer designed using the CMOS technology. Table 1 indicates the compression of the existed architecture with the different types of the architectures respectively.

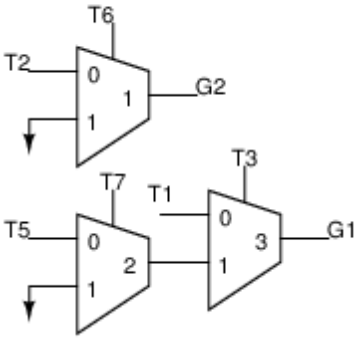

Fig.4: proposed 3 bit encoder.

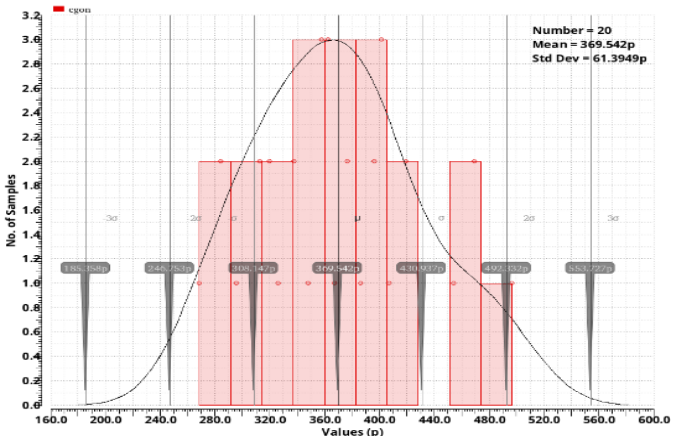

Fig.5: Reliability of encoder over 2K samples.

The proposed encoder variations were measured over the range of -20C to 80C. The variation of the delay can be observed by applying the statistical analysis. From the obtained results it indicates the mean could be 369.542p and standard deviation is the 61.394p respectively.

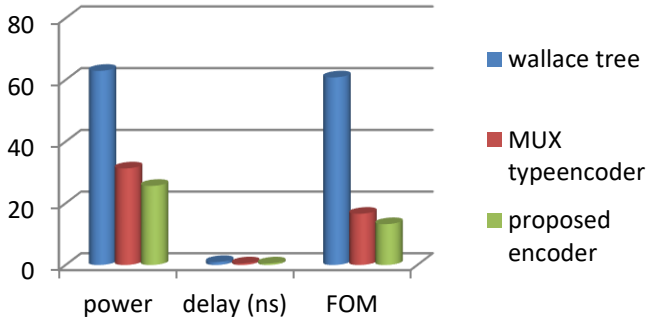

Fig:6

Comparison of proposed encoder with existed structure

Conclusion

The novel mux based encoder is proposed in this paper and which can be used to reduce the delay and power. It can be perfectly suitable for the different types of the Analog to digital converters. This type of the encoder can also be suitable for the communication and other set of the protocols respectively.

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