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# Design of a optimized CMOS Differential Amplifier using Craziness-based PSO

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## Abstract

Particle swarm optimization (PSO) is a computational method used for solving different types of optimization problems. The social behaviors of fish schooling and flocks of birds mostly influence the PSO. PSO uses a collection of particles to explore the search space and locate the best possible solution.Each particle updates its position depending upon experience of itself or from neighboring particles, aiming to find the best solution in terms of the objective function being optimized.Crazinessbased Particle Swarm Optimization (CRPSO) is an advanced variation of the standard Particle Swarm Optimization (PSO) algorithm.CRPSO introduces a “craziness” factor to enhance the diversity of the swarm and prevent premature convergence to local optima.This paper deals with the design of a CMOS differential amplifier circuit with a current mirror load using CRPSO algorithm. The optimized sizes of the transistors are obtained using CRPSO to decrease the overall transistor area while meeting design limitations. The results achieved using the CRPSO are validated in the SPICE. The simulation result shows the superiority of CRPSO in the design of differential amplifier.

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## Introduction

Manual circuit sizing relies on human designers leveraging their expertise, experience, and intuition to determine the optimal sizes for transistors and other components in a VLSI circuit. This approach is suitable for small to medium-sized designs or situations where specific expert knowledge is critical. However, manual sizing can be extremely time-consuming, especially for large and complex circuits.Automated sizing of VLSI circuits is a vital part of the design process, aiming to optimize the dimensions of transistors and other components to meet performance criteria such as area and power consumption. This involves finding the optimal widths and lengths of transistors to achieve desired performance while adhering to design constraints. Automated circuit sizing is ideal for large-scale and complex designs, offering efficiency, consistency, and global optimization. Although it requires significant setup and computational resources, it can achieve superior results by systematically exploring the design space. Automation is particularly essential in analog circuit design to overcome the challenges inherent in manual design.

Various approaches have been explored to automate analog circuit design, as reported in.[1-2] Different optimization technique, such as genetic algorithms,[3-4] Particle Swarm Optimization (PSO),[5-6] craziness-based PSO (CRPSO),[7] MDEA optimization,[8] and the cat swarm optimization algorithm,[9] have been utilized for analog circuit sizing problems. Optimal component values for low-pass filters have been determined using tabu search (TS),[10] differential evolution (DE),[11] average DE (ADE) ,[12] and PSO with Aging Leader and Challenger (ALC-PSO).[13] Additionally, Partition Bound PSO (PB-PSO)[14] and hybrid PSO[15] have been applied for the optimal design of differential amplifiers. The primary contributions

of this paper include optimizing transistor size and designing amplifiers with enhanced performance parameters compared to previously reported techniques. The optimization technique employed here is CRPSO.[16-17]

## Particle Swarm Optimization

PSO[18-19] is a traditional optimization method. It involves a swarm of particles for optimization. Each particle has a position and velocity. The position and velocity updates are governed by the following equations:

$$V_i^{(k+1)} = w * V_i^{(k)} + C_1 * rand_1 * \left(pbest_i^{(k)} - S_i^{(k)}\right) + C_2 * rand_2 * \left(gbest^{(k)} - S_i^{(k)}\right) \quad (1)$$

$$S_i^{(k+1)} = S_i^{(k)} + V_i^{(k+1)} \quad (2)$$

The detailed description of the above-mentioned parameters are given in.[18-19]

## Craziness based Particle Swarm Optimization

Conventional PSO is altered by introducing a "craziness velocity". This modified PSO is termed as CRPSO. The velocity expression can be expressed as follows:[16-17]

$$V_i^{(k+1)} = r_2 \times sign(r_3) \times V_i^{(k)} + (1-r_2) \times C_1 \times r_1 \times \left\{pbest_i^{(k)} - S_i^{(k)}\right\} + (1-r_2) \times C_2 \times (1-r_1) \times \left\{gbest^{(k)} - S_i^{(k)}\right\} \quad (3)$$

where $r_1$, $r_2$ and $r_3$ are within the interval [0,1], and sign ($r_3$) is a function defined as:

$$sign(r_3) = -1 \quad \text{where} \quad r_3 \le 0.5$$
$$= 1 \quad \text{where} \quad r_3 > 0.05 \quad (4)$$

The velocity of the particle is crazed by,

$$V_i^{(k+1)} = V_i^{(k+1)} + P(r_4) \times sign(r_4) \times v_i^{craziness} \quad (5)$$

where $r_4$ is a random parameter within the interval [0,1]; $v_i^{craziness}$ is a random parameter, $P(r_4)$ and $sign(r_4)$ are given in.[7] The flowchart for CRPSO algorithm is given in Fig. 1. The important CRPSO algorithm Parameters is presented in Table 1.

**TABLE 1: Average power CRPSO algorithm parameters**

| Parameters | CRPSO |
|---|---|
| Population Size (m) | 10 |
| Dimension of the optimization problem (n) | 7 |
| Iteration Cycle | 100 |
| $C_1$ | 2 |
| $C_2$ | 2 |
| Pcr | 0.3 |
| $v_{craziness}$ | 0.0001 |

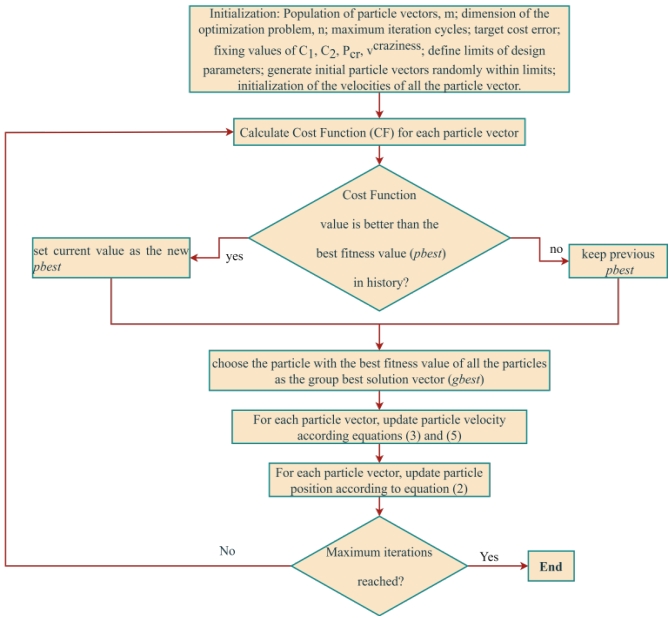


FIG. : Flowchart of CRPSO algorithm

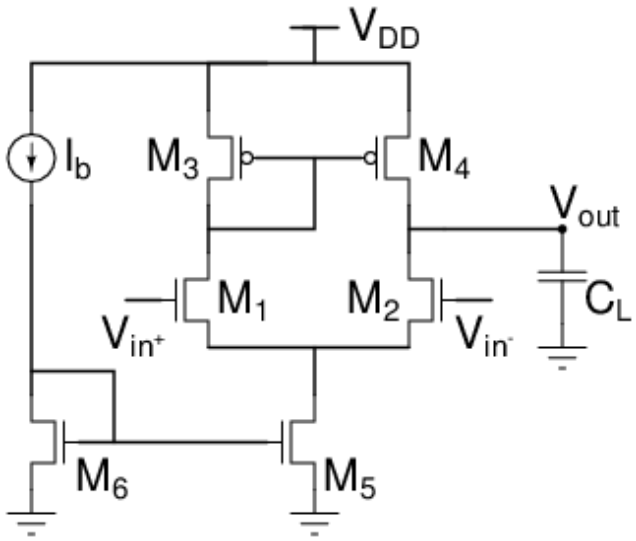


FIG. 2: CMOS differential amplifier circuit with a current mirror load

## Problem Formulation of Differential Amplifier circuit

The circuit diagram of the CMOS differential amplifier circuit with current mirror load is shown in Fig. 2. The important performance parameters for the design of CMOS differential amplifier are considered as follows: SR (Slew rate), gain ($A_v$), unity gain frequency (UGF), $V_{IC(max)}$ (maximum ICMR), $V_{IC(min)}$ (minimum ICMR), power dissipation ($P_{diss}$), and total transistor area. The performance parameters are presented in Table 2. The design variables are as follows: bias current ($I_b$), width ($W$) and length ($L$) of each transistors, and load capacitance ($C_L$). The design steps [20] for the differential amplifier circuit are given in Table 3. The main objective of the design is to minimize the total transistor area.

**TABLE 2: Design specifications of differential amplifier**

| Design parameter | Unit | Values |
|---|---|---|
| Technology | nm | 180 |
| Av | dB | > 39 |
| PM | ° | > 45 |
| UGF | MHz | > 5 |
| CMRR | dB | > 50 |
| PSRR | dB | > 35 |
| SR | V/μS | >5 |
| $V_{IC(min)}$ | V | > 0.4 |
| $V_{IC(max)}$ | V | < 1.5 |
| $P_{diss}$ | μW | < 1000 |
| Total transistor area | μm2 | < 1500 |

**TABLE3:Design step of CMOS differential amplifier circuit**

- ☐ Define $I_{D5}$ to meet SR.
- ☐ Design for $\left(\frac{W_1}{L_1}\right)$ and $\left(\frac{W_2}{L_2}\right)$ to satisfy $A_V$.
- ☐ Design for $\left(\frac{W_3}{L_3}\right)$ and $\left(\frac{W_4}{L_4}\right)$ to validate the upper ICMR.
- ☐ Design for $\left(\frac{W_5}{L_5}\right)$ and $\left(\frac{W_6}{L_6}\right)$ to validate the lower ICMR.
- ☐ Determine $I_{D5}$ to satisfy $P_{diss}$.

The dimensions of particle vectors ($X_{diffamp}$) are described as

$$X_{diffamp} = [P_{diss}, C_L, A_v, SR, UGF, VK_{(min)}, K_{(max)}, TTA]^t$$

The cost-function (CF) is described as

$$CF = \sum_{i=1}^{6} (W_i \times L_i) \qquad (6)$$

## Simulation Results

The CMOS differential amplifier is designed with the help of CRPSO. The optimized value of all design variable such as $I_b$, $W$, $L$ are obtained by using CRPSO in MATLAB. The upper and lower bound of these design variables and the obtained values using CRPSO are presented in Table 4. SPICE simulation is performed for the differential amplifier designed in Cadence virtuoso analog environment using UMC 180 nm technology.

The voltage gain vs frequency plot of the differential amplifier is depicted in Fig. 3. The gain and cut-off frequency of the differential amplifier is 45.96 dB and 9.75 MHz, respectively. The phase vs frequency plot of the differential amplifier is depicted in Fig. 4. The simulated phase margin of the amplifier is 78.28°.

**TABLE4: Optimal design parameters obtained from CRPSO**

| Parameter | Lower bound - Upper bound | Obtained value using CRPSO |
|---|---|---|
| $W_1 = W_2$ | 240 nm - 30 μm | 907.4 nm |
| $W_3 = W_4$ | 240 nm - 30 μm | 1.78 μm |
| $W_5 = W_6$ | 240 nm - 30 μm | 2.8 μm |
| $L$ | 3.5 μm | 3.5 μm |
| $I_b$ | 3.5 μA - 30 μA | 4.8 μA |
| $C_L$ | 0.5 pF | 0.5 pF |

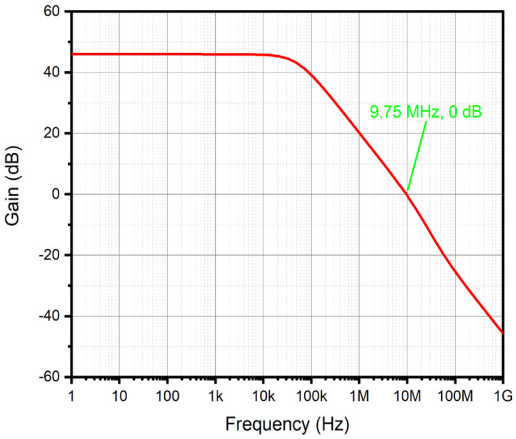


**FIG. 3Gain plot of differential amplifier circuit**

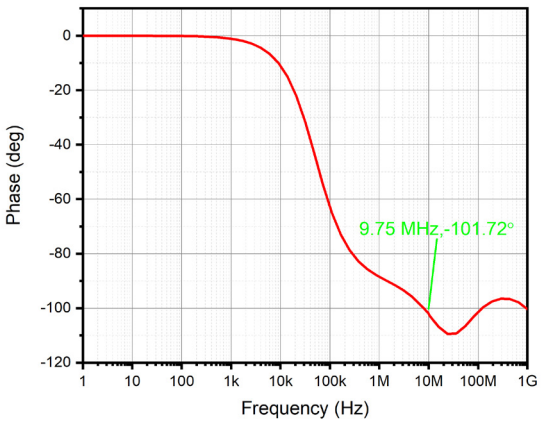


**FIG. 4: Phase plot of differential amplifier circuit**

The simulated common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) plot of differential amplifier is shown in Fig. 5 and Fig. 6, respectively. The PSRR and CMRR of the differential amplifier are 44.75 dB and 73.76 dB, respectively. From Fig. 7, the computed value of SR is 7.74 V/μS. The simulated results for differential amplifier is shown in Table 5 and compared with[14] and. [21] The simulated result of the designed differential amplifier using CRPSO shows better results in terms of voltage gain, phase margin, CMRR, PSRR, Power dissipation and total transistor area. The UGF and SR of the designed differential amplifier is less than the, [14,21],

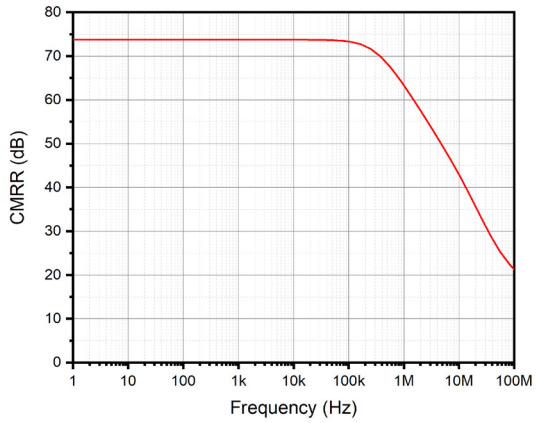


**FIG. 5: CMRR plot of differential amplifier circuit**

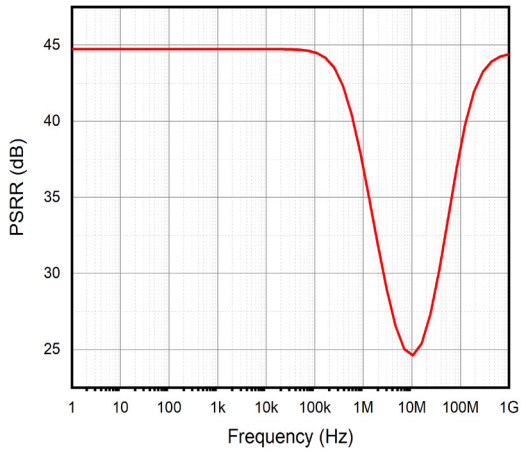


**FIG. 6: PSRR plot of differential amplifier circuit**

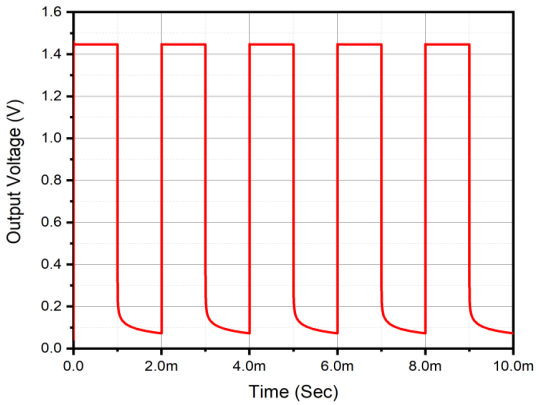


**FIG. 7: SR plot of differential amplifier circuit**

but it is as per the design specification. The $V_{IC(max)}$ and $V_{IC(min)}$ of the differential amplifier is 0.55 V and 1.4 V respectively. The gain of the designed amplifier is increased almost by 17% as compared to.[21]. The power dissipation and total transistor area of the designed amplifier is reduced by 61% and 85% as compared to.[14] The simulated results reported in Table 5 confirms the efficacy of the CRPSO in the differential amplifier design.

**TABLE 5: Simulated result of differential amplifier**

| *Design parameter* | *Unit* | *[14]* | *[21]* | *This work* |
|---|---|---|---|---|
| *Technology* | *nm* | *180* | *180* | *180* |
| *Av* | *dB* | *40.59* | *39.35* | *45.96* |
| *PM* | ° | *47.68* | *53.5* | *78.28* |
| UGF | MHz | 25.23 | 21.70 | 9.75 |
| CMRR | dB | 70 | 56 | 73.76 |
| PSRR | dB | 41.31 | 41.36 | 44.75 |
| SR | V/μS | 22 | 18 | 7.74 |
| $P_{diss}$ | μW | *45* | *50* | *17.28* |
| *Total transistor area* | $\mu m^2$ | *249* | *195.85* | *38.81* |

The simulation of differential amplifier is carried out against change in process, voltage and temperature (PVT) variations. The PVT variation results of the differential amplifier are presented in Table 6-8. The process variation of the design is done at slow-slow (SS), fast-fast (FF), typical-typical (TT), slow NMOS-fast PMOS (SNFP), fast NMOS-slow PMOS (FNSP). The temperature variation of the design is done at -4°¤ - 125 ¤ and supply voltage is varied by maximum 10% from the standard supply voltage of 1.8 V. From Table 6-8, it is evident that all the performance parameters satisfy the design constraint.

**TABLE 6: Process corner analysis of differential amplifier**

| Process | | SS | SNFP | TT | FNSP | FF |
|---|---|---|---|---|---|---|
| **Specification** | **Unit** | | | | | |
| $A_v$ | *dB* | *46.4* | *45.95* | *45.9* | *45.92* | *45.5* |
| *PM* | ° | *78.75* | *78.54* | *78.2* | *78.01* | *77.9* |
| *UGF* | *MHz* | *8.49* | *9.74* | *9.75* | *9.75* | 11.1 |
| CMRR | dB | 73.25 | 69.71 | 73.7 | 76.41 | 73.7 |
| PSRR | dB | 45.1 | 44.48 | 44.7 | 44.89 | 44.3 |
| SR | V/μS | 6.39 | 7.98 | 7.74 | *7.48* | *9.33* |
| $P_{diss}$ | μW | *14.09* | *17.81* | *17.3* | *16.77* | *21* |

**TABLE 7: Temperature variation analysis of differential amplifier**

| Temperature | | -40 ¤ | 27 ¤ | 125 ¤ |
|---|---|---|---|---|
| **Specification** | **Unit** | | | |
| $A_v$ | dB | 46.35 | *45.96* | *45.16* |
| *PM* | ° | *77.6* | *78.28* | *79.12* |
| *UGF* | *MHz* | *12* | *9.75* | *7.88* |
| *CMRR* | *dB* | *76.39* | *73.76* | *67.92* |
| *PSRR* | *dB* | *45.33* | *44.75* | *43.58* |
| *SR* | *V/μS* | *8.16* | *7.74* | *7.67* |
| $P_{diss}$ | μW | *17.82* | *17.28* | *17.04* |

**TABLE8:Supply voltage variation analysis of differential amplifier**

| Supply Voltage | | 1.62 V | 1.8 V | 1.98 V |
|---|---|---|---|---|
| Specification | Unit | | | |
| Av | dB | 45.8 | 45.96 | 45.84 |
| PM | ° | 78.5 | 78.28 | 78.13 |
| UGF | MHz | 8.19 | 9.75 | 11.22 |
| CMRR | dB | 79.95 | 73.76 | 62.63 |
| PSRR | dB | 44.7 | 44.75 | 44.75 |
| SR | V/μS | 5.35 | 7.74 | 10.32 |
| $P_{diss}$ | μW | 10.83 | 17.28 | 25.57 |

## Conclusion

In this study, the CRPSO is used to construct a CMOS differential amplifier circuit. CRPSO is efficient at determining the optimal size of all transistors. The circuit is developed in Cadence to meet the performance requirements. Compared to earlier literature, CRPSO produces better results regarding gain, power dissipation, and area. CRPSO can produce a nearly global optimal analog circuit design. The CRPSO can be used to design more complex analog circuits.

## Conflict of Interest

The authors of this paper like to state that they have no conflicts of interest related to this work with other published works in similar domain as far best of their knowledge.

## Author Contributions

The research work is original in nature and carried out by Sandeep Kumar Dash and Bishnu Prasad De. Bhargav Appasani helped in revising the work. Nirmal Kumar Rout and Avireni Srinivasulusupervised the research.

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