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High Speed Energy Efficient Latch Architectures for Sequential Circuit Design

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Abstract

As per the escalating demand for portable and battery-powered electronic devices, the requirement of energy-efficient, high-speed devices with minimal area has become increasingly imperative in this era of sustainable electronics and green computing. Latches serve as fundamental elements essential for the operation of sequential circuits in Internet of Things (IoT), Edge computing, and high-performance processors. The bulk of on-chip elements in a processor is often composed of sequential parts such as memory, registers, counters and flip-flops, wherein the foundational component is a data latch. This research paper puts forward two level sensitive latch energy-efficient designs using 6 transistors and 5 transistors respectively. The proposed designs are assessed under multiple supply voltages and temperatures. Additionally, corner analysis and Monte Carlo analysis are conducted on the proposed latch designs to validate their robustness and stability, ensuring their sustainability and ability to withstand high error rate at different operating conditions. The results confirm reduced energy consumption, delay and output noise with improved performance of the latches with an improvement of PDP by 10 folds and the delay is reduced by a factor of 10^{-2} with an area occupancy of 5.6024 μm^2 and 4.7183 μm^2 for the two proposed designs. Also, a 3-bit shift register is designed with the proposed design to demonstrate the successful application of these designs.

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Introduction

In order to ensure optimal battery life and reliability[1] for realtime portable applications, it is crucial to minimise energy consumption, delay as well as area of any device. By utilizing a smaller number of transistors, it is possible to reduce parasitic capacitances, chip area, propagation delay, and power consumption. One of the fundamental building blocks for a sequential circuit is latch. These are level-sensitive devices which are used for data storage, synchronization and performance optimization. These devices hold their state when disabled and are transparent when enable signal is active leading to reduced dynamic power dissipation as unnecessary toggling is avoided. Latches find use in pipeline stages, register files, clock gating circuits and memory elements in modern digital systems and microprocessors.[2] Modern clock-gating techniques employ latches to selectively disable inactive sections of a circuit, further minimizing power usage[3] by combining with flip-flops in synchronization circuits. High speed circuits employ pipelined latch circuits or master-slave latch configurations for minimal timing overhead with high-performance operation. A flip-flop can be built using two latches in a master-slave configuration and improve circuit performance through time borrowing and reduced power dissipation.

This paper proposes two designs of D-latch with reduced transistor count, and improved performance. The simulation results are produced with Cadence Virtuoso at 45nm technology node. The standard simulation metrics are set at a supply voltage of 1V and room temperature of 27°C. The analysis encompasses various

critical performance parameters, such as propagation delay, Power-Delay Product (PDP), Energy-Delay-Product (EDP), output noise, noise gain, and chip area. Reliability and robustness of the two proposed D-latch are confirmed by conducting additional evaluations including Monte Carlo and corner analyses, addressing variations in process, voltage, and temperature. These comprehensive assessments are applied to validate the performance and stability of the proposed designs under diverse operating conditions.

The forthcoming section of this research paper will present an overlook of current research on D-latches and the identified recent competing Latch design. The next section presents the two proposed design description followed by the detailed analysis of various performance parameters for the proposed designs as well as the identified competing design followed by an evaluation of the reliability and robustness of the proposed novel D-latches. Lastly, as an application of the proposed design, a 3-bit shift register is implemented before concluding the study.

Literature Review

The focus of early research was to improve area efficiency and power-saving capabilities, which has been accompanied by timing uncertainty, low power requirements, noise immunity, clock skew, and race conditions lately.[2, 4] Master-slave configuration, pulsed latches,[5] and adaptive latch timing techniques is known to address these issues for improved robustness and performance of digital circuits. Moreover, studies on clock domain synchronization have demonstrated the importance of latches in reducing metastability risks, particularly in asynchronous and multi-clock environments.

This review section examines the evolution of latch-based circuits. The existing work in[6] presents a pre-layout simulation of a D-latch. This design demonstrated a significant reduction in propagation delay and Power Delay Product (PDP). It also exhibited a reduced clock load. Han-Yeol Lee introduced a TSPC flip-flop in[7] which utilized three feedback circuits made up of gated inverters. Simulation results revealed that the introduced flip-flop assured error-free operation at low frequencies. However, due to inclusion of three feedback circuits, an increase in power consumption is observed. A Soft Error Hardened D-latch is presented in[8] with a focus on immunity. Based on performance metrics including power consumption, delay, and Power-Delay Product (PDP) under different frequencies, voltages, temperatures, and process variations their design showed improved delay and PDP. Additionally, the standard deviation of delay due to threshold voltage variability was also improved. The work presented in[9] introduced an SCL-based D latch, which offered an understanding of the power-delay trade-offs involved in its design. The study also discussed the dependence of delay on logic swing, which revealed that reducing the logic swing does not necessarily decrease delay[10] stated that this study considered two existing latch architectures, the 4T and 5T D-latches, with a concentration on reducing leakage current. This paper introduced an enhanced configuration using LECTOR, which effectively reduces static power dissipation. There are various approaches to designing D-latches. A comparison of different D-latch topologies including conventional Complementary Metal Oxide Semiconductor (CMOS), MOS Current Mode Logic, and Bulk Driven-MOS Current Mode Logic is presented in.[11]

For improved speed as the objective, a D-latch architecture with N-parallel discharge paths is presented in.[12] These parallel paths enable faster discharge of the load capacitor by increasing the effective current at output node. The approach is novel but the simulations are performed in 180 nm and voltages as high as 1.8 V, which is quite a higher technology node and voltages as per today's scenario.

Pulsed latch combining the latches with flip-flops with transmission gate design method is analyzed for Voltage and Temperature variations in.[5]. The pulsed latches offer low timing overhead and power consumption as compared to flip-flops because they are driven by short pulses generated by a pulser circuit from a conventional clock signal.

Existing 7T latch architecture

The two proposed designs attempt to improve the existing existing latch setup presented in [10], which uses two transistors named 'M5' and 'M6' working together to reduce leakage, as shown in Figure 1. The Leakage Controlled Transistors (LCTs) are designed with two control points, 'a' and 'b', allowing them to operate in different modes. When the clock signal 'Clk' is active high, new input data 'D' is accepted, and when 'Clk' is active low, 'D' is stored safely between M2, M4, M5, M6, and M7 without any static electricity build-up. This avoids the risk of a short circuit occurring between the power supply (Vdd) and ground when the signals 'x' and 'y' fluctuate. The use of Leakage Controlled Transistors (LCTs) with multiple control nodes may introduce additional points of failure or design challenges. Moreover, it may also introduce additional power consumption

or delay in signal propagation. Finally, the reliance on clock signals for data input and storage may impose timing constraints on the system, perhaps limiting its overall speed or efficiency. This design doesnot provide with complementary signal at output. To produce the complemented output Qbar, a CMOS inverter, that is, 2 more transistors will be required, making the transistor count as 9 for the existing design.

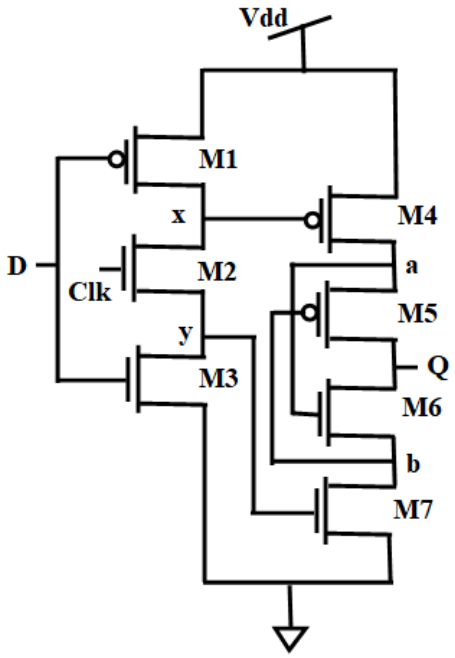


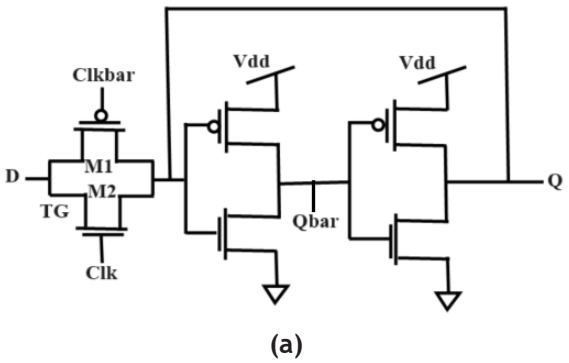
Fig. 1: Circuit diagram of existing 7T latch design

Proposed 6T Latch Architecture

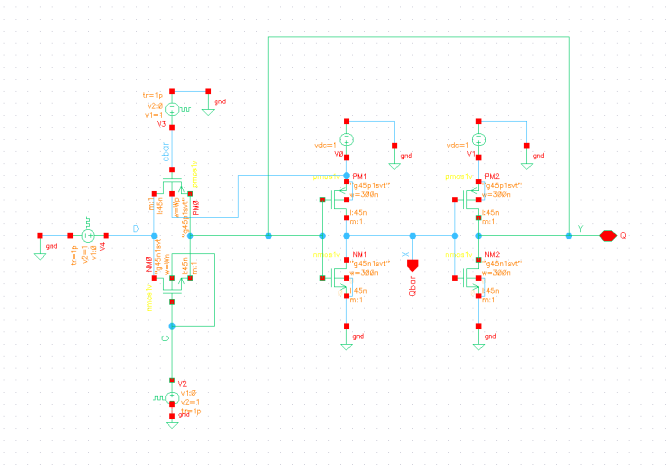
Proposed 6T Latch architecture

The first proposed latch design incorporates a single transmission gate and two CMOS inverters. This reduces the transistor count for the latch to 6 as compared to 7 required for the existing latch in [10]. With three PMOS and three NMOS transistors, the proposed latch design, referred to as 6T latch, later in this paper, the design saves silicon area of 1 transistor, enabling denser integration of components and potentially reducing overall chip size. It functions as a positive level sensitive latch and the use of cascaded inverters and a transmission gate in this latch design can enhance stability and noise immunity, which may lead to more robust operation in practical applications. The architectural layout and schematic representation of the proposed 6T latch are depicted in Figure 2(a) and Figure 2(b) respectively.

The simulated input-output waveforms of the proposed 6T latch are shown in Figure 3 showing the true and complementary output obtained with 1V signal. The level triggered latch is able to track the changes in data readily without loss.



(a)



(b)

Fig. 2: Circuit diagram of proposed 6T latch design (a) architecture (b) schematic representation

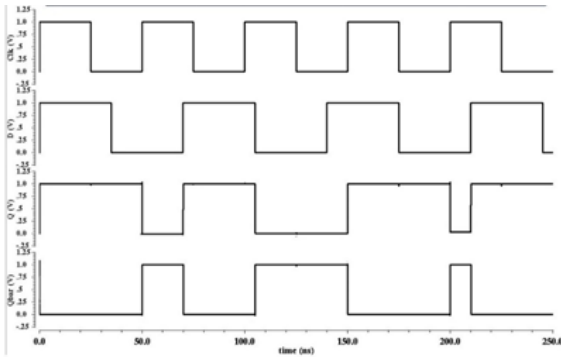
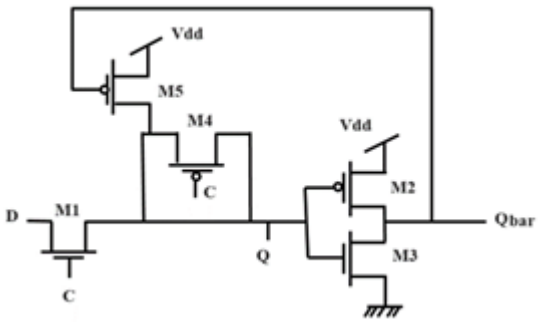


Fig. 3: Input-Output waveforms of proposed 6T latch design

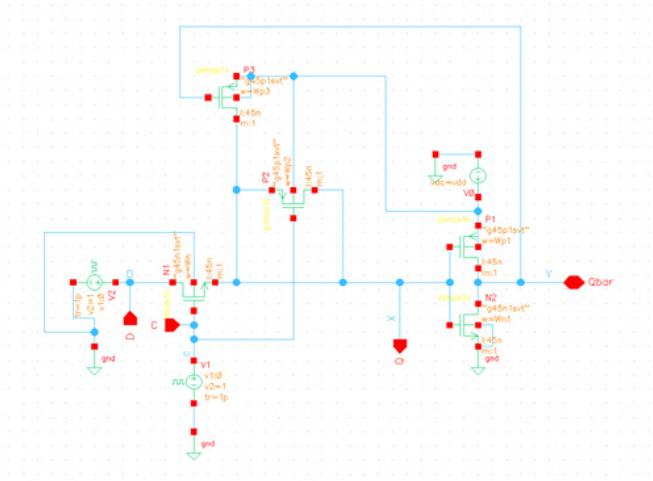
Proposed 5T latch architecture

The second design for D-latch requires even reduced area. This design consists of three pass transistors and a CMOS inverter, adding up to five transistors in the circuit. The second design is referred to as 5T latch in this paper. The pass transistor M1 facilitates the passage of data, 'D' to the output node Q exclusively when the clock signal, denoted as clk, is at logic '1'. Transistors M2 and M3 are employed to configure a CMOS inverter, while pass transistor M4 provides feedback when

clock signal, clk, is at logic '0', ensuring the output remains unchanged during the negative phase of the clock cycle. Lastly, transistor M5 functions as a pull-up transistor, aiding in restoring the output 'Q' to provide complete logic '1' or Vdd. With only five transistors, it requires fewer components compared existing 7T latch configuration, simplifying the circuitry and possibly reducing manufacturing costs.



(a)



(b)

Fig. 4: Circuit diagram of proposed 5T latch design (a) architecture (b) schematic representation

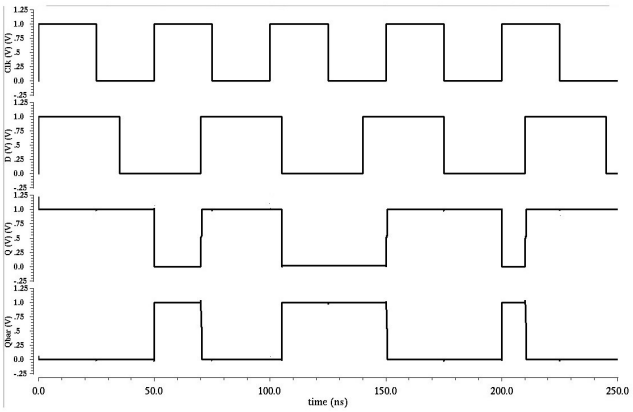


Fig. 5: Input-Output waveforms of proposed 5T latch design

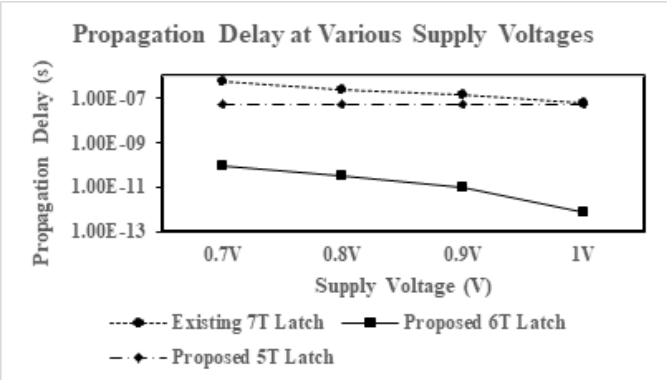
The architectural configuration and schematic illustration of the proposed 6T latch are illustrated in Figure 4(a) and Figure 4(b), respectively. The input-output waveforms of the proposed 5T latch, are depicted in Figure 5 above. The data is faithfully captured by the proposed latch.

Relative Performance Evaluation

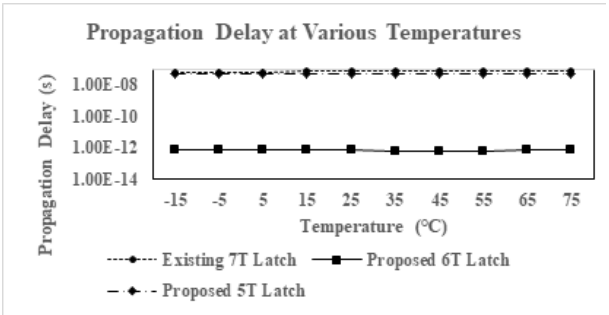
Each of the proposed design is evaluated for performance based on various parameters in the following section. For comparison, the existing 7T latch is simulated in the same environment as the proposed designs. All simulations are performed at 45nm technology on Cadence Virtuoso tool at room temperature. The voltage range for simulations is taken from 0.7 to 1V.

Propagation delay assessment

An analysis was done between the transmission delay of the existing 7T latch and the proposed 6T and 5T latch designs with diverse power supplies. As displayed in Figure 6(a) and 6(b), the delay observed in the proposed 5T latch configuration is significantly less as compared to that of the former 7T latch, where both the mentioned latches offer propagation delay in terms of nanoseconds. The proposed 6T latch stands out for its exceptionally low propagation delay across a range of supply voltages, achieving delays in the picosecond range.



(a)



(b)

Fig. 6: Comparison of Propagation Delay at various (a) supply voltages (b) temperatures

Power-Delay-Product assessment

Power-Delay Product (PDP) is a key performance metric in VLSI circuit design to identify the trade-off between average power consumption and speed of the circuit. Reducing delay results in increased power consumption and vice versa, so this metric helps designers to make a trade-off between the two parameters of the design. Lower value of PDP indicates better power efficiency and fast speed of the circuit. The simulation results for the existing and proposed designs are summarized in graphs shown in Figure 7. The energy consumption for the existing 7T latch and the newly proposed 5T latch is of the order of fJ. However, the 6T latch design introduced in this study provides 10 fold reduction in PDP at lower voltages which is further improved to 100 folds at voltages near 1V.

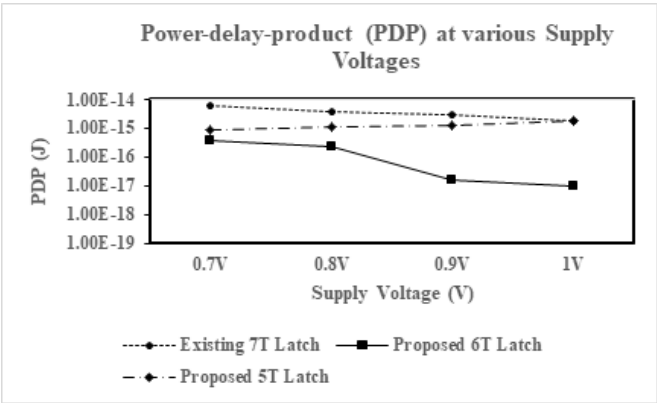


Fig. 7: Comparison of PDP at various supply voltages

Energy-Delay-Product assessment

Energy-Delay-Product (EDP) accounts for energy efficiency and speed in a quadratic manner, emphasizing low-power consumption and faster design. Unlike PDP which considers power and delay EDP prioritizes delay reduction more aggressively. Minimizing EDP in latches contributes to the overall efficiency and effectiveness of a complex digital system, ensuring optimal operation and performance across the entire system. An evaluation of EDP for the existing latch and the proposed latch designs has been conducted across different supply voltages with results shown in Figure 8. It is found that the EDP of the proposed 5T latch and 6T latch are notably lower when compared to that of existing 7T latch design, indicating improved energy efficiency. These results are graphically depicted in Figure 8, illustrating the substantial reductions in EDP achieved by the proposed latch designs.

Both novel designs of D latch offer significantly improved PDP and EDP against existing 7T latch design due to their reduced transistor count which lowers the parasitic capacitance providing better switching and

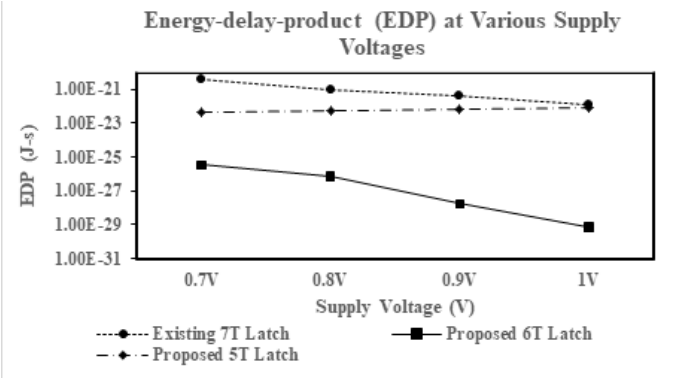
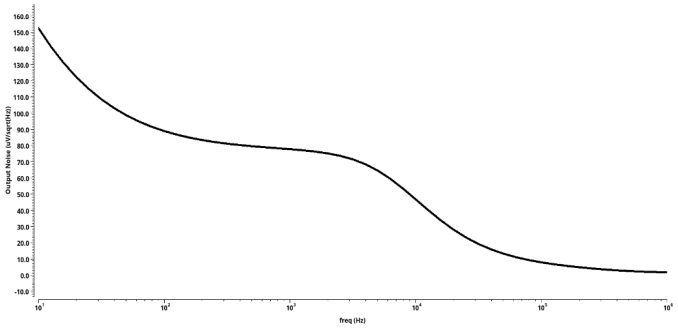


Fig. 8: Comparison of EDP at various supply voltages

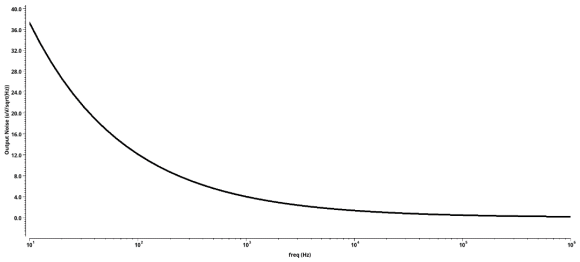
lower power dissipation. The use of transmission gate προωιδεσ βalanced pull-up and pull-down networks with CMOS inverter to ensure robustness of the signal. Also, this structure offers efficient charge transfer because transmission gate has high driving capability with minimum voltage degradation. Proposed 5T latch design is based on pass transistor logic which further reduced the transistor count for even higher energy-efficieny.

Output noise assessment

Minimizing output noise levels is essential for ensuring the robust and reliable operation of latch for achieving optimal system performance and meeting optimal performance requirements. Output noise analysis for existing and proposed latches is carried out for a frequency range of 10 Hz to 1 MHz. The simulation results are shown in Figure 9(a), 9(b) and 9(c) respectively for the existing and proposed designs. It is observed that the proposed 6T latch exhibits an output noise level as



(a)



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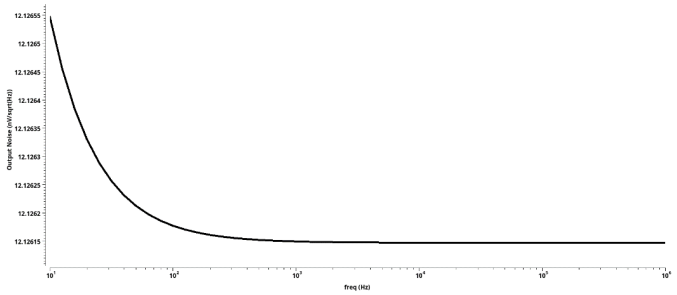


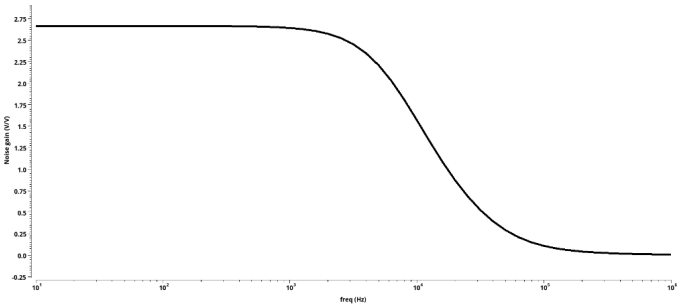
(c)

Fig. 9: Output Noise Analysis of (a) existing 7T latch (b) proposed 6T latch (c) proposed 5T latch

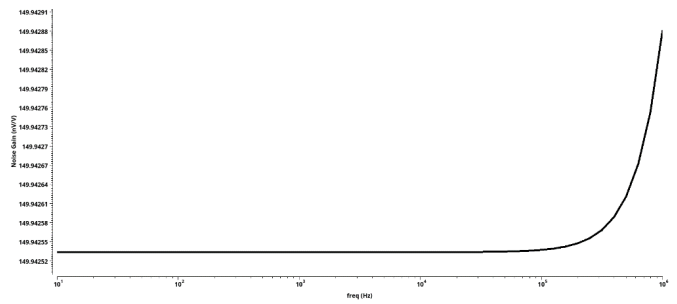
low as 152.458 nv/√Hz, while the 5T latch demonstrates a slightly higher output noise level of the order of 12 nV/√Hz at an operating frequency of 1MHz. The proposed designs improved the noise performance as compared to 1.7001 μV/√Hz offered by the existing 7T latch design.

Noise gain assessment

Noise gain is a vital parameter for analyzing the stability and robustness of sequential circuits by assessing the amplification or attenuation of noise signals within the circuit. High noise gain indicates high susceptibility of the design to unwanted disturbing signals, which reduces the ability of the latch to sustain stable and correct signal levels. Interpreting and reducing the noise gain to minimum is necessary to ensure the reliability and robustness of the D latch, particularly in high-speed applications where noise can effectively impact overall



(a)



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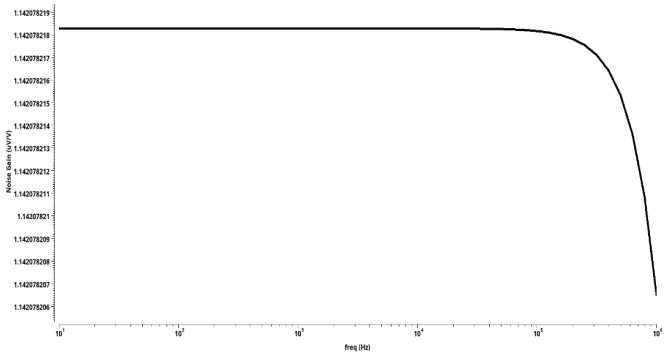


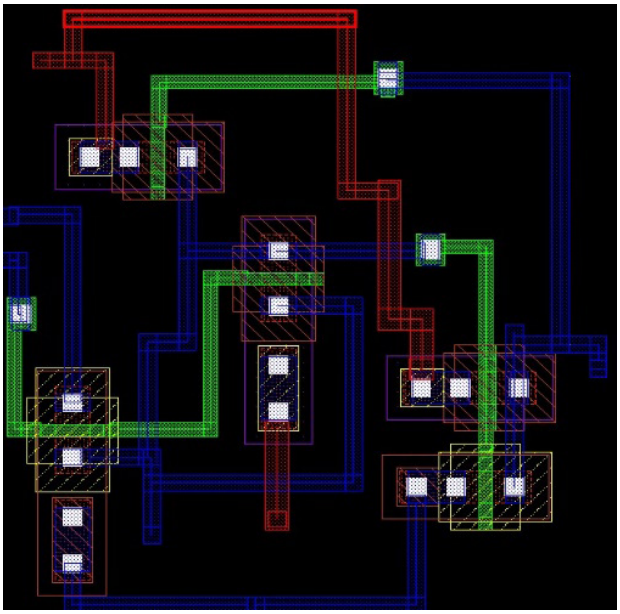
(c)

Fig. 10: Noise gain for (a) existing 7T latch (b) proposed 6T latch (c) proposed 5T latch

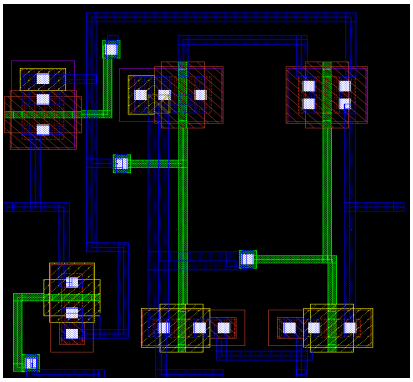
circuit's performance. All designs under consideration are analyzed for their noise gain and the results are presented in Figure 10. The existing 7T latch exhibit high noise gain of 2.65, which is greatly reduced for the proposed 6T and 5T designs. However, the gain increases at higher frequencies for 6T design. The reasons for this change in gain is left as an exercise for next stage of work. Thus, small noise gain ensure reliability and noise handling capabilities of the proposed design.

Area assessment

Another important improvement offered by the proposed design is in terms of reduced area. The layout of both the proposed latch designs is shown in Figure 11(a) and Figure 11(b) respectively which occupies an area of 4.7183 μm^2 for 5T latch design and 5.6024 μm^2 for 6T latch design. The area is lower than the existing couterparts as the number of transistors is reduced.



(a)



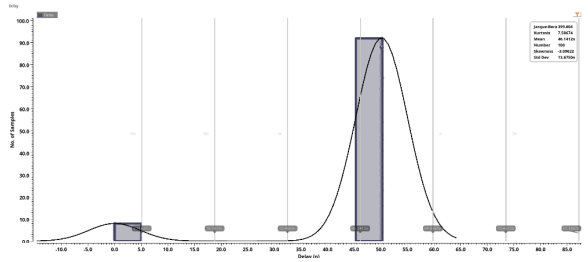
(b)

Fig. 11: Layout of proposed (a) 5T latch (b) 6T latch

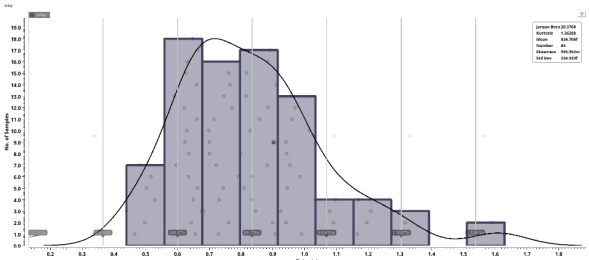
Robustness Analysis of Proposed Latch Configurations

Monte Carlo analysis

Monte Carlo analysis[13-15] accounts for parameter variations by simulating numerous random process variations, which allows to assess the impact of process variability on different essential parameters like propagation delay. Monte Carlo analysis also helps in evaluating the robustness of the proposed latch designs against process variations. This analysis provides statistical insights into the distribution of propagation delay values due to process variations. Monte Carlo analysis of proposed 5T and 6T latch designs is conducted for 100 samples and yields zero failures, it signifies robustness and reliability in the context of propagation delay. Monte Carlo analysis of proposed 5T and 6T latch configurations are shown in Figure 12(a) and Figure 12(b) respectively.



(a)



(b)

Fig. 12: Monte Carlo analysis of (a) proposed 5T latch (b) proposed 6T latch

Corner analysis

Corner analysis is used to study the performance of a circuit across various process parameters known as process corners, such as voltage, temperature, and manufacturing variations. This process variation study is performed to identify and quantify how manufacturing variations during the chip fabrication process can impact the performance and functionality of the circuit, its power consumption, propagation delay, and reliability by deviating transistor characteristics. The study involves different combinations of slow and fast PMOS and NMOS transistors.[16-17] These corners are typically categorized as Slow-Fast (SF), Slow-Slow (SS), Fast-Slow (FS) and Fast-Fast (FF). The aim of this analysis is to find how these variations affect circuit performance under worst-case conditions and ensure that the design operates effectively across the entire range of process variations. By corner analysis of proposed latch designs, their behaviour at extreme process corners, robustness, reliability, and manufacturability of the latch designs are ensured while optimizing performance and yield for practical implementation. Simulation outcomes for propagation delay obtained by corner analysis performed on the proposed novel 5T and 6T latches across various supply voltages are displayed in Table 1 and Table 2. Table 3 and Table 4 present the simulation results of corner analysis for propagation delay conducted on proposed 5T and 6T latches respectively under different temperature variations. All the values of propagation delay in Table 1 are recorded in ns while those in Table 2 are measured in ps.

Table 1: Corner analysis of proposed 5T latch with voltage variations

Voltage (V)	Process				
	FF	FS	SF	SS	TT
0.6	20.01	20.49	20.02	20.07	20.02
0.8	50.07	50.1	50.28	50.46	50.16
1	50.06	50.09	50.24	50.41	50.14
1.2	50.05	50.08	50.24	50.41	50.13
1.4	50.05	50.08	50.23	50.41	50.13

Table 2: Corner analysis of proposed 6T latch with voltage variations

Voltage (V)	Process				
	FF	FS	SF	SS	TT
0.6	2.151	5.164	4.244	2.77	4.566
0.8	6.236	9.348	5.727	1.771	6.811
1	13.37	1.309	2.828	0.7087	0.7897
1.2	18.64	0.7473	1.481	0.698	5.771
1.4	21.55	0.6269	1.154	1.583	1.754

Table 3. Corner analysis of proposed 5T latch with temperature variations

Temperature (°C)	Process				
	FF	FS	SF	SS	TT
-15	50.07	50.12	50.3	50.54	50.17
-5	50.06	50.11	50.28	50.54	50.16
5	50.06	50.1	50.26	50.46	50.15
15	50.06	50.1	50.25	50.43	50.15
25	50.06	50.09	50.24	50.41	50.14
35	50.06	50.09	50.23	50.39	50.13
45	50.06	50.09	50.22	50.37	50.13
55	50.06	50.08	50.21	50.36	50.13
65	50.06	50.08	50.21	50.35	50.12
75	50.06	50.08	50.2	50.34	50.12

As evidenced by the data obtained by corner analysis, it is clear that under a 1V power supply, the fast-fast (FF) process yields the optimal result in terms of propagation delay for the proposed 5T latch. Conversely, most favourable results in terms of propagation delay are demonstrated by the slow-slow (SS) process for the 6T latch design. . Table 1 and table 3 show that the values of propagation delay remain nearly same under voltage and temperature variations in the corner analysis. This infers that proposed 5T latch configuration indicates stability of propagation delay at different supply voltages and wide temperature range which suggests that the proposed 5T latch design is robust and indicates minimum susceptibility to environmental fluctuations. The proposed 5T latch-based shift register demonstrates significant efficiency in terms of transistor count and performance, making it a highly suitable choice for low-power and compact applications, while effectively supporting Serial-in parallel-out and serial-in serial-out operations with minimal hardware complexity.

Table 4: Corner analysis of proposed 6T latch with temperature variations

Temperature (°C)	Process				
	FF	FS	SF	SS	TT
-15	13.04	1.213	1.9935	16.04	0.769
-5	13.05	1.194	1.9939	16.05	0.7732
5	13.09	1.213	1.9966	16.1	0.778
15	13.16	1.232	1.9976	0.7171	0.7826
25	13.34	1.252	1.9979	0.7101	0.787
35	0.7652	1.327	2.0941	0.7018	0.6711
45	0.7729	1.226	2.1596	0.6207	0.6771
55	0.7802	1.251	2.1608	0.6162	0.6826
65	0.7878	1.275	2.2472	17.03	0.6875
75	0.797	1.299	2.3221	17.24	0.6917

The results obtained by performing corner analysis assures that both the proposed designs of D latch maintain optimal performance at manufacturing variations, validating robust operation with least impact on power consumption and operating speed of the circuits.

Application of Latch: Shift Register

Proposed CMOS latches can be used for making various digital circuit applications. This section of the paper presents a 3-bit shift register that uses the proposed 5T design. A shift register [18-20] leverages a cascade arrangement of D latches which stores and shifts data sequentially, bit by bit at each clock cycle. This is utilized in efficient serial-to-parallel data conversion, delay line operations, and for storing data temporarily in digital systems. Given that the proposed 5T latch deploys the least number of transistors for implementation of latch, it works as an optimal basic unit for designing a shift register. As a result, a 3-bit shift register is designed utilizing three similar proposed 5T latches which leads to utilization of a total of 15 transistors. The shift register functions efficiently and the circuit can be extended to n-bit shift register as well by utilizing n number of such latches. The corresponding schematic of proposed shift register circuit and its relevant simulation output waveforms are illustrated in Figure 13 and Figure 14, respectively.

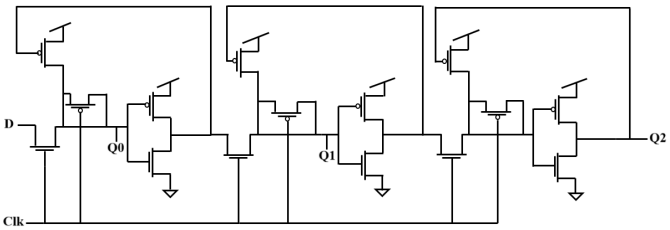


Fig. 13: Circuit diagram of shift register using proposed 5T latch

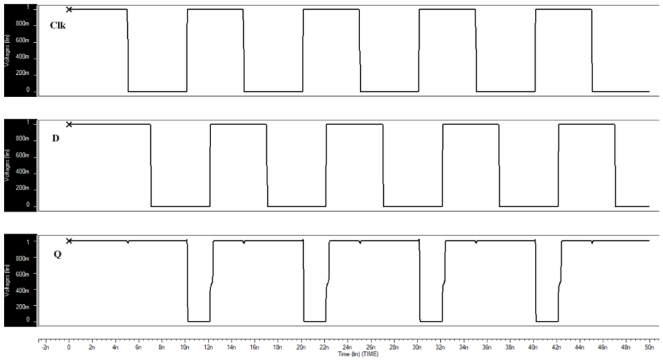


Fig. 14: Simulation waveforms of shift register using proposed 5T latch

Conclusion

The research findings after simulating the existing and both the proposed circuits of latch utilising Cadence

Virtuoso tool in 45nm technology at room temperature and supply voltage as 1V, demonstrate that the proposed latch configurations exhibit superior performance characteristics as compared to the existing 7T latch design. Two D latches have been designed using 5 and 6 transistors, individually, showcasing a reduction in transistor count compared to the existing design, which utilizes 7 transistors. As proposed 5T latch utilises minimum number of transistors, it implies that it would require least area on chip which is found out to be 4.7183 μm^2 obtained by designing layout of the mentioned configuration of latch. Additionally, proposed 6T latch would require 5.6024 μm^2 silicon area on chip which is obtained by evaluation conducted on designed layout of 6T latch configuration. The proposed latch designs show superior speed performance when compared to the existing design of latch, as evidenced by significantly lower propagation delays. Specifically, the proposed 6T latch configuration stands out with propagation delays measured in picoseconds range, a remarkable improvement from the nanoseconds range of propagation delay observed in the existing 7T latch design. Similarly, the outcomes of energy consumed (PDP) and energy efficiency (EDP) of both the proposed 5T and 6T latch designs exhibit significant improvements when contrasted with those of existing latch configuration. In this regard also, the proposed 6T latch stands out, demonstrating highly superiority as compared to the existing design. The output noise metrics for the existing latch design, along with both the proposed designs of latch. The analysis show that both the proposed latches offer a substantially lower output noise as compared to that offered by the existing design of latch. Additionally, the noise gain of the existing latch design and both proposed latch designs were also assessed, and on comparison, it is revealed that the noise gain of both the proposed latches is significantly lower than that exhibited by the existing latch design. For testing the reliability of proposed 5T and 6T latch designs, Monte Carlo analysis of these latches for 100 samples is conducted which yielded zero failures for both the latch designs, it provides strong evidence of robustness, reliability, and suitability of both the proposed configurations of D latch for use in practical applications. Additionally, by comprehensively evaluating behaviour of both the proposed latch designs across process corners and at different supply voltage values and temperature range, it is ensured that both the proposed configurations of D latch are robust and reliable designs that meet performance specifications under varying manufacturing conditions. An application of the proposed 5T latch, i.e., a 3-bit shift register has also been designed and simulated. Results demonstrate efficient operation of the designed circuit, and the design is scalable to an n-bit shift register by making use of n such latches which validates the practicality of the proposed 5T latch in advanced applications. Their compact transistor level designs aids in achieving high-density placement, minimizing area, power, energy and interconnect delay for Application Specific Integrated Circuit (ASIC) designs, especially for microprocessors, digital signal processors and IoT applications.

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