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A 3.7-4.8GHz Programmable Integer-N PLL With Multi-Modulus Divider and Tunable VCO in Standard 45nm CMOS Technology

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Abstract

This paper presents a comprehensive study of each phase-locked loop (PLL) component to enhance its flexibility for various applications. First, a differential voltage-controlled oscillator (VCO) is designed with programmability enabled through a capacitor bank controlled by a 4-bit word, allowing it to cover a wide frequency range. Second, an integer-type frequency divider is implemented using a multi-modulus technique, introducing programmability to the divider. The multi-modulus divider consists of seven divider stages, where each stage can divide the input frequency by a factor of two or three, controlled by a seven-bit control word, enabling a wide range of division values. Since the frequency decreases after each stage, each divider stage is optimized for power efficiency. Third, a phase-frequency detector is designed with an extended phase detection range from -2π to +2π. Additionally, a charge pump and loop filter are designed to provide a stable control voltage, ensuring the VCO operates at the desired frequency. The PLL is designed using the Cadence Virtuoso Analog Design Environment with 45nm CMOS technology and simulated using the Spectre simulator. Operating at a 1.1V supply, the PLL achieves a lock state in 14μs while consuming 27.4mW of power. The designed PLL delivers stable output frequencies in the range of 3.7–4.8GHz. The PLL shows PSRR of about 8dB when a small AC noise source (V_n=1mV) applied on the power supply.

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Introduction

The advances in wireless technology have made the transfer or sharing of information simple and efficient thereby maximizing its impact to society around the globe. Due to these advances more memory space is required to store such a large transfer of information. This can only be done by reducing the device size which means scaling of MOS transistor to deep submicron levels. The most important part of wireless technology is the wireless trans-receiver. Its role is to transmit or receive the information to (or from) the wireless device. In the wireless trans-receiver, the frequency synthesizer is responsible for generating a stable output frequency which is used further to mix the received signal down to lower frequencies and vice-versa. This stable output frequency is generated by using Phase Locked Loop (PLL). PLL design consists of five components namely, Phase Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage Controlled Oscillator (VCO) and Frequency Divider. The PLL is designed for Bluetooth application. However, with tuning ability of our proposed VCO and programmability in frequency divider, the proposed frequency synthesizer design can be utilized for several other wireless applications also.[1-4] From two decades several designs have been published of low power charge pump, accurate loop filters, tunable VCOs and frequency dividers.[5-12] Before actual transistor level closed loop simulation of PLL, the mathematical modeling of PLL is to done using MATLAB Simulink. This is done in order to save time and to get an idea that whether the loop is going to lock or not. Also, the model of PLL at Simulink can also be imported with Verilog code of different components of PLL and thus can be tested using FPGA. Hence the paper first illustrates the design of various PLL components with their basic circuits. Then, later in the paper, PLL simulation results are presented. Furthermore, using system generator Verilog implementation of PLL can be imported to

Simulink and the designs can be tested using any FPGA board. The proposed design can also be fabricated using CMOS process, but integrating several components will be challenging.

Three-State phase Frequency Detector

The schematic of designed PFD is shown in Figure 1. The Reference signal (f_{ref}) and the divided output signal (fvco/N) acts as input clock signals to both of the D flip-flops. The inputs of D flip-flops are always remained connected to logic high which in this case is power supply voltage Vdd. The Phase Frequency Detector outputs are named UP and DN which are also connected to the input terminals of AND gate whose output is connected reset (rst) terminals of both the flip-flops.

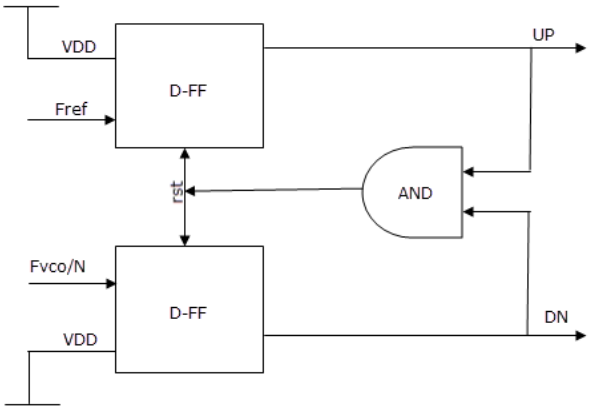

Fig.1: Schematic of PFD

A. Characteristics of designed PFD

(i) Both phase as well as frequency difference between the two input signals can be detected.

(ii) It has highest linear phase detection range of thereby increasing Lock-in range of PLL.

(iii) Edge-triggered implementation makes output of this PFD independent from duty cycle of the input signals.

(iv) This circuit will change the state only at the rising edges of the inputs as the D inputs are always connected to logic '1'.

Charge Pump and Loop Filter

The MOS switches (UP and DN) are connected to the source terminals of their respective current mirrors as shown in Figure 2 thus, configuration is known as source-switched charge pump. Also the signal at 'UP' is passed through a NOT gate before entering the Charge Pump. This is because, the MOS switch for 'UP' signal is made using PMOS. Whereas, for 'DN' signal, NMOS is used as a switch.

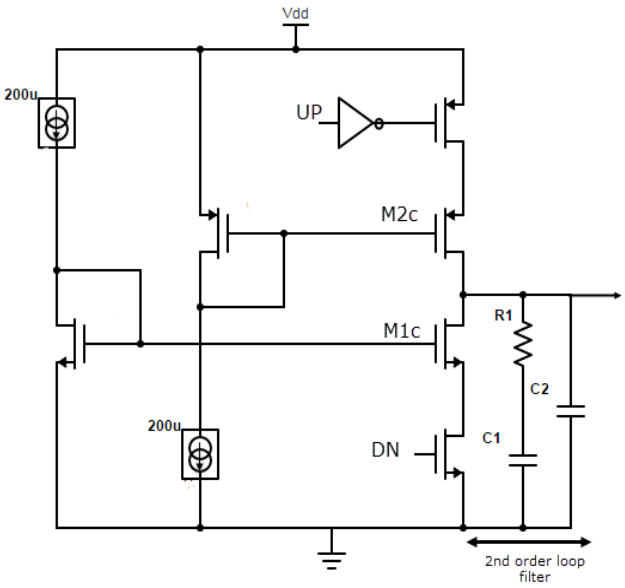

Fig. 2: Schematic of source switched charge pump.

A. Characteristics of designed Charge Pump

(i) In this topology, charge pump current (Icp) at the output is independent of the switching time because the bias transistors M2c and M1c (shown in Figure 2) are not connected to switches. This was not the case with gate-switch topology where, reduction in Icp leads to low switching time.

(ii) Higher switching speed is attained since, the switch is connected to a single transistor with lower parasitic capacitance.

(iii) In OFF state DN switch gets connected to virtual ground thereby, giving higher output impedance which results from series connection of two transistors in OFF state. Due to this, leakage current is also gets reduced.

(iv) Transistors M1c and M2c will always remain in saturation due to which no current spikes exists in this topology.

(v) This topology can handle higher frequencies.

Voltage Controlled Oscillator

The programmable differential VCO in this PLL synthesizer is designed using complimentary CMOS topology. The VCO is made programmable using capacitor bank which is used for discrete frequency tuning. The combined schematic diagram is shown in Figure 3.

The proposed VCO generates oscillations at all possible 16 input control words. Therefore, it can be concluded that the VCO is programmable. The proposed VCO generates frequencies between 3.7-4.8GHz having phase

noise between -94 to -100.21dBc/Hz @ 1MHz frequency offset. and tuning linearity is 200MHz/V. The proposed VCO consumes 12 mW power. All the simulated results are summarized in table 1.

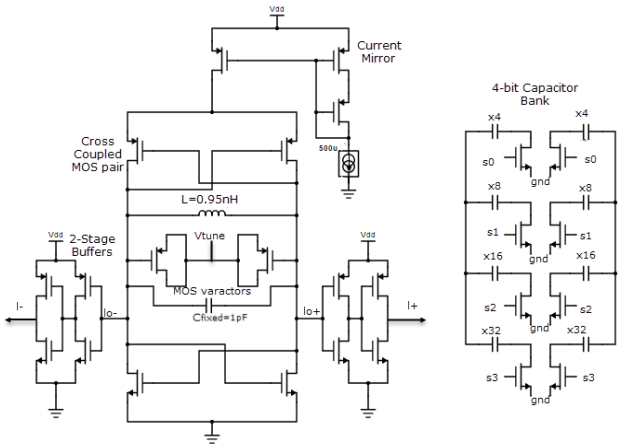

Fig. 3: Schematic of proposed programmable VCO.

Frequency Divider

Our proposed PLL synthesizer uses truly modular fully programmable divider architecture[7] as it has high reusability, simple layout, easy optimization, high flexibility, and low power consumption.

A. Circuit design of D Latch

The D latch is designed using Current-mode Logic (CML) topology. In this topology, instead of having seven blocks in total (four D latches and three AND gate) used in conventional topology, only four blocks exist in the designed combined AND_D Latch schematic is shown in Figure 4.

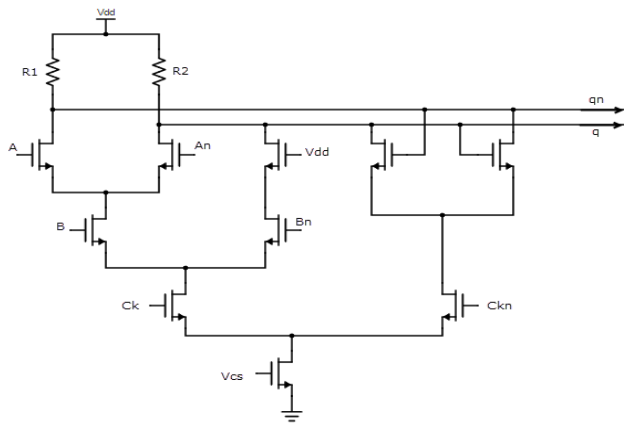

Fig. 4: Schematic of AND_D latch.

B. 2/3 DIVIDER cell

A single 2/3 cell [8] is designed using four D Latches. The resulting circuit now behaves as 2/3 divider which can divide input frequency by a factor of 2 or 3 depending on control pin (p). Means, if p=0 then the cell divides by 2 and if p=1 the cell will divide by3. The designed 2/3 cell schematic is shown in Figure 5.

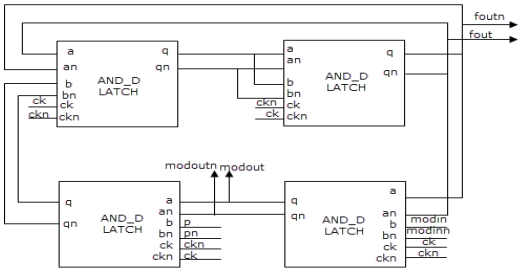

Fig. 5: 2/3 Divider cell schematic.

In this PLL, we are using reference frequency of 20 MHz and VCO frequency of 4.8 GHz. Therefore to scale down the frequency of 4.8 GHz to 20 MHz, the division ratio needed can be calculated as follows,

$$Fvco = M \cdot Fref$$
$$\Rightarrow M = Fvco/Fref$$
$$M = 240$$

Since the VCO is tunable, therefore the minimum frequency given by it is 3.7 GHz for this frequency the ratio of M =185. Therefore, the division ratio range need is from 240 to 185.

Thus, taking n=7 such that the division ratio ranges from 2^7(=128) to $2^{7+1}-1$ (= 255). The actual divider circuit top level architecture is shown in figure 6.

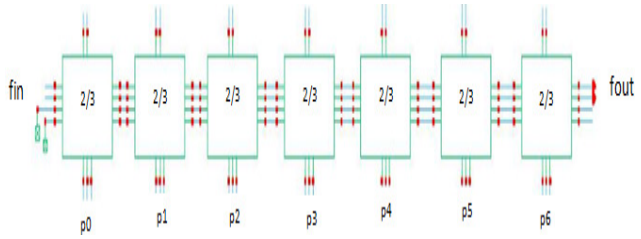

Fig. 6: Designed 7-bit differential multi-modulus divider.

Thus, we conclude that when n = 7, the desired divide ratio(185 to 240) lies in case when 7 stages are used which provides divide ratios between(128 to 255). These divide ratios are obtained using control pins p0,p1,p2,p3…..p6 which decides whether to divide by 2 or 3 with the help of seven-bit control word.

Proposed PLL Simulation in Simulink

In order to save time and to get an approximate idea of closed loop behavior of PLL, each component of PLL is converted into mathematical model from transistor level. This is done by using MATLAB Simulink. The properties

of each mathematical block are their respective values which are extracted from transistor level simulation. With this, all the components are combined and simulated together to obtain quick and accurate results of various loop analysis such as Loop dynamic behavior, stability, and output performance.

A. PFD design in Simulink.

The Simulink model of tri-state phase frequency detector (PFD) is made using different components like, AND gate, D flip-flop from their respective libraries. The resulting circuit in Simulink is shown in Figure 7.

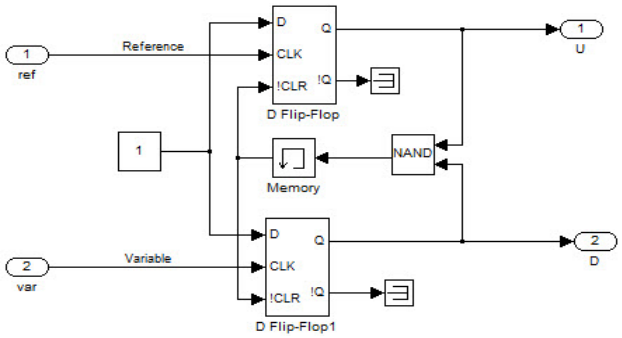

Fig. 7: PFD schematic.

B. Charge pump and loop filter in Simulink

The combined circuit of CP-LF in Simulink is shown in figure 8. The circuit in this figure is designed similar to the circuit of figure 2.

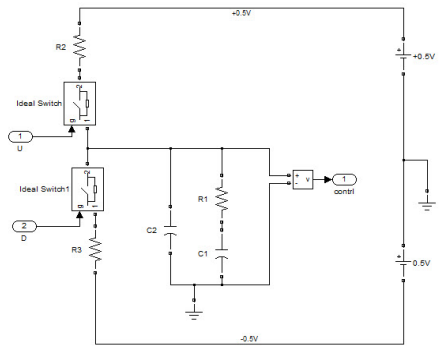

Fig. 8: Charge pump loop filter schematic in simulink

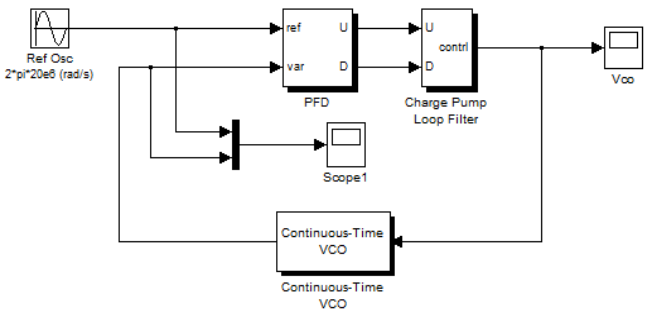

Fig. 9: Charge pump PLL in Simulink

C. Simulation results of PLL in Simulink

Transient simulation is done for the case when divide ratio is 240 (ratio to divide 4.8GHz frequency to 20MHz reference frequency) and gain of VCO is 200MHz/V. The resulting waveform is shown in figure 10. From figure 7.7 it can be concluded that the loop gets locked successfully after 5us.

Simulation Results of Proposed PLL in Cadence Virtuoso.

The PLL circuit is realized by connecting all the designed blocks namely, Phase Frequency Detector (PFD)(Section II), Charge Pump (CP)(Section III), Loop Filter (LF), Voltage Controlled Oscillator (VCO)(section IV) and Frequency Divider (FD)(section V) in a closed loop. The resulting circuit is shown in Figure 11. The proposed PLL is simulated using “Cadence Virtuoso Analog Design Environment” and using 45nm technology file. The circuit is simulated using “Spectre” simulator. The voltage supply used is 1.1V. The input frequency is 20MHz.

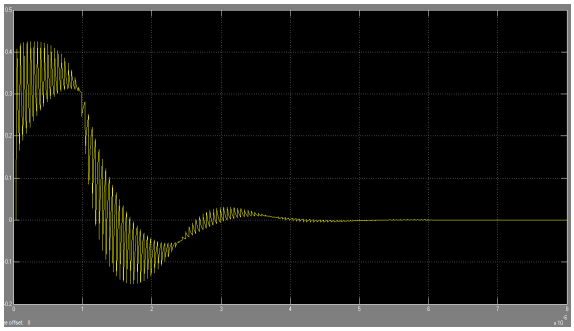

Fig. 10: Transient simulation of PLL.

The transient simulation of PLL is done for the case when output frequency of VCO is 4.8GHz. This is done by setting its switches as s0=s1=s2=s3=0 to get 4.8GHz as its output frequency (table 5.1).

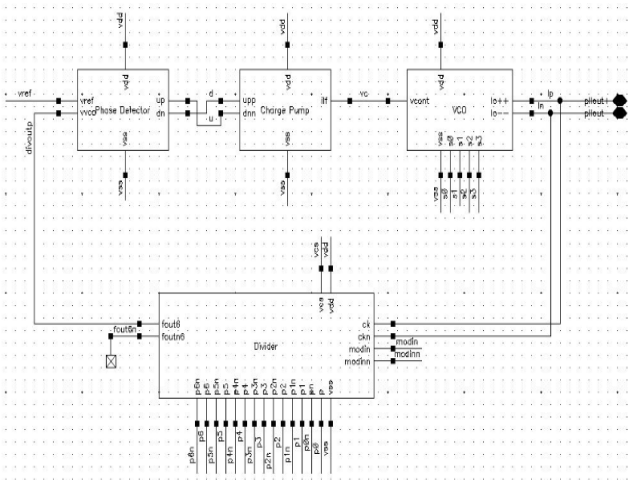

Fig. 11: Schematic of proposed PLL

To get the exact frequency, the constant tuning voltage of 680mV is required from charge pump. Now this frequency is to be scaled down to 20MHz, so division ratio is calculated as follows

$$Fvco = M \cdot Fref$$
$$M = 4.8GHz/20MHz$$
$$M = 240$$

Thus, the 7-bit control word for the frequency divider would be "1110000" where, P0=P1=P2=P3=0 and P4=P5=P6=1. Thus, the transient simulation results of PLL for this case are shown in figure 12 to 16. Figure 12 display transient simulation output of charge pump in closed loop and 13 represents VCO waveform. Figure 14 displays phase frequency detector transient response of reference frequency and VCO frequency and figure 15 shows PLL in Locked State. The proposed PLL can also be fabricated 45nm CMOS process keeping following challenges; frequency divider, phase-frequency detector switches at high frequency which can introduce substrate noise, PLL require stable clock routing which are free from jitters and skews, parasitic capacitances of VCO can vary tuning range and frequency, charge pump is sensitive to leakage currents, and most importantly charge pump mismatch dur to process variations is very critical. Post layout simulation using extracted file, Corner / Monte Carlo simulations, jitter and phase noise analysis will definitely improve the design credentials. During fabrication some improvised solutions like guard rings, isolation, routing strategies can be used to minimize noise and jitter reduction. Furthermore, to test proposed design of PLL, all its components phase detector, charge pump, VCO and frequency divider can be designed and simulated using Verilog and also synthesized and tested using any FPGA board, the code can be imported through system generator to the Simulink and tested again keeping same frequency range.

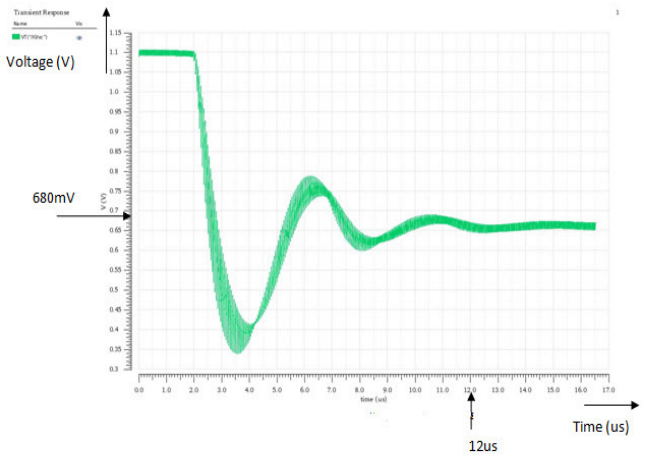

Fig. 12: Transient simulation output of charge pump in closed loop

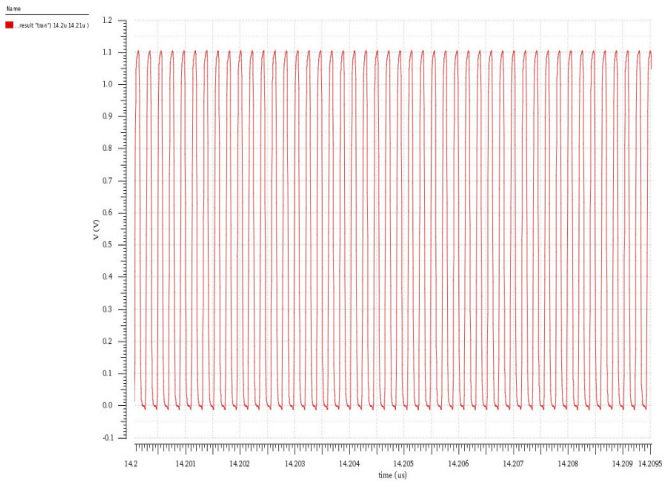

Fig. 13: The output frequency VCO

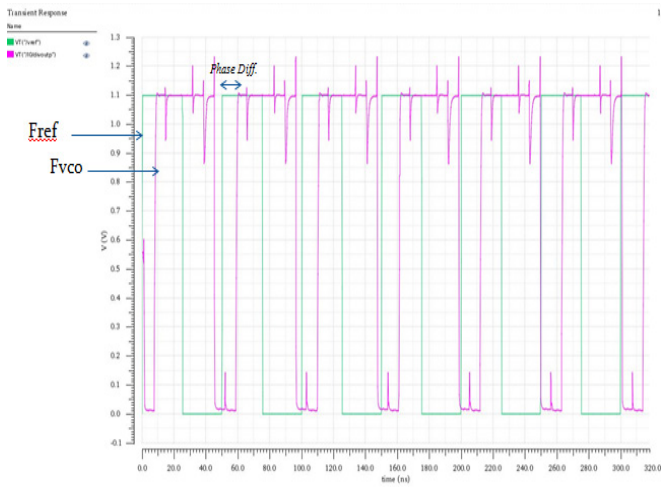

Fig. 14: Transient waveform at PFD inputs

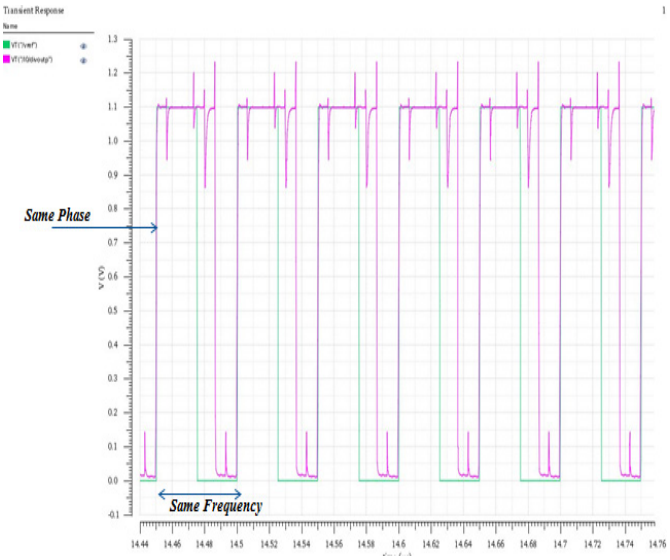

Fig. 15: PLL in Locked State

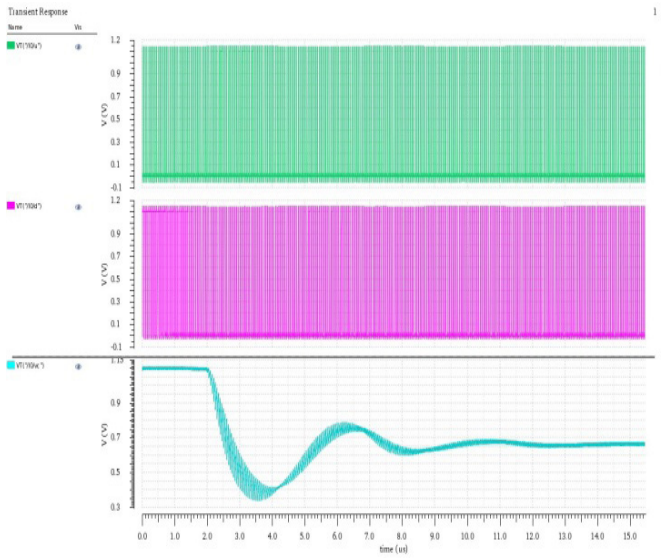

Fig. 16: PFD-CP-LF transient responses

Conclusion

All the simulations of proposed PLL is done using "Cadence Virtuoso Analog Design Environment" using 45nm technology file. The PLL circuit is simulated using "Spectre" simulator. The voltage supply used is 1.1V. The simulation is done for 20us and the input frequency is 20MHz. The proposed PLL successfully locks frequencies within 3.7-4.8GHz frequency range and consumes 27.4mW of power. The setting time of PLL is 12us. The PLL shows PSRR of about 8dB when a small AC noise source (V_n=1mV) applied on the power supply. Tuning range and phase noise analysis of VCO is illustrated in Table 1. Phase noise of VCO is directly related to jitter. The characteristics of PLL are summarized in Table 2. Improving power supply isolation, optimizing the VCO, and reducing charge pump mismatch can reduce the phase noise and thus jitter. Comparative Analysis with state of the art have been tabulated in Table 3. Studying state of the art PLL literature, our proposed design is

Table 1: Tuning Range and Phase Noise of Proposed VCO

S3S2S1 S0	0.5V to1.1V (GHz)	Kvco (MHz/V)	Phase Noise @ 1MHz
0 0 0 0	4.83 – 4.71	200	- 94.00 dBc/Hz
0 0 0 1	4.72 – 4.61	183.3	- 94.80 dBc/Hz
0 0 1 0	4.62 – 4.51	183.3	- 95.65 dBc/Hz
0 0 1 1	4.53 – 4.42	183.3	- 96.10 dBc/Hz
0 1 0 0	4.43 – 4.33	166.6	- 96.53 dBc/Hz
0 1 0 1	4.35 – 4.26	150	- 96.99 dBc/Hz
0 1 1 0	4.27 – 4.19	133.3	- 97.42 dBc/Hz
0 1 1 1	4.20 – 4.12	133.3	- 97.52 dBc/Hz
1 0 0 0	4.12 – 4.04	133.3	- 97.93 dBc/Hz
1 0 0 1	4.06 – 3.99	116.6	- 98.12 dBc/Hz
1 0 1 0	4.00 – 3.93	116.6	- 98.48 dBc/Hz
1 0 1 1	3.94 – 3.88	100	- 98.74 dBc/Hz
1 1 0 0	3.88 – 3.82	100	- 99.10 dBc/Hz
1 1 0 1	3.83 – 3.77	100	- 99.36 dBc/Hz
1 1 1 0	3.78 – 3.72	100	- 99.69 dBc/Hz
1 1 1 1	3.73 – 3.67	100	- 100.21 dBc/Hz

Table 2: PLL Synthesizer Performance

Synthesizer Configuration	Multi-Modulus
Input Reference Frequency	20MHz
Division ratio	185-240
Power Consumption (Programmable Divider)	13.92mW
Power Consumption (VCO)	12mW
Tuning Range	3.7 – 4.8 GHz
Power Consumption (PLL)	27.4mW
Supply Voltage	1.1V
CMOS Technology	45nm
Charge pump bias current	200uA
PLL settling time	**12us**

Table 3: Comparative Analysis of state of the art PLLs

PLL Name	VCO Frequency	Size	Phase Noise	Supply voltage	CMOS Technology	Power Consumption	Application
Ting Wu1, Pavan Kumar Hanumolu, Kartikeya Mayaram, and Un-Ku Moon 2007 [13]	4.096GHz and 4.208GHz	1.5 mm^2 1.3x1.15	-110 dBc/Hz (1 MHz)	-	0.13 µm	48mW	All basic Clocking applications.
P. K. Rout, B. P. Panda, D. P. Acharya and G. Panda Jan 2014 [14]	1 GHz	-	-54.12dBc/Hz	1.8V.	90nm	11.9 mW	Clocking Application For Low Voltage, Fast Phase and Frequency Acquisition.

PLL Name	VCO Frequency	Size	Phase Noise	Supply voltage	CMOS Technology	Power Consumption	Application
Ramanjaneyulu Ningampalli, Satyanarayana Donti and Satya Prasad Kodati 2018[15]	1.5 GHz and 3.28 GHz	-	-116 dBc/Hz	1.8V	0.18 µm	18.4 mW	All basic Clocking applications. HDMI applications.
Jian Chen 1, Wei Zhang, Qingqing Sun 1 and Lizheng Liu 2021 [16]	12.72 GHz	0.25mm²	−108.1dBc/Hz (1MHz)	1.8V	UMC 28-nm 1P10M	16.5mW	Communication and system clock generation.
Xiaokang Niu, Xu Wu , Lianming Li, Long He , Depeng Cheng and Dongming Wang 2022 [17]	45.2 GHz and 52.6 GHz	800 µm × 950 µm.	- 99 dBc/Hz	-	65nm	80mW	Communication System, Satellite Communication systems.
Proposed Design	3.7 – 4.8 GHz	0.042 mm² (probable)	- 94.00 dBc/Hz	1.1V	45nm	27.4mW	wireless communication, radar, satellite, and high-speed networking applications

designed at 45nm technology, low supply voltage (1.1V), comparable phase noise (jitter) and power consumption. The proposed PLL shows low settling time of about 12µs and chip area of about 0.042 mm² probably. Furthermore, to test proposed design of PLL, all its components phase detector, charge pump, VCO and frequency divider can be designed and simulated using Verilog and also synthesized and tested using any FPGA board, the code can be imported through system generator to the Simulink and tested again keeping same frequency range. The proposed PLL can be used in wireless communication, radar, satellite, and high-speed networking applications. PLLs in 3.7GHz to 4.8GHz frequency range function as local oscillators (LOs), frequency synthesizers, and clock generators, ensuring precise frequency control and synchronization.

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