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Energy Efficient GNRFET Based Ternary Full Adder for Next Generation Integrated Circuits

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Abstract

Ternary logic is an appealing alternative to binary logic, because it reduces circuit complexity, implementation area, and power consumption. This paper covers Graphene Nanoribbon Field Effect Transistor (GNRFET) based Ternary Full Adder (TFA) used for Next Generation Integrated Circuits. Instead of utilizing two states, ternary logic uses three states to execute efficiently in computation and data processing. This significantly reduces the complexity of the arithmetic circuit, making it suitable for high-speed applications. New technology, based on GNRFET, proposed as possible successor to CMOS technology. Proposed TFA1 and TFA2 with 98 transistors and 68 transistors, simulated using the HSPICE Simulator with 32nm MOS-GNRFET Nano Hub Models. Simulated results reveal that the proposed TFA2 has reduced Power Delay Product (PDP) than the proposed TFA1 approach. The most essential parameter of digital circuit design used in Multi Valued Logic (MVL) is the threshold voltage of GNRFET, changed in ternary logic to reduce power consumption and delay. Low power consumption and fast processing of these circuits make it suitable for the next-generation integrated circuits.

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Introduction

The growing need for high-performance and energy-efficient devices creates major circuit design problems to satisfy the evolution of Internet of Things and Embedded devices utilizing binary logic needs additional circuits, which leads to adoption of ternary logic-based circuit design. Complementary Metal Oxide Semiconductor (CMOS) transistors fail to meet efficient demands, making them less suitable for advanced applications beyond 32nm regime scaling because of the increased metal contact resistance, reduced reliability, and higher current leakage. Compared to traditional CMOS devices, GNRFETs planar structure reduces heat loss, and delay because of its low metal contact resistance. It has exceptional carrier mobility and thermal conductivity, which enhances circuit efficiency. Incorporating GNRFETs into ternary logic circuits, which utilize three distinct logic levels, enhances computational effectiveness.

GNRFETs demonstrate two key advantages for next-generation VLSI circuits through improved carrier mobility and decreased power requirements. The integration of GNRFETs into VLSI design processes faces three significant physical design challenges because of fabrication incompatibility and heat management requirements. GNRFET integration requires successful resolution of these issues to achieve their deployment in modern VLSI technologies.

Ternary operations consume much lesser power, fewer transitions and switching activities than the binary logic system.[1-5] Ternary logic uses three different logic levels to function. In ternary circuits, the ground GND level is low, while the supply voltage VDD is at a high level. Midway point voltage is at half the supply voltage VDD/2. This middle point is labeled as "0.5" to represent the middle value. This third voltage level, the middle point VDD/2, minimizes the number of gates which makes connections in the circuit less complicated.

The remaining section of this paper is stated as follows: section II illustrates the literature survey, section III highlights the GNRFET based Ternary Logic concepts,

section IV provides the detailed operation of proposed design of GNRFET based Ternary Full Adder, section V talks about results and discussions and section VI provides the conclusion.

Literature Survey

This section describes the literature review of ternary logic design methods such as binary logic gates, intermediate binary logic gates-based design, unary operators with Ternary Multiplexer (TMUX) based pass transistor logic, and unary operators with transmission gate based TMUX logic using Carbon Nano Tube Field Effect Transistors (CNTFET) and GNRFET transistors.

Pasupuleti Naga Sudhagar et al.[1] designed the GNRFET-based multiplier using the ternary logic, the author described the ternary logic using unary operators and tolerance variation of the implemented design has been analyzed with help of Monte Carlo Simulation.

Anuska Aggarwal et al.[2] described the ternary logic, dual value logic and multi valued logic circuits based on pass transistors, double pass transistors using CMOS and CNTFETs.

Erfan Abbasian et al.[3] implemented a ternary half adder utilizing the unary operators, multiplexers with pass transistor logic. The Sum circuit is generated utilizing unary operators combining with a 3:1 ternary multiplexer while the Carry circuit uses unary operators combined with pass transistor logic. Outputs from the unary operators fed as inputs to both the multiplexer and the pass transistor.

Mahdieh Nayeri et al.[4] proposed the arithmetic circuits by implementing with armchair graphene nano ribbon field effect transistor based on multi value logic design approach.

Erfan Abbasian et al.[5] implemented ternary half adder, by combining the unary operators with 3:1TMUXs. To obtain the Sum and Cout of Ternary Half Adder, Unary Operators output, given as input to the two 3:1 Ternary Multiplexer.

Ying-Yu Chen et al.[6] provided the basic SPICE compatible model used for analyzing the delay and power of GNRFET transistors.

Aloke Saha et al.[7] structured the CMOS ternary full adder and implemented using Single poly double metal 90nm CMOS process technology.

Mingyan Zhang et al.[8] introduced and presented a CMOS ternary full adder using Hybrid Pass transistor logic along with Static CMOS.

Sumeer Goel et al.[9] designed ternary full adder, using ternary inverters, ternary successor and predecessor circuits, along with unary operators like X0, X1, and X2. These unary operators produced through a ternary decoder.

Mariano Aguirre et al.[10] designed CMOS ternary full adder with 0.18 µm CMOS technology, using pass transistor logic to produce the Sum and Carry.

Parameshwara et al.[11] designed CMOS ternary full adder, using Transmission gate and Pass transistor logic to produce Sum and carry by using Cadence 90nm GPDK technology.

Sneh Lata Murotiya et al.[12] proposed a Ternary Full Adder by combining different ternary inverters. These inverters combined with pass transistor logic and a ternary buffer to obtain the desired functionality. Pass transistor usage reduces power consumption in the circuit.

Ramzi A. Jaber et al.[13] presented the ternary full adder with unary operators and two variations of TMUXs implemented with transmission gates. In the first method, the inputs to the unary operators connected through a 2:1 multiplexer-based transmission gate, and their output fed into a 3:1 multiplexer-based transmission gate in order to obtain the final TFA sum and carry. The unary operator outputs fed into a 3:1 ternary multiplexer-based transmission gate and the output from this multiplexer, fed to a 2:1 ternary multiplexer-based transmission gate to produce the sum and carry of the second TFA method.

Trapti Sharma et al.[14] proposed ternary arithmetic circuits implemented with ternary and binary logic gates that includes multiplexer, subtractor, half adder and full adder. TFA proposed in this design, implemented using unary operators and a multiplexer. Additionally, multiplexers and encoders applied in designing the ternary subtractor circuits.

Farzin Mahboob Sardroudi et al[15] structured the ternary full adder with Pass Transistor Logic using standard ternary buffers (STB). Ternary buffers outputs passed to pass transistors by dynamically, ternary buffers either precharge the output node for required output or discharge the output node.

Seyyed Ashkan Ebrahimi et al.[16] demonstrated a ternary full adder with ternary half adders. A and B presented to the first THA that produces the intermediate result H. This result, with the aid of A and B, presented to both the second ternary half adder and carry generator unit which produces the Sum and Carry of TFA.

Fereshteh Jafarzadehpour et al.[17] have designed a TFA comprises of two Ternary Half Adder Sum Generator circuits. These circuits employed in conjunction with the Carry Generation Unit to produce the TFA Sum and Carry. Results from the first Ternary Half Sum Generator, developed in the Sum Generator Unit passed to the Carry Unit to calculate the Carry Out value.

Jihab Mohamed Aljaam et al.[18] designed Half Adder and Multiplier based on ternary logic combination. These circuits realized using Unary Operators and Transmission Gates. Ternary Half Adder outputs obtained by using the outputs of the Unary Operators as inputs to the transmission gates. Ternary Multiplier also designed with the help of Unary Operators and Transmission Gates.

Zarin Tasnim Sandhie et al.[19] implemented logic gates and arithmetic circuits based on ternary logic. GNR-based ternary half adder circuit design implemented using positive, negative and standard ternary inverter, and multiplexer by altering the width and the dimer lines of the GNR.

Peiman Keshavarzian et al.[20] presented ternary full adder that operates with two independent Sum and Carry generators. Both the Sum and Carry generator circuits, uses CNTFETs with three distinct diameters and threshold voltages.

Sepehr Tabrizchi et al.[21] illustrated a TFA based on unary operators with standard ternary inverter, and two operators of unary functions. Unary Operators used along with the ternary multiplexer for obtaining sum output and the carry output.

Ramzi A. Jaber et al.[22] suggested the ternary half adder design through multiplexer and unary operators. Sum and carry derived from a series of ternary multiplexers implemented using the following unary operators: positive and negative ternary inverter, and decisive literal operators.

Narges Hajizadeh Bastani et al.[23] implemented a switching logic-based ternary full adder that depends on pass transistors and transmission gates for the sum and carry outputs. Switching logic improves circuit efficiency and performance. The sum circuit constructed from the unary operators, including positive and negative ternary inverter, its successor and predecessor, combined with transmission gates. Carry-out circuit obtained by cascading pass transistor logic circuits consisting of positive and negative ternary inverter circuits.

Fazel Sharifi et al.[24] designed ternary full adder using ternary inverters and a buffer. The Sum output generated with two approaches. In the first approach, two cascaded Standard Ternary Inverters (STI) with three capacitors used for the design and the output of STIs passed to the transmission gates. In the second configuration, instead of applying the STIs, the circuit relies on two cascaded ternary buffer gates with three capacitors and these STBs outputs summed using the transmission gates to give the output at Sum. Ternary buffer used for producing the Cout. The utilization of Standard Ternary Buffers (STB) in the full ternary adder diminishes the delay in the circuit compared to the STIs.

Erfan Abbasian et al.[25] illustrated ternary half adder circuit, to get the Sum and Carry Output, Unary Operators are used. The system with single input and single output termed as Logic gates referred as Unary Operators.

Based on the literature survey, implementation of ternary full adder based on conventional design using binary logic gates as intermediate stage requires high number of transistors producing high PDP,[7] implementation of ternary full adder based on pass transistor logic with ternary multiplexers requires medium transistor count which produces medium PDP[12] and finally, ternary full adder designed with unary operators and ternary multiplexers reduces the transistor count produces the low PDP.[22]

GNRFET Transistor Based Ternary Logic

MOS – Armchair GNR field-effect transistors with different threshold voltages, suitable for multi-valued logic, used in this design. GNRFET utilizes Graphene Nano Ribbons as channel material is shown in Fig.1. The hexagonal structure of graphene arranged in a single layer of carbon atoms has exceptional mechanical, electrical, and thermal capabilities.[1] GNRFETs exist in two types: Schottky-Barrier GNRFETs and MOS GNRFETs.

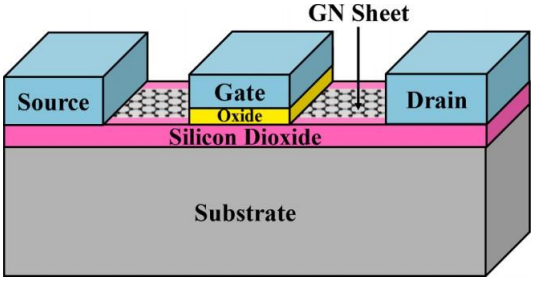


Fig. 1: Structure of GNRFET

Graphene, a single and densely packed sheet of carbon atoms as shown in Fig. 2, has extraordinary electrical characteristics, such as high carrier concentration, outstanding thermal conductivity, and high electron mobility.[4] Band gap in GNRs is tunable as the bandgap of ribbon widens with the GNRs width, which makes it feasible to utilize GNRs in semiconductor

devices. These properties of GNRFETs contribute to better switching performance and lower power consumption.

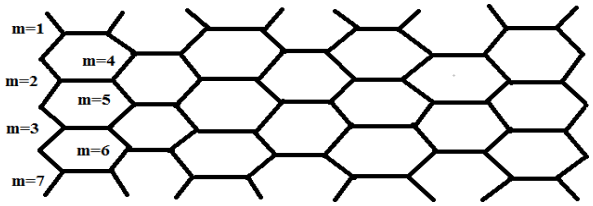


Fig. 2: Hexagonal Structure of Graphene

GNRFETs can have both metallic and semiconductor properties depending on the formation of shape of their edge and based on these properties GNRs named as Armchair GNRs (AGNRS) and Zig Zag GNRs (ZGNR). AGNRs, created by breaking the lattice so that the carbon atoms at its edges form a pair known as dimers. Depending on the formation of edge, the edges of Armchair GNRS have semiconducting properties. The electronic properties of AGNRs associated with their width and determined by the count of dimer lines [3], GNRFETs 2-Dimensional view is shown in Fig.3.

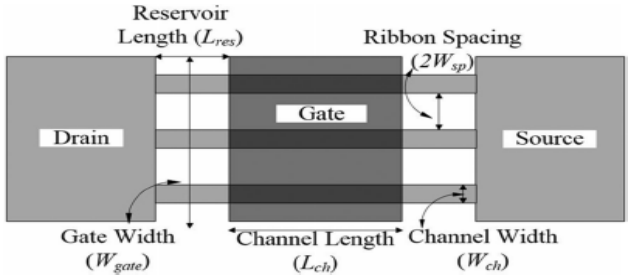


Fig. 3: 2-D View of GNRFET

The proposed design, based on unbalanced ternary logic with three supply voltages (0, VDD and VDD/2) which requires two threshold Voltage of AGNRFETs for using three logic states. Table.1 shows the main GNRFET parameters used in this paper.

The semiconducting behavior of the graphene nanoribbons (GNRs) depends on the number of dimer lines (N) in the GNR structure. Specifically, the GNRs show improved semiconducting behavior when the N = 3P or N = 3P+1, where P is an Integer.[3] Fig.4 shows the GNRFET Current-Voltage characteristics curve for three values of N which are simulated at room temperature using SPICE compatible model. The threshold voltage of MOS-GNRFET can be determined by choosing the appropriate values of dimer lines (N) [5,6]. Thus, GNRFETs threshold voltage has been altered by changing the dimer lines of the GNRs.

The choice of threshold voltage (Vth) in Graphene Nanoribbon Field Effect Transistors (GNRFETs) determines

Table 1: Main GNRFET Parameters

S. NO	Parameters	Values
1.	Ribbons Numbers of GNR	3
2.	Length of the Physical Gate (Lgate)	32nm
3.	Thickness of the Gate Oxide Material (Tox)	1.5n
4.	Distance Between Two Adjacent GNR, Ribbon Spacing (sp)	2n
5.	Dimer Lines Number (N)	7 and 9
6.	Line Edge Roughness Percentage	0
7.	Doping Fraction, (Dop)	0.005
8.	Substrate Oxide Thickness, Tox2	20n
9.	Temperature (°c)	27
10.	Supply Voltage	0.9

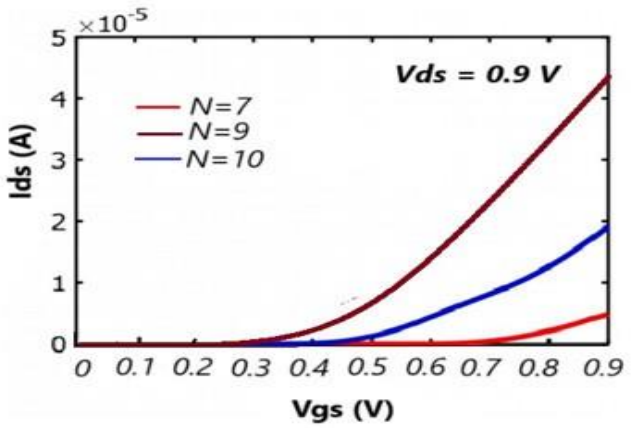


Fig. 4: Current-Voltage Characteristics of N-type GNRFET

device performance together with power efficiency and circuit reliability. GNRFETs utilize graphene nanoribbon quantum confinement to modify threshold voltage because traditional MOSFETs depend on doping levels and gate oxide thickness for Vth control. The nanoribbon width determines Vth values because narrow ribbons generate higher bandgaps that increase Vth but wider ribbons produce lower Vth.

Table.2 shows the ON-OFF status with dimer lines and threshold voltage of the MOS GNRFET. Armchair MOS GNRFET has higher ON-to-OFF current ratio compared with Schottky Barrier GNRFET because they are heavily doped with GNR reservoirs for their source and drain contacts and MOS AGNR with threshold voltage of Vth = 0.6V, 0.24V and N=7, N=9 dimer lines are used in this paper [3-5], and the gate width of GNR is derived using the equation (1) and equation (2)

$$Wch = \sqrt{3}/2\ dc\text{-}c\ (N-1) \quad (1)$$

$$Wgate = (Wch + 2\ Wsp) * nribbon \quad (2)$$

Where, dc-c is the carbon to carbon bond distance (0.142nm)

N is the number of dimer lines.

Table. 2 Operation of MOS GNRFET showing when the transistor is open and close

S. NO	MOS GNR	Dimer lines - N	Threshold Voltage - Vth	Gate Voltage		
				0V	0.45V	0.9V
1	P GNR	7	-0.6	ON	OFF	OFF
		9	-0.24	ON	ON	OFF
2	N GNR	7	0.6	OFF	OFF	ON
		9	0.24	OFF	ON	ON

Thus, MOS GNRFETs is suitable for designing the ternary logic circuits such as adders, multipliers, etc. GNRFETs can be operated with low-power consumption and contribute to faster switching speed compared to the traditional CMOS transistors. AGNRFET with its high-speed operations have greater potential used for high frequency application in Nano electronics.

Proposed Approach for Ternary Full Adder Design

Two different approaches, used in the proposed GNRFET Ternary Full Adder design, in first approach, the design technique starts from Unary Operators, 3:1 ternary multiplexer and 2:1 ternary multiplexer to generate the Sum and Carry. In Second approach, the design technique starts from Unary Operators, 2:1 ternary multiplexer (2:1 TMUX) and 3:1 ternary multiplexer (3:1 TMUX) to generate the Sum and Carry.

Table 3: Unary Operators - Truth Table

S. NO	Input (K)	PTI (Kp)	NTI (Kn)	Cyclic Operator (K1)	Cyclic Operator (K2)	1. $\overline{Kn}$	1. $\overline{Kp}$	Decisive Literal K1	Complement of Decisive Literal or K1K
1	0	2	2	1	2	0	0	0	2
2	1	2	0	2	0	1	0	2	0
3	2	0	0	0	1	1	1	0	2

Unary Operators Design

Unary Operators are defined as K-valued logic system with single input and single output. The Unary Operators used in this design, taken from,[3] where K is ternary input, Kp is Positive Ternary Inverter, Kn is Negative Ternary Inverter, K1 and K2 represented as Cyclic operators, K1 and are Decisive Literal and Complement Decisive Literal respectively. The Circuit diagram for Unary Operators is shown in Fig.5 and Table.3 shows the Truth Table of Unary Operators.

The mathematical expressions for the NTI and PTI, given in equations (3) and (4)

$$Kn = \begin{cases} 0, if K \neq 0 \\ 2, if K = 0 \end{cases} \quad (3)$$

$$Kp = \begin{cases} 2, if K \neq 2 \\ 0, if K = 2 \end{cases} \quad (4)$$

The mathematical expressions for the Cyclic Operators, given in equation (5) and (6)

For Successor (Cyclic Operator - K^1)

$$K^1 = K+1 \quad (5)$$

For Predecessor (Cyclic Operator - K^2)

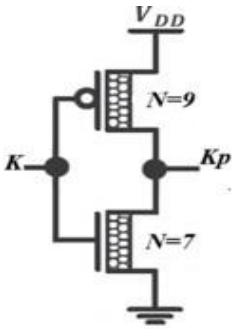
$$K^2 = K+2 \quad (6)$$

Proposed Ternary Multiplexers Design

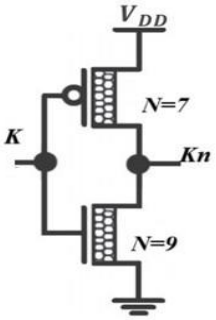
In this section, two types of transmission gate based ternary multiplexers such as 3:1 ternary multiplexer which is shown in Fig.6 and 2:1 ternary multiplexer which is shown in Fig.7 are used. The transmission gates can be ON are OFF and it will pass either 0, 1 or 2 according to the threshold voltage of the GNRFET.

The ternary inputs and the Unary Operator output are given as input lines and selection inputs for the transmission gate based 3:1 TMUX. According to the ternary inputs with respect to the select lines the 3: 1 TMUX produces the output.

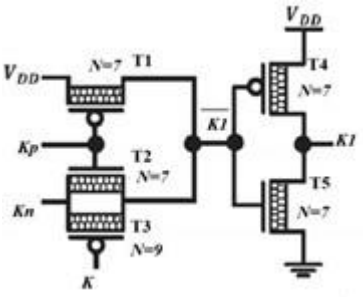
The Unary Operator output is given as input lines and Cin as selection inputs for 2:1 TMUX, with four transistors proposed in this paper.



a. PTI

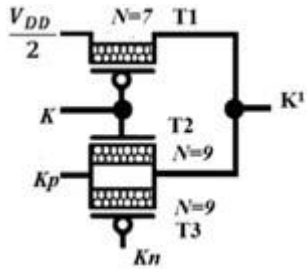


b. NTI



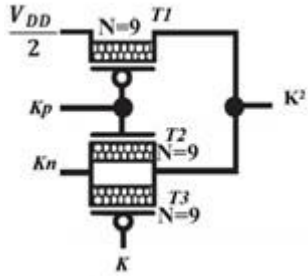
S.No	Ternary input (K)	Logic 0	Logic 1	Logic 2
1	Transistor 1 (T1)	OFF	OFF	ON
2	Transistor 2 (T2)	ON	ON	OFF
3	Transistor 3 (T3)	ON	ON	OFF
4	Transistor 4 (T4)	OFF	ON	OFF
5	Transistor 5 (T5)	ON	OFF	ON

c. Decisive Literal and its Complement (K1 and $\overline{K1}$) with its circuit operation



S.No	Ternary input (K)	Logic 0	Logic 1	Logic 2
1	Transistor 1 (T1)	ON	OFF	OFF
2	Transistor 2 (T2)	OFF	ON	ON
3	Transistor 3 (T3)	OFF	ON	ON

d. Cyclic Operator (K1) with its circuit operation



S.No	Ternary input (K)	Logic 0	Logic 1	Logic 2
1	Transistor 1 (T1)	OFF	OFF	ON
2	Transistor 2 (T2)	ON	ON	OFF
3	Transistor 3 (T3)	ON	ON	OFF

e. Cyclic Operator (K2) with its circuit operation

Fig. 5: Circuit Diagram for Unary Operators with its Operation

Proposed Approach for GNRFET based Ternary Full Adder

This section discusses the two approaches used for creating the GNRFET-based ternary complete adder with three inputs, A, B, and Cin, and two outputs, Sum and Cout, respectively. The Truth Table of Ternary Full Adder is provided in Table 4, and the general equations for Sum and Carry are shown in equations 9 and 10, respectively.

$$Sum = \{A + B + Cin\} \quad (9)$$

$$Cout = [\{A + B + Cin\}/3] \quad (10)$$

4.3.1 Proposed Approach for First Ternary Full Adder

The proposed approach for first TFA uses Unary Operators along with four 3:1 TMUX and two 2:1 TMUX for executing

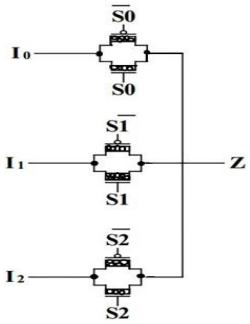


Fig. 6: The proposed 3:1 Ternary Multiplexer Circuit Diagram

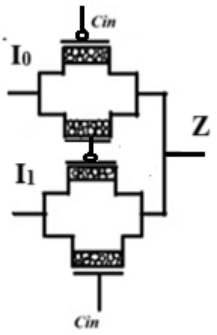


Fig.7 The proposed 2:1 Ternary Multiplexer Circuit Diagram

the Sum, Carry Out of ternary full adder. The proposed ternary full layout diagram is shown in Fig.8 and full adder1 circuit diagram is shown in Fig.9.

Ternary input namely A, B and Cin enter as inputs to the unary operator circuits. Then, the Unary Operator outputs, given as inputs to 3:1 TMUX and the output of these 3:1 TMUX provided as input to the 2:1 ternary multiplexer to produce the Sum and Carryout results of TFA1. The Unary Operator outputs, given as inputs to 3:1 TMUX and the output of these 3:1 TMUX, provided as input to the 2:1 ternary multiplexer to produce the Sum and Carry results of TFA1.

The operation of the first TFA Sum, analyzed from the input A, A2 and A1 first transmission gate based 3:1 TMUX (second 3:1 TG based TMUX) and the first transmission gate based 2:1 TMUX (second 2:1 TMUX) to produce the Sum, Carry Out can be analyzed as same as Sum.

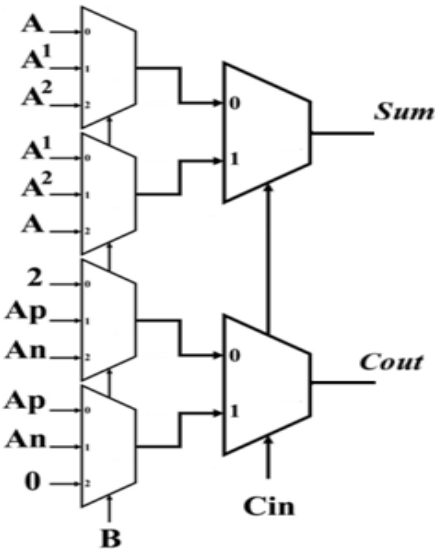


Fig. 8: Layout of Ternary Full Adder First Approach

Table. 4 Truth Table - Ternary Full Adder

S.NO	A	B	Cin	Sum	Carry
1	0	0	0	0	0
2	1	0	0	1	0
3	2	0	0	2	0
4	0	1	0	1	0
5	1	1	0	2	0
6	2	1	0	0	1
7	0	2	0	2	0
8	1	2	0	0	1
9	2	2	0	1	1
10	0	0	1	1	0
11	1	0	1	2	0
12	2	0	1	0	1
13	0	1	1	2	0
14	1	1	1	0	1
15	2	1	1	1	1
16	0	2	1	0	1
17	1	2	1	1	1
18	2	2	1	2	1

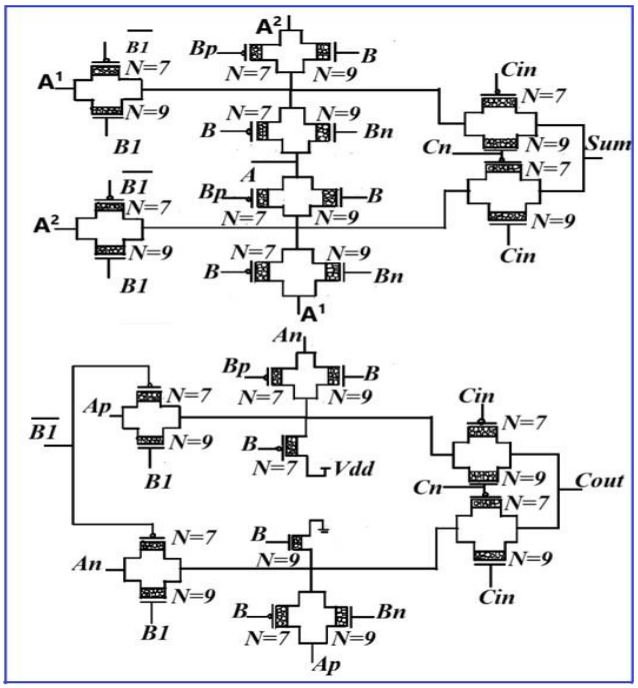


Fig. 9: Ternary Full Adder First Design - Circuit Diagram

4.3.2 Proposed approach for Second Ternary Full Adder

The proposed approach for the second TFA2 design combines Unary Operators together with six 2:1 TMUX and two 3:1 TMUX, to generate the Sum and Carry. The proposed TFA2 design layout diagram is shown in Fig.10 and TFA2 Circuit diagram is shown in Fig.11. Ternary input namely A, B and Cin enter as inputs to the unary operator circuits. Then, the Unary Operator outputs given as input to the 2:1 TMUX and the output of the 2:1 TMUX, fed as inputs to the 3:1 TMUX to produce the Sum and Carry results of TFA2.

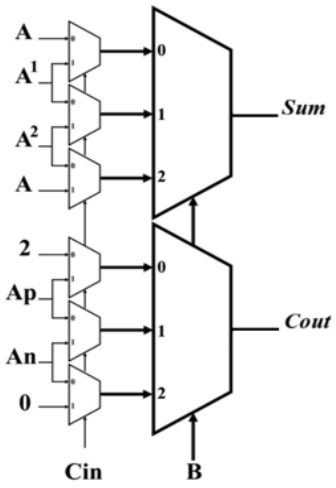


Fig. 10: Layout of Ternary Full Adder Second Design

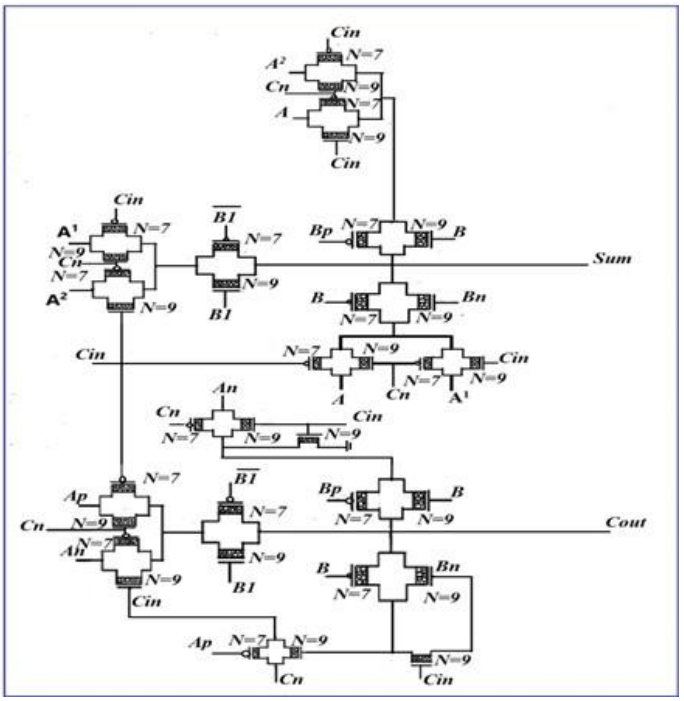


Fig. 11: Ternary Full Adder Second Design - Circuit Diagram

Results of Simulation snd Discussions

The proposed 32nm GNRFET-based TFAs, designed and simulated using HSPICE simulator and the following parameters are used for simulation: Voltage =0.9V, Temperature = 27° C, rise time and fall time of the signals are provided as 10 ps, simulated output results compared with existing CMOS technology and CNFET-based technology TFAs with the literature papers [7,8,9,10,11,12,21]. Based on the observation from the output, Table.5 provides the result of proposed TFA approaches with the transistor count, power consumption, maximum delay and power delay product with lowest values highlighted in bold indicates that GNRFET TFA2 exhibits better performance.

The comparative result analysis of proposed GNRFET TFA approaches with the CMOS and CNTFET TFA designs based on the literature survey provided in Table.6 and the results indicate that proposed GNRFET TFA2 exhibits better performance with lowest PDP compared with the literature papers [7,8, 9,10,11,12,21].

The proposed GNRFET-based TFAs simulated transient response, verified according to the Truth Table. 4, based on the one input logic and one output logic of unary operators, Fig.12 represents the proposed GNRFET TFA1 approach simulated transient response and Fig.13 represents the proposed GNRFET based TFA2 approach simulated transient response respectively.

Table 5: Results of proposed GNRFET TFAs with Power, Max Delay and PDP

S.NO	Metrics	GNRFET 1	GNRFET2	Improvement (%)
1	Transistor Count	98	68	30.61%
2	Avg Power (μW)	56.51	18.056	68.05%
3	Max Delay (ps)	17.58	5.427	69.13%
4	Power Delay Product ($\times 10^{16}$ J)	9.93	0.97	90.23%

Table 6: Comparison Results of Proposed GNRFET TFAs with CNTFET TFAs based on Literature papers

S. NO	TFA/Year	Technology Model	Avg Power (W)	Maximum Delay (s)	PDP (J)
1	In [7] 2016	CMOS	1.29 μw	81.67ps	1.05 e-16
2	In [8] 2003	CMOS	12.32 μw	756.2ps	9.31 e-15
3	In [9] 2006	CMOS	7.16 μw	500.6ps	3.59 e-15
4	In [10] 2011	CMOS	3.92 μw	1871ps	7.35 e-15
5	In [11] 2017	CMOS	2.11 μw	606.2ps	1.28 e-15
6	In [12] 2014	CNTFET	1.45 μw	100ps	1.45 e-16
7	In [13] 2023	CNTFET	0.22 μw	34ps	7.48 e-18
		CNTFET	0.46 μw	27ps	12.42 e-18
8	In [15] 2021	CNTFET	127.85nw	98.24ps	12.5 e-18
9	In [21] 2016	CNTFET	0.824 μw	146ps	1.206 e-16
10	In [23] 2017	CNTFET	205nw	18.2ps	3.73 e-18
11	Proposed TFA1	GNRFET	56.51 μw	17.58ps	9.93 e-16
	Proposed TFA2	GNRFET	18.056 μw	5.427ps	0.97 e-16

The fabrication viability of a GNRFET-based Ternary Full Adder (TFA) is very promising at the research level but it presents enormous challenges for mass integration. The advantages of GNRFETs include high carrier mobility, scaling to sub-10 nm dimensions, and tunable bandgaps, which place them in a good position for ternary logic applications. But accurate production of graphene nanoribbons with a controlled width and sharp edges is challenging, and the existing methods such as chemical vapor deposition and lithography are not reliable enough for mass production. However, GNRFETs are very compatible with multi-valued logic architectures because GNRFTEs can accommodate multi-threshold voltages, which means reduced circuit complexity and less power consumption. Although not directly compatible with the conventional CMOS, the ternary circuits based on GNRFETs have an opportunity for future integration via hybrid or emerging technologies.

The scalability of the proposed GNRFET-based ternary full adder is high because of the nanometer-scale dimensions of graphene nanoribbons and their suitability to multi-threshold designs. However, process variations like edge roughness and width fluctuation have huge effects on the threshold voltage and signal integrity in ternary logic levels.

Conclusion

This paper successfully proposed the GNRFET Ternary Full Adder with two approaches using HSPICE Simulator. The results for GNRFET-based TFAs indicated that they performed better in terms of power consumption, maximum delay, and Power Delay Product. Ternary logic will play a major role for developing future generation integrated circuits, it will reduce the area of the chip, computation speed will increase, and it will be helpful for many IoT and Embedded devices to function effectively with reduced power consumption for future integrated circuits. Optimizing the number of dimer lines of GNRFETs has the potential to enhance circuit efficiency and response speed. The versatility of GNRFETs positions them as an alternate to CMOS technology for developing energy efficient, low power ternary logic designs in Nano scale applications.

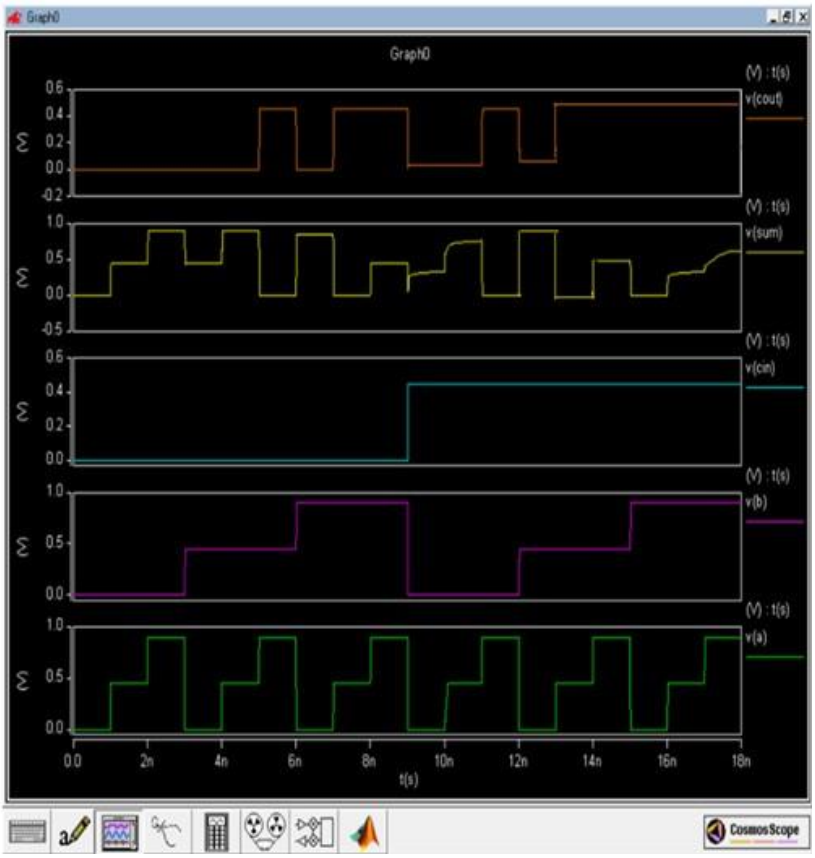


Fig. 12: Output Waveform for the proposed TFA1 - Transient Response

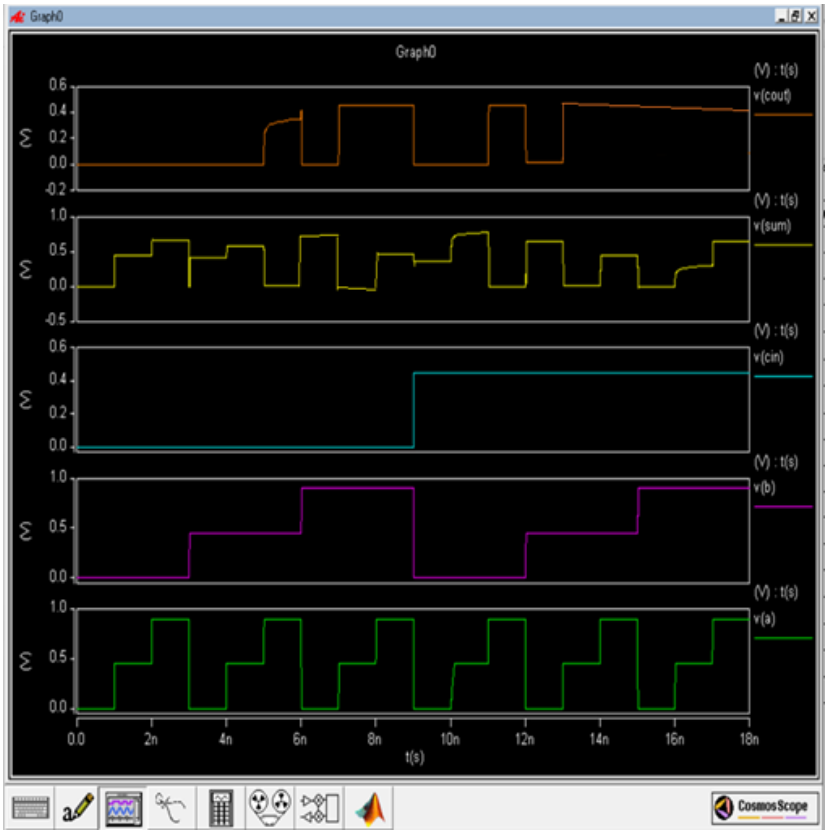


Fig. 13: Output waveform for the proposed TFA2 - Transient Response

Conflict of Interest

All authors declare that they have no conflict of interest.

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