ISSN:2582-1458
https://doi.org/10.31838/jvcs/02.02.06

Research Article

Design of Set Based D Flip-Flop for High-Speed Applications

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Received: 14.10.20, Revised: 20.11.20, Accepted: 06.12.20

ABSTRACT:
Increasing demand of portable devices creating larger scope in the field of Low power device design. VLSI designing of the efficient circuits is aiming towards the devices consuming less power and produces less delay with capability to operate in wider range of frequencies. This research paper proposes the modified Single Edge Triggered (SET) D-flip flop design for the low power applications. The earlier proposed design is tested for various substrate bias techniques in sub threshold region to opt for better design.

Keywords: SET DFF, low power, high speed

Introduction

The ever increase of portable based applications such as laptops, mobile devices and PDAs it requires the high speed and low power. As long as the devices are operated in the high frequency which tends to dissipates the huge amount of power. Hence this may indirectly impacts the reliability of the circuit, therefore building the circuits with the help of the low threshold voltage levels it eventually consumes the low power and virtually enhances the reliability of the device. The clocking circuits D-flip flops are major building blocks and it should consume the 30% to 50% of the total power in the system. The logic delay in the clock circuits are reduced by the 25% of the high performance of the microprocessors, and approaches to the 10% of its actual value.

Background and proposed circuit

Flip-flops can be deigned based on the dynamic and static nature. The dynamic FF produces the charge leakage from the FF can be removed for the output capacitance. The static FF on the other hand significantly plays the prominent role on the biasing of the transistors in order to control the voltage. And also it eliminates the inherent noise on the transmission gates. Figure 1 depicts the conventional D flip flop using SET condition.

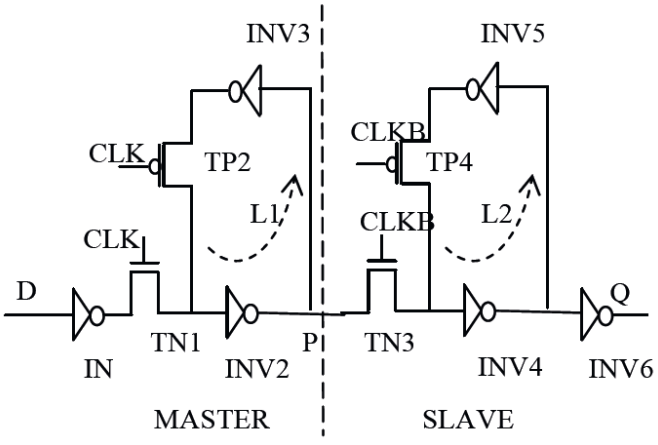

Fig.1: Conventional SET D flip-flop.

The design of the 10 transistors has the edge triggered SET D flip flop and which is shown in the figure 2.In the feedback based flip flop having the a loop and transmission gate. When clock is set to high and master latch is functional condition and the slave latch becomes on active condition when loop1 becomes functional and produces the data output in Q1 and Q2 respectively.

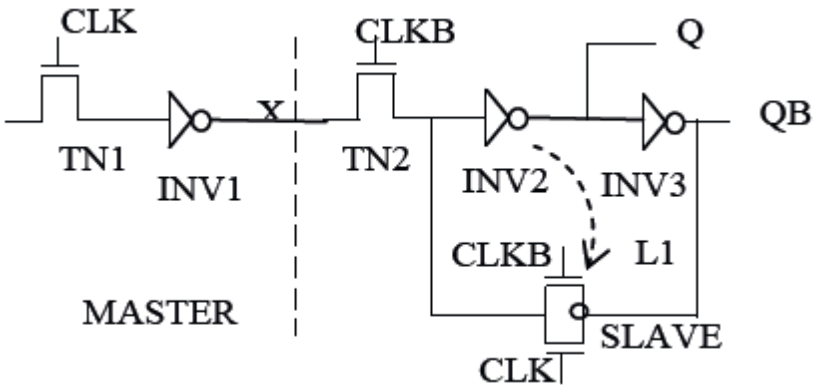

Fig.2: 10 transistor set D flip-Flop.

Table 1: Aspect ratio of the CMOS transistors in the D-FF

Transistor	Aspect Ratio (W/L)
TN1	22 / 0.6
INV1 – NMOS	22 / 0.6
INV1 – PMOS	22 / 0.6
TN2	22 / 0.6
INV2 – NMOS	22 / 0.6
INV2 – PMOS	22 / 0.6
INV3 – NMOS	2 / 0.6
INV3 – PMOS	2 / 0.6
TG – NMOS	2 / 0.6
TG – PMOS	2 / 0.6

The power consumption of the proposed SET D flip flop has the effect on the output and it has the wired behaviour as long as the frequency is ingress the quit normal way.

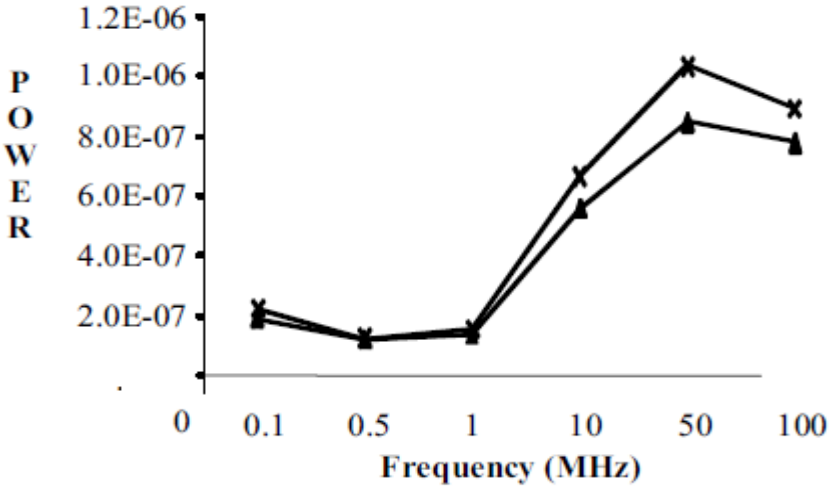

Fig.3: Power consumption of D FF in CMOS 65nm technology.

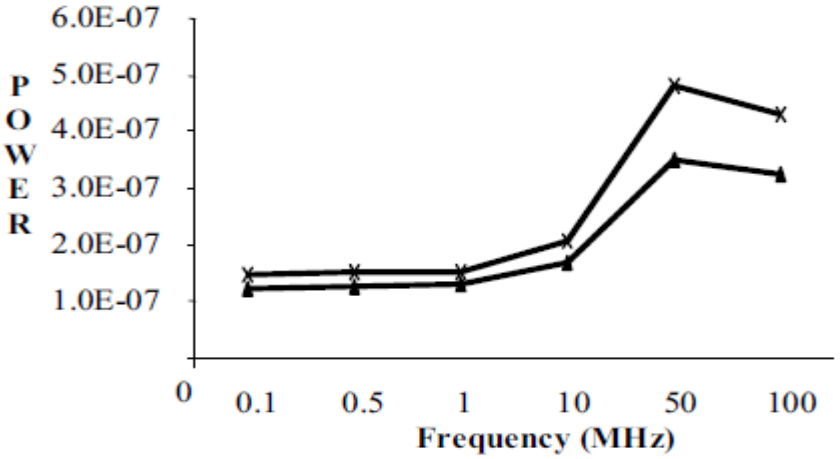

Fig.4: Power-Delay Product at various frequencies in 65nm technology in Percentage scale.

Conclusion

In the low power applications and high speed data transmission these SET D flip flops are placing the critical role in the current day modern day emergencies and it has the avoid the body effect condition .

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