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A Novel Investigation on p-GaN GATE with and without AlGaN Back Barrier for AlGaN/GaN High Electron Mobility Transistors

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Abstract

p-GaN layers are relatively mature and controllable, making p-GaN HEMTs the leading structure that is most likely to be commercialized. The analysis of the gate design parameters, such as transconductance, breakdown voltage, threshold voltage, Johnson Figure of Merit (JFOM), and gate turn-on current of p-GaN devices, which determine the on-state characteristics, needs to be investigated. The AlGaN barrier, p-GaN gate, GaN, AlGaN back barrier, and SiC substrate constitute the structure of p-GaN, which is operated in the E-mode. The use of an AlGaN back barrier reduces the punch-through current. Silicon carbide (SiC) is used as a substrate to have lower lattice mismatch with the nitride layer. The transfer characteristics, transconductance, threshold voltage, breakdown voltage, and JFOM are analyzed. The device demonstrates a positive threshold voltage that varies linearly with changes in ambient temperature. In addition, the device featuring an AlGaN back barrier shows a higher breakdown voltage of 105 V, in contrast to the device lacking a back barrier.

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Introduction

To offer adequate safety conditions for switching applications, normally off high electron mobility transistors (HEMTs) are required. It is necessary to construct an enhancement mode device since power electronics systems do not require depletion-mode or normally on devices. The usage of fluorinated gate dielectrics, recessed gate structures [1], pGaN gates, and pAlGaN gates, and cascading an enhancement mode device with a low-voltage normally off Si device are a few efficient methods to do this, each with their own advantages. A p-GaN gate AlGaN/GaN HEMT emerged as a leading solution for failsafe operation and circuit complexity reduction among many techniques to implement enhancement mode (e-mode) operation. However, the highest gate operation voltages (VG-max) for p-GaN gate HEMTs are typically between 6 and 8 V because of the comparatively low gate breakdown voltage (BV) (often 10-12 V) [2]. The gate driver design has been constrained by the modest gate voltage swings, which has decreased longevity [3]. Using strained films, p-GaN gate HEMTs have been successfully optimized. They have shown that a negative polarization-induced charge density may be produced in the gate area by using the mechanical interaction of compressive films, resulting in a temporary increase in electron confinement. This results in a better trade-off between threshold voltage (VTH) and on-resistance (RON), where VTH can be raised without

affecting RON. A bigger design margin can be achieved by combining this approach with an AlGaN back-barrier, which they have also demonstrated [4]. An enhancement-mode GaN HEMT structure was designed through two-dimensional device simulations. A p-type doped buffer was incorporated to achieve improved device characteristics and reliable performance. The RON of the device was analyzed and estimated to be comparable to conventional HEMTs. The electric field profiles suggested a lower breakdown in the case of doped buffer as compared to the case of an undoped one, which may be overcome by optimizing the buffer design such as lowering the acceptor concentration, patterning it under the source and gate, and adding field plates. Finally, the RC delay in the pGaN back HEMT was calculated to estimate the switching performance. These results demonstrate the potential of the proposed pGaN back HEMT in achieving a threshold that is much larger than it is possible in conventional HEMT. [5] proposed a study of the frequency dependence of the reliability of pGaN Gated GaN HEMTs from the market. To comprehend the cause of deterioration better at the device level, studies at the circuit and device levels were carried out. Their tests showed a definite correlation between switching frequency and gate voltage stress and device degradation. Furthermore, a rise in gate current was accompanied by a nonlinear decrease in overshoot. Efficiency suffers as a result both during and after degradation episodes. Furthermore, it was shown that the breakdown was dependent on frequency. Trap-related events in the devices' gate structure have been blamed for this phenomenon. [6] have proposed p-GaN gate AlGaN/GaN power HEMTs have been shown to exhibit non monotonic dynamic RON behavior with rising OFF-state stress bias. We have investigated this phenomenon using calibrated 2D numerical device simulations. They have demonstrated that during the OFF-state phase of the pulse-mode tests, holes detrapping from buffer traps within the gate–drain access zone are what cause the dynamic RON to increase relative to its static value. The holes produced by a high electric field mechanism that get captured in C-related traps and partially neutralize the negatively ionized acceptors are what cause the recovery of RON at significant drain stress bias. Reference [7] have proposed a model p-GaN HEMT. that regulates channel potential to increase BV and VTH stability. The clamping channels potential for P-HEMT is generated by a somewhat recessed p-GaN layer (PR p-GaN layer). The two-dimensional electron gas (2DEG) channel of the PR p-GaN layer is depleted to withstand the effects of high drain bias in the device.The channel potential at the p-GaN layer's drain side is clamped to improve BV and VTH stability. The BV is increased by 120% compared to the conventional p-GaN HEMT (C-HEMT), and the VTH stability caused by high drain bias is increased by 490% for the same RON, according to simulation data. In addition, the impact of the PR p-GaN layers; length, thickness, and doping density on the stability of the BV and VTH are investigated. The static transfer and output characteristics are exactly the same as those of a C-HEMT, and the overall switching loss is increased at 500 kHz by less than 7.8%. We also examined the effects of the PR layers; length, thickness, and doping density on performance. [8] have proposed that comparison to the BV of p-GaN HEMTs on SiC is much greater than the conclusions for grounded silicon substrates for p-GaN HEMTs. With the substrate grounded, the vertical BV for the p-GaN-on-SiC material was more than 3 kV. Furthermore, with a minor VTH shift, the maximum drain current at 48% for a temperature at 300 [9] proposed a thorough simulation investigation of the unique device construction that combines a p-GaN back barrier layer into the conventional AlInN/AlN/GaN gate-recessed enhancement-mode HEMT device in order to reduce short channel effects, gate leakage, and improve frequency performance [28-30]. The proposed device transfer characteristics, including its transconductance (gm), gate leakage current (Ig), drain-induced barrier lowering (DIBL), subthreshold slope (SS), threshold voltage (VTH, on-current off-current ratio (Ion/Ioff), gate capacitance (Cgg), and cutoff frequency, are analyzed through simulations. The proposed device with a p-GaN rear barrier layer is compared with the device without a back barrier layer. The use of p-GaN back barrier layer involves generating higher positive VTH and enhances fT because of the depletion effect, decreased Ig, reduced DIBL, and capacity to prevent the SS from degrading. fT up to 123 GHz is particularly impressive compared to the device without a back barrier 70 GHz. The channel maximum electric field is 1.17 MV/cm, which is an order higher than that of a typical GaN buffer. Because of the increased electron concentration in the channel, the drain current is 332 mA/mm. With back barrier, transfer properties and ION/IOFF ratio are enhanced. InAlN back barriers have higher ION/IOFF ratios than InGaN back barriers, making them more dependable and power-efficient than p-GaN/AlGaN/GaN devices. Yi-Sheng Chang proposed HEMTs with composited barriers and normally off operation mode made of pGaN/AlN/AlGaN/GaN structure. After running under pulsed current-voltage stress, the composited barriers can successfully reduce plasma-induced damage, which in turn reduces the increase in dynamic RON. In the suggested composited barriers p-GaN gate construction of HEMT, the good electrical features of maximum drain current density and low subthreshold swing (SS) may be

attained [31]. The composited barriers' design with the addition of an AlN capping layer can enhance the plasma damage induced in current collapse and dynamic on-state resistance. Reference [10] using p-gallium nitride (GaN) gate HEMTs with normally OFF single-layer intrinsic and fluorinated graphene as gate insertion layers (HEMTs). They employed graphene as an insertion layer beneath the gate metal stacks, which form an Au/Ti/graphene/p-GaN stack in the center and an Au/Ti/graphene/SiNx stack on either side, to reduce gate leakage and boost gate BV. Reference [11] proposed two different epitaxial structures—one with a high resistive GaN buffer layer and the other with an AlGaN back-barrier—that are evaluated in terms of their VTH, drain current density, and buffer leakage current. GaN layer in the epitaxial structure, which has a high resistivity and a VTH of +0.5 V, enables normally off operation. The VTH was increased to +2 V with the installation of the AlGaN back-barrier, and the buffer leakage current was significantly decreased. The p-GaN/InAlN/GaN structure obtains a positive VTH of +0.5 V with the addition of an AlGaN back-barrier [32]. which is subsequently increased to +2 V. AlGaN back-barrier devices also exhibit five orders of magnitude that reduced buffer leakage currents. By adding and increasing the Al content of the barrier layer or adding an AlN spacer layer between the barrier layer and the GaN channel could reduce the drain current observed in systems with an AlGaN back-barrier. The presence of an AlGaN back-barrier results in observable current flow in the system.

Structure of p-GaN HEMT

The VTH can be improved by connecting the layer of p-GaN to an electrode source. In this case, the source-connected p-GaN layer extends its depletion width. Therefore, the VTH is increased from 0.93 volt to 2.44 volt. The source-connected p-GaN device is also given the drain current of 350 mA for a gate width of 1 mm. Its noticeable that the VTH is improved without compromising the drain current. However, the negative side of the source-connected p-GaN HEMT has higher gate leakage. The gate leakage for normal HEMT and source-connected p-GaN HEMT are 10^{-5} A and 10^{-3} A, respectively. Therefore, future research needs to reduce the gate leakage in source-connected p-GaN HEMT. The p-GaN is used not only to increase the VTH but also to improve the reverse blocking voltage. This can be attained using the p-GaN island. The use of p-GaN island yields higher voltage breakdown of 1092 V and low RON of 8.3 mΩ·cm^2. This performance is achieved at the gate-to-drain distance of 22 μm, and this is a large gate-to-drain distance. Further, the use of p-GaN Island may induce surface traps. The surface strap is a serious concern in switch and RF application. In switching application, the traps increase the switching loss [12] and thereby the efficiency will be reduced in power converters [13]. Further, the surface traps also induce the gate lag, which limits the fast-switching feature. In the case of RF application, the surface traps [14] induce current collapse and increases the dynamic RON. In 2012, the IMEC and IBM demonstrated VTH in the range of −4V to −3V. In 2013, Texas A M demonstrated the VTH in the order of −2V. 2011, MIT also demonstrated the VTH in the order of −2V. The Texas and IMEC also demonstrated positive VTH in the order of 1V. In 2013, Samsung demonstrated the highest VTH of 3V. Although, these companies demonstrated a positive VTH, the BV needs to improve further. In the work, it used p-GaN gate and back-barrier to obtain a positive VTH as well as improved BV.

p-GaN HEMT Principles

[15]The p-GaN HEMT is compared to conventional D-Mode HEMT and is well explained using various parameters such as energy profile, electron concentration, hole concentration, and an equivalent circuit model. Hence, these parameters are analyzed one by one. The energy profile of p-GaN HEMT for various drain and gate bias are shown in Figure 1(A) and Figure 1(B) The upper and lower lines of the solid represents valence band and conductance band, respectively [16]. The Fermi level is represented by a dotted line where 50% of the electron is located. In the bottom of the figure, the vertical stack, such as p-GaN, AlGaN, and GaN, is shown. For Vds=0V and Vgs=0V, the conduction band is above the Fermi level. As Vgs increased to a positive voltage, the conduction band goes below the Fermi level at GaN/AlGaN interface. In all other regions, this band of conductance is above the Fermi level.

In Figure 2 (A), Figure 2(B), and Figure 2(C), the electron concentration and current flow line for various gate biases with VG is Vgs. For Vgs=0V, there is no electron in the channel below the gate. Therefore, the drain-to-source current is zero. In case of the d-mode HEMT, electrons are available in the entire channel and hence the current flows for Vgs=0V. For E-Mode HEMT, for Vgs> VTH and < forward voltage (VF), the electron is available in the entire channel. Therefore, the current is not zero. In the case of Vgs > forward voltage, holes are injected by p-GaN to the channel. Therefore, drain-to-source current reduces [21-27].

An equivalent circuit of p-GaN HEMT is shown in Figure 3. This circuit consists of two diodes, one MOSFET and

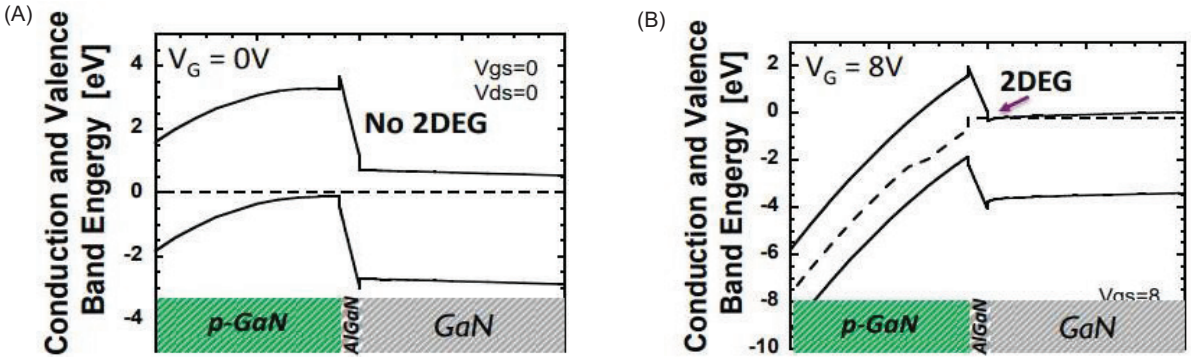

Fig. 1: (A) Conduction and valence bands at Vds=0V and Vgs=0V. (B). Conduction and valence bands at Vds=8V and Vgs=8V [17-20].

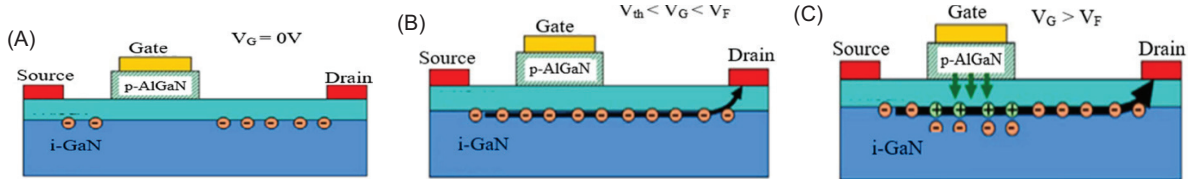

Fig. 2: (A) Electron concentration and current flow line of p-GaN HEMT for various gate biases, VG = 0V. (B) Electron concentration and current flow line of p-GaN HEMT for various gate biases, Vth<VG<VF. (C) Electron concentration and current flow line of p-GaN HEMT for various gate biases, VG>VF.

two junction capacitances. The gate metal and p-GaN layer contribute to the diode (D1). The p-GaN/n-channel/AlGaN stack contributes to the PIN diode (D2). In other words, it is said that the stack is similar to the tunnel FET structure. Therefore, this stack may create carrier tunneling also. In the case d-Mode HEMT, positive-intrinsic-negative (PID) diode structure does not exist. Although the device is having diode kind of structure, it does not have similar I-V behavior as that of the diode I-V behavior. The junction capacitance is Cj1 and Cj2 which are contributed by the separation of conductive regions by space charge region.

Investigated Structure

In recent years, the development of HEMTs has gained significant attention because of their superior performance in power electronics, RF (radio frequency) applications, and high-voltage systems. One promising variation of HEMTs is the use of p-GaN for the gate material, which has led to advancements in achieving higher VTHs and improved breakdown capabilities. This paper discusses the investigated structures of conventional p-GaN HEMTs and a proposed variant incorporating a back-barrier, as shown in Figure 4(A) and Figure 4(B). The proposed structure aims to address certain limitations in conventional p-GaN HEMTs, including punch-through current and lattice mismatch issues. The doping concentrations in both the conventional and proposed

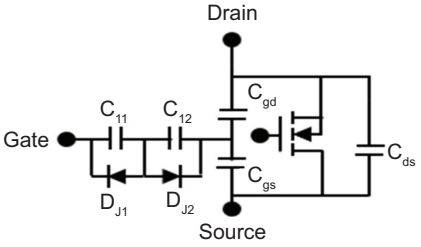

Fig. 3: Equivalent circuit of the p-GaN device.

p-GaN HEMT structures are critical for achieving optimal device performance. As shown in Table 1, the doping concentrations of the AlGaN, GaN, and p-GaN layers are carefully controlled to ensure the desired electrical characteristics. The p-GaN gate is doped to create the necessary voltage control for turning the device on and off, while the AlGaN layers (both the barrier and back-barrier) are typically n-type doped to support the formation of the 2DEG at then GaN/AlGaN interface. The GaN layer is typically undoped or lightly doped to maintain the high electron mobility needed for current conduction. Table 2 provides the thickness values for each of the layers in the device. The thicknesses of the AlGaN and GaN layers are optimized to balance performance and manufacturability. The AlGaN barrier layer needs to be thick enough to induce significant piezoelectric polarization and form a strong 2DEG, while the GaN layer should be thick enough to accommodate the

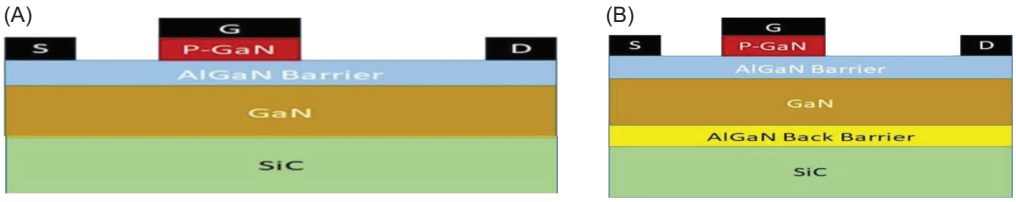

Fig. 4: (A) Structure of the investigated (GaN) p-GaN HEMT without back-barrier. (B) Structure of the investigated (GaN) p-GaN HEMT with back-barrier.

high current densities typical of HEMT applications without suffering from excessive resistive losses. The thickness of the AlGaN back-barrier must also be carefully designed to provide the desired punch-through current reduction without adversely affecting the overall BV.

A lateral dimension used in the simulation is given in Table 3 such as length gate (Lg), gate to drain distance (Lgd), and gate spacing source (Lsg). The gate-source spacing is kept low to reduce channel resistance and source resistance. The higher drain gate distance is used to have higher BV.

The gate model treats the gate as a Schottky barrier, with a work function of 5.2 eV. The Schottky gate allows for efficient control of the channel conductivity by modulating the barrier height at the gate interface, enabling fast switching and high-performance characteristics in the device.

As BV is analyzed in this work, impact ionization model is included in the simulation. The ionization impact model used is the Selberherr model. The ionization impact model has various ionization coefficients. With all the models being defined in the simulation, the simulator solves these models in the device. For this, the entire device is divided into many triangular cells. In other words, the divisions are referred to as meshing in Table 4. There are two kinds of meshing, namely, fine and coarse meshing. Fine meshing is used in important regions like channel and contact area. Coarse meshing is typically used in the substrate area. Physics-based equations are solved using the Newton method.

Results and Discussion

Figure 5 illustrates the potential contour is illustrated under preliminary conditions, where the device is simulated at an initial bias of 0 V drain voltage and 0 V gate voltage. The dark red region corresponds to a higher potential of 1.96 V. The blue region represents the 0V. The other color regions represent the voltage between 0V and 1.96V. As it is simulated in the initial bias condition (Vds=0V and Vgs=0V), the gate, drain, and source

Table 1. Doping in various layers.

Layer	Doping
p-GaN	2×1019 cm^{-3}
AlGaN barrier	2×1015 cm^{-3}
GaN buffer	1.5×1015 cm^{-3}
AlGaN back-barrier	1.5×1015 cm^{-3}
SiC substrate	-

Table 2. Thickness of various layers.

Layer	Thickness
p-GaN	10 nm
AlGaN barrier	25 nm
GaN buffer	0.5 µm
AlGaN back-barrier	400 nm
SiC substrate	50 µm

Table 3: Lateral dimensions.

Layer	Doping
Lgd	6 µm
Lg	1.5 µm
Lsg	1 µm

electrodes are in 0V. The voltage above 0V is a built-in potential.

Figure 6 illustrates the energy profile of the p-GaN HEMT along the vertical axis, which represents the gate-to-substrate direction. In this figure, the green line indicates the Fermi energy, the red line represents the conduction band energy, and the blue line depicts the valence band energy. Fermi energy represents the state where 50% of the electrons accumulate. Conduction band is the region were free or conduction electrons are available. Valence band represents the electrons in the outer orbit of the atom. The energy profile is observed at the gate voltage 0V and drain voltage of 0V. In the p-GaN region, the valence band is uplifted or closer to the fermi level. It is because of higher holes in the p-GaN region by acceptor or p-type doping.

Table 4: Physics-based models.

Model	Description
Consrh	It is a recombination model and depends on the carrier concentration in the semiconductor layers.
Auger	It is a recombination model, and it is effective when current density is high.
Fermi	This model incorporates the statistical behavior of electron and hole.
Temp	This model fixes as the ambient temperature of 300 K during the simulation.
Polarization	This model induces the polarized charges at the interface of semiconductor layers.
Mobility	This model governs the carrier transport in linear
Lat.temp	This model governs the heat flow in the device.

At the AlGaN/GaN interface, the conduction band is above the fermi level, and there is no evidence of quantum well. Therefore, at the zero bias condition (Vds=0V and Vgs=0V), the electron concentration is zero at AlGaN/GaN interface, as illustrated in Figure 7. In other words, the channel is not formed along the AlGaN/GaN interface. Therefore, the device is normally off at Vgs=0V.

In GaN HEMTs, BV is an important parameter. During a hard shutdown, unexpected voltages can develop between the electrodes, necessitating that the BV exceeds these unforeseen voltages. Breakdown can occur defining its safe operating area, which is essential for circuit designers to consider in various applications. Specifically, the bias conditions are influenced by these breakdown points, alongside the application requirements. This study analyses the BV of p-GaN HEMTs with and without a back-barrier, focusing on the off-state conditions. Figure 8 illustrates the off-state drain current as a function of drain voltage for both configurations. In the off-state, the gate voltage is maintained significantly below the threshold. The data show that the drain current remains below 10−7 A when the drain voltage is close to 0V. However, beyond 600V, there is a noticeable increase in drain current, indicative of avalanche breakdown, which occurs because of a rapid generation of electrons. From Figure 8, it can be seen that the BVs for HEMTs with and without the back-barrier are

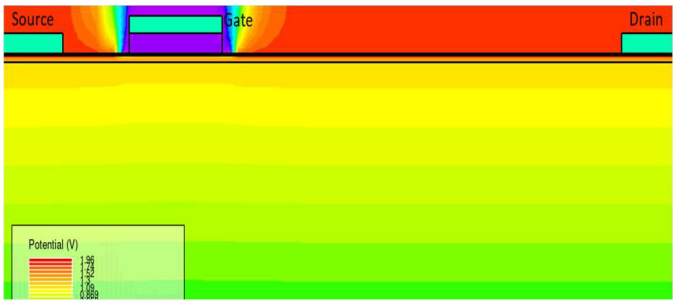

Fig. 5: Potential profile of the GaN HEMT in a TCAD physical simulator.

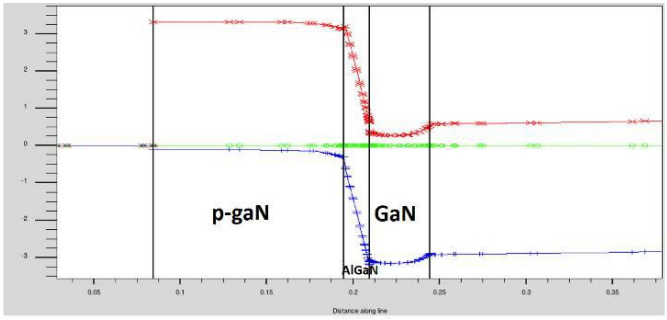

Fig. 6: Energy profile along the vertical axis.

700V and 805V, respectively, with breakdown occurring at a compliance current of 10−5 A. The presence of the back-barrier enhances the BV by 105V, attributed to the reduced surface field resulting from this technique.

Enhancing BV is one of the objectives in HEMT. Figure 9 shows the transconductance versus gate voltage for various ambient temperatures. The ambient temperature is varied as 25°C, 50°C, 75°C, 100°C, 125°C, and 150°C. The p-GaN device in this work has VTH around 1V. The transconductance below the VTH is zero for various ambient temperatures. It is also closer to 0 value for gate voltage above 3V. The transconductance is noted as spikes at gate voltage around 2.5V. Further, it is noted that the peak transconductance decreases with increase in ambient temperature from 25°C to 150°C. The extracted transconductance is plotted against ambient temperature in Figure 10. The transconductance is extracted at the constant gate voltage of 2V. It's interesting to note that the peak transconductance has a linear relationship with ambient temperature.

The relationship between VTH and ambient temperature was examined for both p-GaN HEMTs with and without a back-barrier. In each configuration, this study demonstrates the temperature variations' impact on the VTH, as shown in Figure 11. This evaluation is essential for optimizing device performance and functionality across

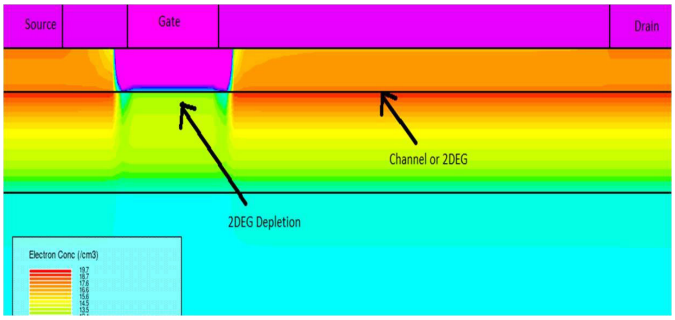

Fig. 7: Electron concentration in the p-GaN gate AlGaN/GaN HEMT.

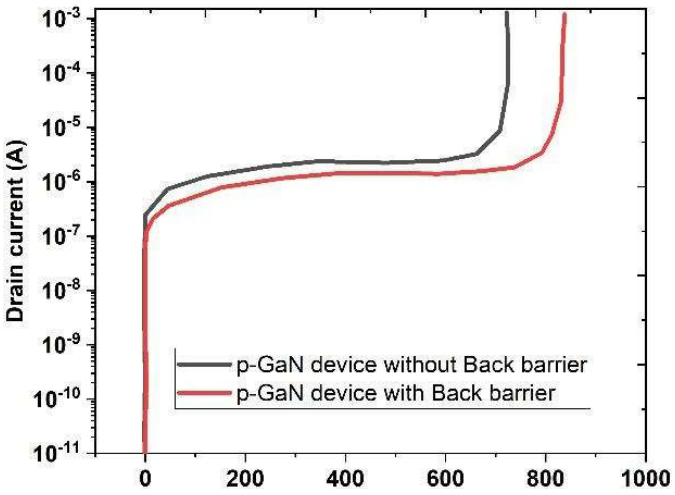

Fig. 8: pGaN HEMT with and without back-barrier for drain current versus drain voltage under the off-state condition.

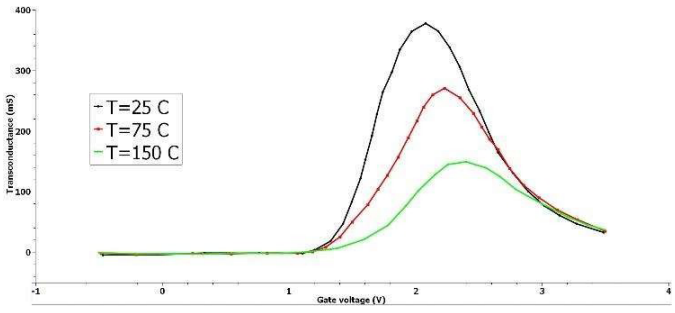

Fig. 9. Transconductance versus gate voltage for various ambient temperatures.

various electronic applications Figure 12 illustrates that the cut-off frequency of the p-GaN without AlGaN back-barrier and AlGaN with back barrier are 9.5 GHz and 10.1 GHz, respectively.

The Johnson Figure of Merit (JFOM) for p-GaN HEMTs without the AlGaN back-barrier is measured at 6.65×1012 V/s, while the value for p-GaN HEMTs with

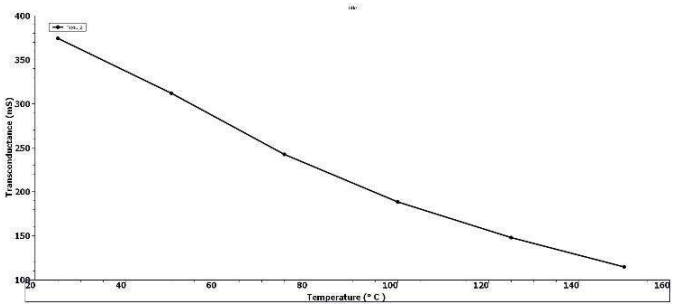

Fig. 10. Transconductance versus temperature at Vgs=2V.

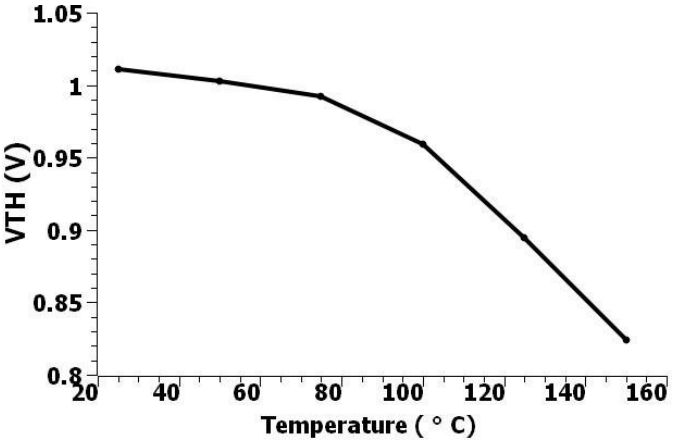

Fig. 11. Threshold voltage versus temperature at ID of 10^{-5} A.

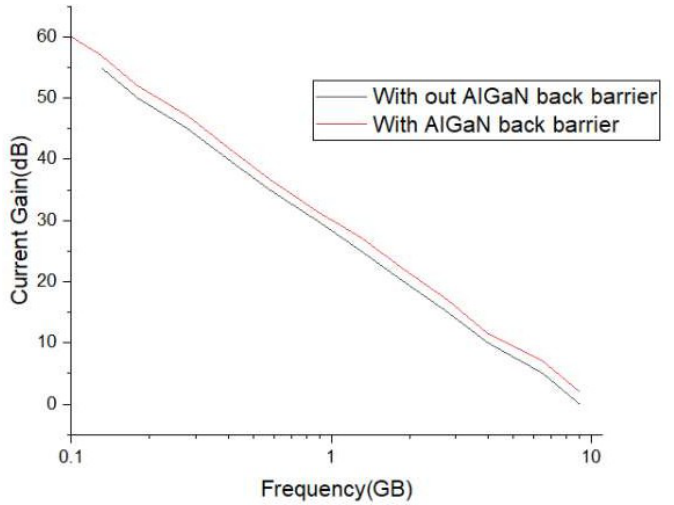

Fig. 12: Current gain of p-GaN without back-barrier and p-GaN with back-barrier.

the AlGaN back-barrier is 8.13×1012 V/s. This indicates a 22% improvement with JFOM for the HEMT device featuring the AlGaN back-barrier. The performance of the p-GaN device without the back-barrier has been evaluated in comparison to the proposed configuration, highlighting the benefits of incorporating the back-barrier in

Table 5: Comparison work with Transconductance, Threshold voltage, breakdown voltage, cutoff frequency and JFOM.

Parameter	p-GaN HEMT (without AlGaN back barrier)	Shenglei ZHAO *et al.*	Wang, Hongyue (2022)	Proposed Device with AlGaN back barrier
Transconductance	385 ms/120 ms	390 ms/130 ms	382 ms/132 ms	380 mS/120mS
Threshold voltage	1.12V/0.89V	1.2V/.9V	1.17V/0.9V	1V/0.83V
Breakdown Voltage (VBR)	700V	732V	796V	805V
Cut off Frequency (GHz)	9.5	-	-	10.1
JFOM (V s−1)	$6.65x10^{12}$	-	-	$8.13x10^{12}$

enhancing the device performance. Table 5 shows the comparison with research works present in literature with the proposed work in terms of transconductance, threshold, and BV. The analysis shows that is there is a major increase in BV and JFOM as compared to other works in literature. It was observed that the transconductance has a linear relationship with ambient temperature and decreases with an increase in temperature.

Conclusion

The influence of the AlGaN back-barrier and p-GaN gate on the performance of GaN HEMTs has been extensively evaluated through technology computer-aided design (TCAD) simulations. The results reveal several critical performance improvements, particularly in terms of the VTH, transconductance, BV, and JFOM. In terms of VTH, the device with the p-GaN gate and AlGaN back-barrier exhibits a VTH of 1V, primarily attributed to the depletion of channel electrons. This voltage is crucial for controlling the device's switching behavior and making it suitable for high-efficiency power applications. The transconductance of the device, a measure of its amplification capability, was found to decrease with rising ambient temperature. At 25°C, the transconductance value is 380 mS, but this decreases to 120 mS at 150°C. This temperature sensitivity highlights the importance of thermal management in high-power applications. Notably, the BV of the GaN HEMT with the AlGaN back-barrier shows a significant improvement of 105V compared to the device without the barrier. This enhancement makes the device more robust for high-voltage operations. Finally, the JFOM, a key performance indicator in high-frequency applications, showed a 22% increase with the p-GaN gate and back-barrier configuration, further emphasizing the potential of these devices in power electronics and other demanding applications.

Author Contributions

Arunraja A- Main concept Kishorekumar- Simulation Sangeetha D- result Supervisor Dharmaprakash R Implementation Bharathy K S – Implementation Balamanikandan A - Simulation

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Informed Consent Statement

Informed consent was obtained from all subjects involved in the study

Data Availability Statement

The data are not publicly available due to ethical and privacy restrictions.

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