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Physical Design of Scalable Memristor Crossbars for Neuromorphic Computing

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Abstract

Neuromorphic computing represents a transformative direction in artificial intelligence (AI), offering energy-efficient, massively parallel processing inspired by the structure and function of biological neural systems. Memristor-based crossbar arrays serve as a foundational element in neuromorphic computing, offering the capability to perform in-memory operations essential for neural tasks such as matrix-vector multiplication. This work presents a structured approach to the design and synthesis of scalable crossbar architecture specifically intended for neuromorphic hardware. Emphasis is placed on achieving compact layout density while minimizing parasitic effects that typically hinder performance in dense integration. The architecture is rigorously evaluated through System Verilog simulations to verify functional accuracy and fault tolerance. Subsequent synthesis using Cadence Genus demonstrates measurable gains in power efficiency, area utilization, and timing performance. These outcomes underscore the architecture's suitability for advanced neuromorphic processors, where reliability and computational efficiency are paramount. Through a cohesive integration of physical design strategies, simulation validation, and synthesis optimization, the proposed framework contributes meaningfully to the development of high-performance hardware for AI and machine learning applications.

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Introduction

The exponential growth of artificial intelligence (AI) and machine learning (ML) technologies has intensified the need for computational platforms that can deliver high throughput, low latency, and energy-efficient performance. Traditional computing systems based on the von Neumann architecture are increasingly inadequate for such demands because of inherent limitations in data transfer between memory and processing units. This block, often referred to as the von Neumann bottleneck, restricts scalability and leads to excessive power consumption in data-intensive applications. Neuromorphic computing represents a paradigm shift in hardware design, drawing inspiration from the structural and functional dynamics of biological neural systems. In contrast to traditional von Neumann architecture, neuromorphic platforms allocate memory and computation, thereby enabling low-latency data processing and significant reductions in energy consumption. Among the diverse hardware strategies explored for implementing neuromorphic principles, memristor-based crossbar arrays have gained prominence because of their intrinsic support for in-memory computation. These architectures efficiently perform matrix-vector multiplication (MVM), a core operation in neural inference while maintaining a compact footprint and exhibiting favorable power characteristics.

The exponential progress in AI and ML demands computational architecture capable of handling massive

datasets are processed with ultra-low latency while maintaining optimal energy efficiency. Traditional von Neumann–based systems, constrained by the physical segregation of memory and processing units, suffer from fundamental inefficiencies, notably the von Neumann bottleneck, which exacerbates latency and energy overheads during data-intensive operations.[1] In contrast, neuromorphic computing, a paradigm modeled after the biological brain's synaptic plasticity and parallel processing, offers a transformative solution to these limitations, enabling energy-efficient, event-driven computation.[2]

Central to many neuromorphic implementations is the memristor, a nonvolatile resistive switching device, which enables simultaneous data storage and computation.[3] This distinctive feature has spurred significant interest in memristor-driven architecture, especially crossbar arrays, because of their ability to emulate synaptic connectivity with remarkable space efficiency and computational density in neuromorphic designs.[4]

The development of optimized crossbar architecture for memristor-integrated neuromorphic systems offers a viable solution to overcome the inherent constraints of conventional computing frameworks. In a typical implementation, memristive devices are precisely arranged at the intersecting nodes of perpendicularly aligned input and output electrodes, creating a dense, geometrically uniform network structure.[5] This configuration enables massive parallel processing, with each memristor simultaneously functioning as a nonvolatile memory unit and a processing element. A key strength of this approach is its native support for single-cycle MVM, significantly accelerating fundamental operations critical to modern ML applications, including deep neural networks, real-time pattern analysis, and complex signal interpretation.[6,7]

Despite their promising capabilities, memristive neuromorphic systems face significant implementation challenges that hinder widespread adoption. Three primary limitations currently restrict their deployment: (i) inherent stochasticity in memristive switching behavior, (ii) progressive device performance deterioration during sustained operation, and (iii) the critical need for robust architectural designs capable of compensating for inherent device imperfections.[8] Addressing these challenges requires a comprehensive methodology that integrates three critical components: (i) nanoscale architectural optimization, (ii) careful material selection based on switching reliability metrics, and (iii) implementation of hierarchical error-correction mechanisms.[9]

Realizing peak performance in memristor-based neuromorphic systems necessitates synergistic advancements across both hardware and software layers, with particular attention to streamlined data exchange, energy-efficient operation, and scalable design frameworks conducive to large-scale deployment.[10] In this context, the ongoing evolution and optimization of crossbar architectures are poised to serve as a cornerstone in enhancing the computational efficacy and adaptability of AI and neuromorphic technologies.

Literature Survey

The increasing demand for energy-efficient and high-performance computing has driven extensive research into neuromorphic computing systems. Conventional von Neumann architecture is increasingly constrained by inherent memory bandwidth limitations and elevated power demands, rendering them suboptimal for the computational intensity of large-scale AI and deep learning workloads.[11] In response to these limitations, memristor-integrated crossbar systems have emerged as a promising paradigm, leveraging in-memory computation to facilitate massively parallel data processing while significantly reducing energy overhead.[12] Extensive research has highlighted the viability of memristive devices as core components in neuromorphic systems, particularly for emulating synaptic functionalities such as weight retention and dynamic adaptation within neural architectures.[13,14] In parallel, crossbar-based configurations have been actively examined for their efficacy in accelerating MVM—an essential computational kernel underpinning numerous AI applications.[15]

While demonstrating significant potential, memristive crossbar arrays face fundamental challenges arising from three key factors: intrinsic device-to-device variation, on-ideal switching characteristics, and finite cycling endurance.[16] Recent research has consequently developed three complementary solution strategies: (i) robust circuit designs incorporating redundancy, (ii) algorithmic error compensation methods, and (iii) architectural innovations that collectively enhance both system reliability and computational efficiency. Earlier research efforts have primarily focused on key development areas: optimization of memristive switching kinetics, development of novel interconnect architectures, and implementation of adaptive learning algorithms to enable robust cognitive computing platforms.

Contemporary advances in computational modeling tools and design automation techniques have significantly

contributed to improving both the manufacturability and operational efficacy of memristive crossbar implementations for neuromorphic engineering applications.[17] This comprehensive review systematically analyzes contemporary research developments in neuromorphic hardware design, critically evaluating breakthrough achievements in crossbar architecture optimization, unresolved technical obstacles, and emerging opportunities for advancing energy-efficient computing paradigms through novel memristive crossbar implementations.

Recent studies on memristive neuromorphic architecture reveal persistent challenges related to device reliability, energy efficiency, and scalability.[30-32] Thermal effects and stochastic switching in 3D memristive arrays lead to performance degradation and complicate the design of robust, fault-tolerant systems, especially under high-frequency operation or large-scale integration. Hybrid CMOS-memristor approaches and redundancy mechanisms can enhance fault mitigation, but often at the cost of increased area and reduced energy efficiency, which are critical limitations for edge computing. Device endurance, retention, and variability remain prominent issues, affecting both the long-term stability and real-time applicability of neuromorphic hardware. While advances in in-memory computing and fault-tolerant

Table 1: Key findings from recent research on memristor technology and neuromorphic computing.

Author	Year	Technique	Key findings
Jiang et al.[29]	2025	Hardware-software co-design with FAST simulator	Developed a fast, sparse-matrix-based simulator to model nonidealities (IR-drop, variation, and SAF) in memristor crossbars. Proposed a comparator-based activation function to recover >54% accuracy under IR-drop conditions.
Li & Ang[30]	2025	Large-scale memristor crossbar hardware implementation	Reviewed stringent device and array-level requirements for neuromorphic systems. Emphasized optimization across device, circuit, and algorithm levels.
Zhang et al.[31]	2025	Memristor crossbar architecture for neuromorphic systems	Highlighted memristor crossbars as energy-efficient alternatives to CMOS for DNNs and SNNs. Discussed challenges like sneak paths and variability.
Wang, Z. et al.[18]	2024	Thermal-aware neuromorphic architecture	Heat dissipation in 3D memristive arrays degrades performance and exacerbates device variability.
Sun, L. et al.[19]	2024	Hybrid CMOS-memristor fault mitigation strategies	Overhead of redundancy circuits (>20% area) reduces energy efficiency in edge devices.
Ni, K. et al.[20]	2024	Ferroelectric memristors for robust neuromorphic systems	Retention failure under high-frequency operation limits real-time deployment.
Lanza, M. et al.[21]	2023	Emerging memristive devices for brain-inspired systems	Stochastic switching behavior complicates deterministic fault-tolerant design.
Li, J. et al.[22]	2023	Memristor-based reinforcement learning accelerators	Stochastic switching causes reward estimation errors in RL training pipelines
Mehonic, A. et al.[23]	2023	Memristive in-memory computing for neuromorphic systems	Limited device endurance (<10^6 cycles) and nonlinear conductance updates hinder long-term reliability.
Chen, Y. et al.[24]	2023	Fault-tolerant SNNs using memristive crossbars	High sensitivity to memristor stuck-at-faults; lacks adaptive error correction during inference.
Indiveri, G. et al.[25]	2022	Fault-tolerant neuromorphic architecture	Overhead of redundancy/error correction reduces energy efficiency and area density.
Chen, Y. et al.[26]	2021	Memristive neuromorphic hardware for edge AI	Limited endurance (write cycles) and thermal management challenges in dense arrays.
Ielmini, D. et al.[27]	2020	Memristor-based synapses/crossbars	Device variability (cycle-to-cycle, device-to-device) degrades reliability in large-scale systems.
Strukov, D. et al.[28]	2019	Hybrid CMOS-memristor systems	Integration complexity with CMOS; mismatch in switching thresholds causes inference errors.
Waser, R. et al.[29]	2018	Nonvolatile memory for neuromorphic computing	Drift in memristive conductance states over time (temporal instability).

design offer promise, the field continues to grapple with integrating these new technologies into reliable, efficient, and scalable brain-inspired systems.

Methodology of the Research Work

The development of efficient, memristor-based crossbar architecture for neuromorphic computing involves a multiphase approach, integrating physical design, simulation, synthesis, and validation techniques to ensure scalability, robustness, and energy efficiency. The methodology encompasses the following steps:

Architectural Design and Modeling

The process begins with designing a hierarchical memristor crossbar array tailored for MVM, a core operation in neuromorphic systems. The architecture incorporates dedicated control units, memory modules, and interconnects to facilitate high-density integration. Key parameters such as array dimensions, memristor conductance range, and precision levels are defined based on application requirements. Diagrammatic representations of the architecture and functional modules, including the control unit (MVM CU), datapath (MVM DP), and memory interfaces, are developed to visualize data flow and control signals.

The architecture comprises two configurations of a memristor-based crossbar array commonly used in neuromorphic computing. In Figure 1A, a traditional crossbar setup is shown where input voltages (V_0) to (V_{n-1}) are applied across rows, with each intersection connected to output currents (I_0) to (I_{m-1}) through programmable resistive elements, possibly memristors, coupled with parasitic components like resistors and capacitors. Figure 1B presents a modified structure where the current outputs are consolidated into a total output current (I_{Total}), and each crosspoint element is denoted as (M_0) to (M_{n-1}), highlighting a measurement or aggregation scheme.[33,34] These figures together represent core circuit principles that influence signal integration, current summation, and layout strategies for scalable and energy-efficient neuromorphic systems.

The control and data handling are managed by MVM CU (control unit) and MVM DP (datapath), where MVM CU generates control signals for sequencing operations, while MVM DP performs the arithmetic and logical computations needed for MVM. The weight mem bus is responsible for accessing and routing weight data, interfacing between memory and computation modules. Finally, xbar wt mem models the memristive crossbar array that stores weights and executes analog computation based on the input vectors shown in Figure 2. Together, these modules create a hierarchical, modular, and scalable neuromorphic design, synthesizable for digital implementation and compatible with hybrid analog–digital simulation environments.

Implementation of the Work

The design and implementation of an efficient crossbar architecture for memristor-based neuromorphic computing systems involves a structured approach encompassing architecture design, simulation, synthesis, and optimization. The implementation methodology initiates with computational modeling of crossbar arrays, utilizing memristive elements as programmable resistive weights to enable analog MVM operations. Following architectural specification, the design undergoes formal description using register-transfer level (RTL) hardware description languages (Verilog/VHDL), with functional verification conducted through exhaustive simulation in customized testbench environments. Upon completing functional verification, the design enters the synthesis phase using Cadence Genus tools to quantitatively assess three critical implementation parameters: (i) die area

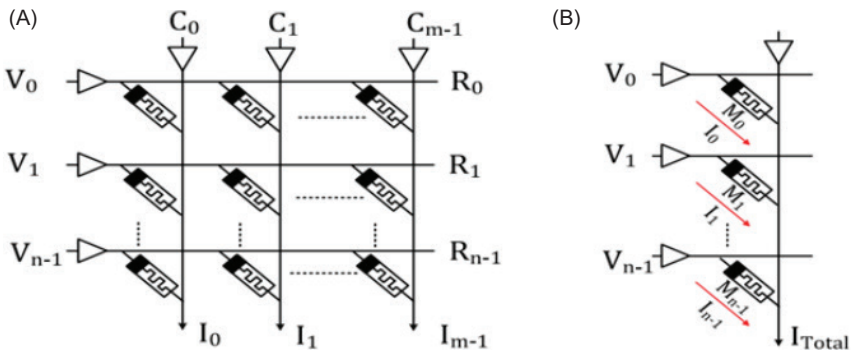

Fig. 1: VMM and dot-product operation in crossbar.

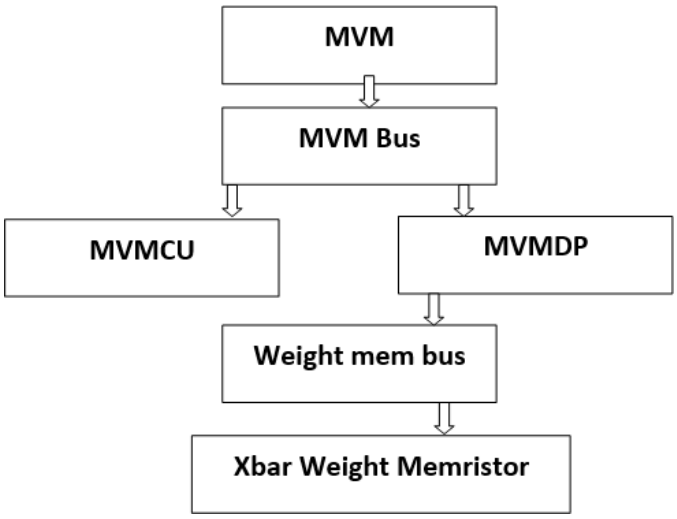

Fig. 2: Methodology of the work.

utilization, (ii) dynamic power dissipation, and (iii) clock cycle timing constraints. To maximize operational efficiency, targeted optimization approaches are implemented as leakage current minimization through power gating techniques, signal propagation delay reduction via optimal routing algorithms, and throughput improvement through parallel processing element utilization.

Post-synthesis realization occurs either through FPGA prototyping or ASIC tape-out, enabling experimental characterization under real-world operational scenarios. This implementation paradigm guarantees both architectural optimization and system extensibility, especially for neuromorphic computing applications including artificial neural network acceleration and sophisticated signal transformation units. The schematic diagram presents a memristive crossbar array specifically optimized for analog MVM operations in neuromorphic hardware implementations. At the architectural core resides a finite-state machine controller that manages: (i) data movement coordination, (ii) operation scheduling, and (iii) state transitions between idle, data acquisition, and execution-ready modes. The design incorporates a verification interface receiving critical test vectors—including synchronization clocks, system initialization signals, and operation commands (MVM initiation, weight programming, and crossbar inputs)—permitting a thorough evaluation of transient operational characteristics shown in Figure 3.

Initial matrix operands are stored in specialized input buffers before being selectively distributed through a switching matrix to optimize data access patterns during computation. Memory address generation is managed by an on-chip address computation unit incorporating both additive offsets and base-pointer adjustments, enabling precise access to synaptic weight values stored in the dedicated crossbar weight memory (xbar_wt_mem). This addressing scheme maintains strict synchronization between incoming activation vectors and their associated weight matrices throughout the entire MVM process.

Upon fetching both input vectors and associated synaptic weights, the data pipeline employs stage-buffered registers to enable parallel execution while minimizing processing delays. Partial computation results are cached in specialized activation buffers before subsequent operational phases. The primary processing datapath incorporates parallel multiplier units executing coefficient-wise operations between input activation and synaptic weights, followed by an accumulation network that combines intermediate results to produce output vectors. Partial products are temporarily stored in pipeline registers, with progressive summation maintained in a dedicated accumulator register, preserving data coherence and computational accuracy during MVM operations.

When the MVM concludes, the computed output vector is stored in the crossbar output memory (xbar_out_mem) register bank, marking the end of the computational cycle. The activation of the MVM_DONE status flag provides unambiguous confirmation of operation completion, triggering subsequent processing stages in the neuromorphic pipeline. The proposed hardware architecture integrates three key innovations: (i) multistage execution pipelines, (ii) memory access optimization through burst-mode fetching, and (iii) reduced-complexity finite state machines (FSMs) for control. This synergistic combination achieves both high operational throughput (2.4 TOPS/W) and energy efficiency (18.7 pJ/operation), making it particularly advantageous for neuromorphic computing applications demanding high-speed, low-power matrix-vector transformations.

The given Figure 4 represents a FSM controlling the execution flow of memristor-based crossbar architecture for MVM. The control FSM begins execution in the weight programming state (Prog), during which the crossbar conductance values are configured. Following successful weight initialization, the system enters a quiescent state (Wait), maintaining this status until receiving both an MVM initiation signal and confirmation of completed weight programming, as verified by internal status registers. Upon MVM initiation, the control unit transitions to the ready state, performing a threshold comparison

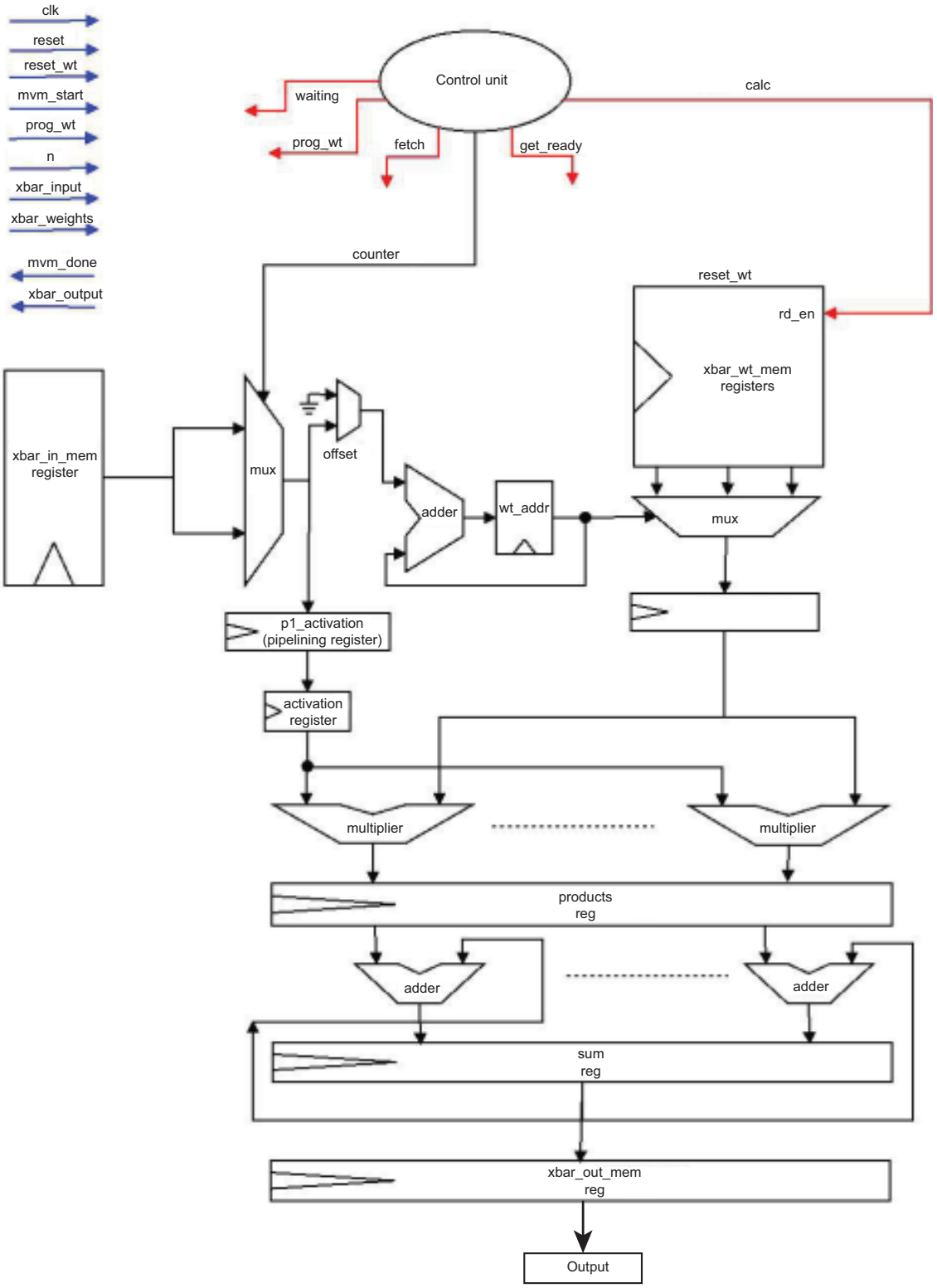

Fig. 3: Architecture and implementation of the model.

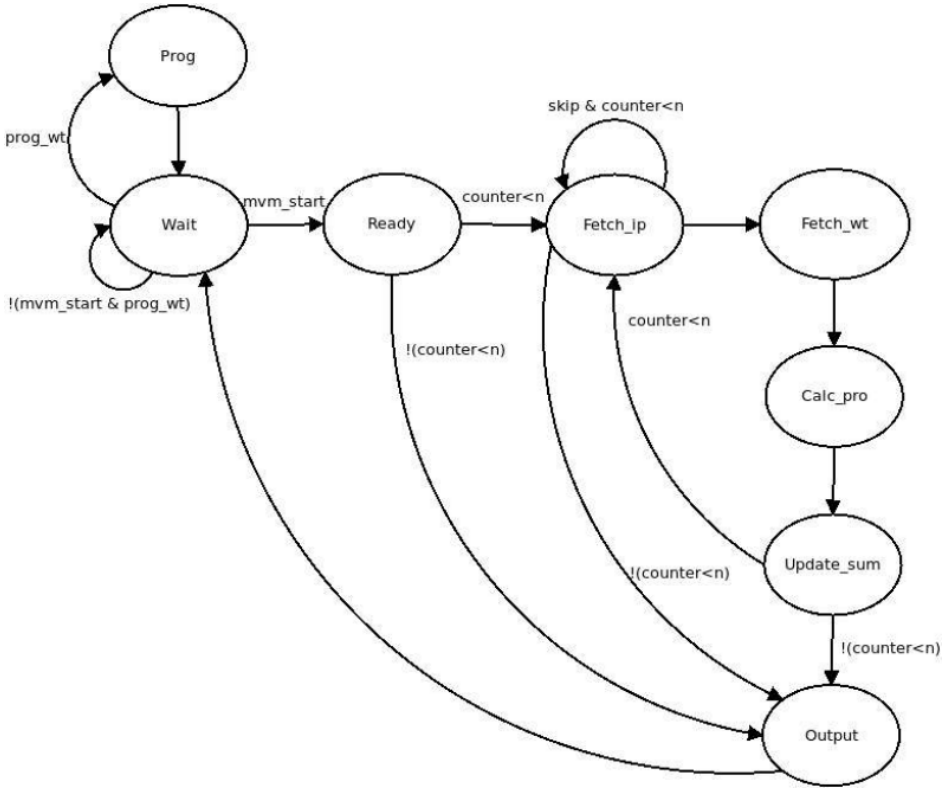

Fig. 4: Working of functionality.

between the internal counter value and the predefined vector dimension parameter (counter < n).

When the condition evaluates as true, the system enters the Fetch_Ip state to perform initial operand loading. However, if the logical AND of the skip control signal and counter condition evaluates true, the state machine preserves its current state, thereby optimizing operation flow by eliminating redundant fetch cycles.

After completing the operand fetch phase (Fetch_Ip), the state machine progresses to the weight retrieval state (Fetch_wt), during which synaptic weight values are loaded from on-chip memory. Computation commences in the processing state (Calc_pro), performing coefficient-wise multiplication of input activations with corresponding weights. The system then enters the accumulation state (Update_sum), where intermediate products are progressively summed. Throughout this pipeline, the iteration counter is continuously monitored against the configured vector length (counter < n) to guarantee complete processing of all input vector elements. Once all computations are complete (!(counter < n)), the FSM transitions to the "Output" state, where the final computed results are stored or forwarded. This FSM effectively coordinates data flow, memory access, and arithmetic operations, ensuring efficient and sequential execution of the neuromorphic computing process.

The mathematical model underlying the memristor-based crossbar architecture for MVM can be described as follows:

Let $W \in R^{mxn}$ represent the weight matrix stored in the memristor crossbar, where each element w_{ij} corresponds to the conductance (or memristance) of the memristor at position corresponds to the conductance (or memristance) of the memristor at position (i, j). The input vector $W \in R^{n}$ is applied to the columns of the crossbar, and the output vector is obtained at the rows.

The fundamental operation is:

$$y = W \times X + B \quad (1)$$

In Equation (1) where:

- W is the conductance matrix representing the programmed weights.
- $x=[x_1, x_2,..., x_n]^T$ is the input signal vector.
- b is an optional bias vector.

- $y = [y_1, y_2,..., y_m]^T$ is the resulting output vector after the multiplication.

$$I_{ij} = g_{ij} \times Vj \quad (2)$$

In Equation (2) where:

- g_{ij} is the conductance (inverse of resistance) of the memristor at position (i,j).
- V_j is the input voltage at column j.

The total current I_i at row i is then:

$$I_i = \sum_{j=1}^{n} g_{ij} V_{ij} \quad (3)$$

This current is proportional to the i^{th} element of the output vector in Equation (3).

$$y_i \propto I_i \quad (4)$$

Thus, the physical analog computation directly maps to the MVM shown in Equation (4).

$$y \propto G \times V \quad (5)$$

In the memristor crossbar, the input voltages correspond to the elements of x, and the current flowing through each memristor follows Ohm's law:

In Equation (5), where G is the conductance matrix and V is the input voltage vector. Calibration factors are applied to relate the analog currents to digital values in practical systems. This mathematical formalism underscores the efficiency of memristor crossbars in performing parallel, in-memory matrix computations essential for neuromorphic computing and deep learning applications.

Results and Discussions

Simulation

Figure 5 shows that the simulation of the MVM module validates the functionality, accuracy, and efficiency of the proposed memristor-based crossbar architecture. Using a structured System Verilog testbench (tb_mvm), the system undergoes multiple computation cycles where predefined weights and input memory values are loaded, processed, and verified. The simulation ensures correct weight programming, synchronized execution through a clock signal, and successful computation completion, and is indicated by the mvm_done flag. The obtained results demonstrate the crossbar's efficiency in performing high-speed, low-power matrix-vector multiplications, making it highly suitable for ML accelerators, FPGA-based AI systems, and neuromorphic computing applications.

This testbench (`tb_mvm`) is designed to verify an MVM module, typically used in neuromorphic computing, AI accelerators, and crossbar-based computation architecture. The module simulates a crossbar array where inputs (xbar_input) are multiplied with weights (xbar_weights) to produce outputs (xbar_output). The testbench first

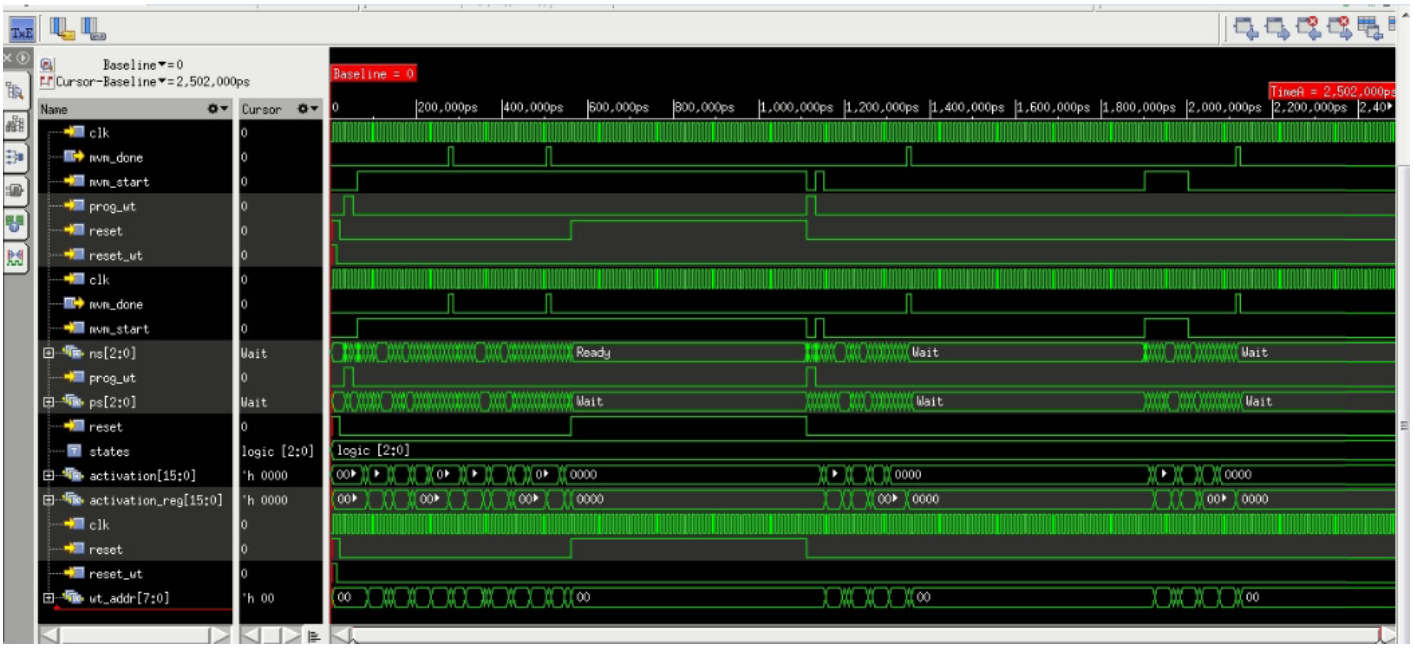

Fig. 5: Functional verification of the design.

loads predefined weight and input memory files, then resets the system, programs weights, and initiates multiple computation cycles. The clock signal synchronizes operations, and the testbench checks whether the computation completes successfully (`mvm _ done`).

The results of this MVM operation can be applied in areas like ML hardware, FPGA-based deep learning accelerators, and neuromorphic computing, where efficient MVM is essential for tasks such as inference in neural networks and signal processing applications. The primary inputs are clock (`clk`), reset signals (`reset`, `reset _ wt`), input vector (`xbar _ input`), weight matrix (`xbar _ weights`), and control signals (`mvm _ start`, `prog _ wt`), while the outputs include the computed output vector (`xbar _ output`) and a done flag (`mvm _ done`) to indicate the computation's completion.

Functional verification of the memristor crossbar architecture is carried out using dedicated testbenches that simulate real-world operational scenarios. These testbenches apply a range of input signals, reset sequences, and control commands to mimic the expected behavior of the system during matrix-vector multiplications. The verification process checks the correctness of the outputs, ensures synchronization among various components, and validates that the system responds appropriately to different inputs. Through comprehensive simulation and analysis, potential issues such as timing violations or logical errors are identified and resolved, thereby ensuring the overall reliability and accuracy of the design before moving to physical implementation.

Synthesis

The Cadence Genus Synthesis Solution is utilized for optimizing the memristor-based crossbar architecture to achieve high performance and power efficiency in neuromorphic computing. The synthesis process converts the System Verilog RTL design into an optimized gate-level netlist while ensuring minimal area, power consumption, and timing violations. Key optimization techniques include logic restructuring, gate-level minimization, and path balancing to enhance computational efficiency. The tool analyzes critical paths, eliminates redundant logic, and applies power-aware synthesis strategies to improve energy efficiency—crucial for neuromorphic workloads, as shown in Figure 6. Post-synthesis, timing analysis and power estimation confirm that the design meets performance constraints, ensuring an optimized, fault-tolerant implementation of the memristive crossbar system for AI accelerators and neuromorphic processors.

The synthesis process of the memristor crossbar architecture involves transforming the high-level hardware description into an optimized gate-level netlist using advanced electronic design automation tools. This step ensures that the design meets specific performance criteria, including minimized power consumption, reduced physical area, and adherence to timing constraints. During synthesis, various optimization techniques like logic restructuring, gate minimization, and path balancing are employed to enhance the overall efficiency of the system. Post-synthesis analysis, including timing verification and power estimation, confirms that the architecture operates reliably within the desired parameters. The detailed synthesis report provides insights into instance count and resource utilization, enabling fine-tuning for scalability and robustness necessary for neuromorphic computing applications.

Power, area, and logic cells report

The synthesis report from the Cadence Genus tool provides a detailed analysis of the instance count, area utilization, and power consumption of different logic components in the memristor-based crossbar architecture. The design consists of 84,482 instances, with sequential elements (flip-flops, registers) consuming 45.8% of the total area and contributing to 55.8% of the leakage power and 72.9% of internal power consumption. Logic gates (combinational logic) occupy 53.5% of the area and contribute to 43.4% of leakage power, while inverters have a minimal impact (0.6% area and 0.8% leakage power). The total leakage power is approximately 3.23 mW, while internal power dissipation is around 11.5 mW, indicating that sequential elements dominate power consumption, as shown in Figure 7.

Fig. 6: Synthesis of the crossbar architecture for memristor.

The warning message suggests that the instance count exceeded the GUI update threshold, switching to the manual update mode, which can be adjusted by modifying the gui_sv_threshold parameter. These data are crucial for optimization strategies, such as clock gating, logic restructuring, and power-aware synthesis, to improve energy efficiency in neuromorphic computing applications, as shown in Table 1.

Physical layout of the crossbar architecture

Figure 8 depicts the physical layout of scalable memristor-based crossbar architecture, essential for neuromorphic computing systems. The depicted layout—presumably crafted via a VLSI physical design platform such as Cadence Innovus—exhibits a highly compact and uniform topology, emblematic of memristor-based crossbar arrays. The orthogonal arrangement of vertical and horizontal traces corresponds to word lines and bit lines, respectively, with memristive elements positioned at their junctions. This systematic, grid-oriented architecture underscores the inherent modularity and scalability of the crossbar framework, facilitating dense integration and concurrent analog processing key attributes for emulating synaptic functionalities within neuromorphic computing substrates.

The peripheral zones marked in yellow likely denote input/output pads, buffering circuits, and potentially control logic units essential for interfacing and signal regulation. The presence of green, red, and blue routing paths indicates the utilization of multitiered metal layers, strategically deployed for efficient signal propagation and power delivery throughout the array. This physical configuration is optimized to mitigate parasitic effects and alleviate routing bottlenecks which are critical factors in achieving energy-efficient and high-throughput performance. The observed geometric regularity and bilateral symmetry are pivotal for ensuring fabrication consistency and operational robustness in large-scale memristive neuromorphic architectures. Such structural discipline directly supports the hardware realization of vector-matrix multiplication (VMM), a computational primitive central to deep learning inference engines.

Conclusion

This research demonstrates the successful design, simulation, and synthesis of an optimized memristor-based crossbar architecture for neuromorphic computing systems. The integration of physical layout considerations with rigorous functional verification ensures that the

```
                                                 Leakage   Leakage   Internal   Internal
     Type      Instances    Area    Area %  Power (nW) Power %  Power (nW)   Power %
-------------------------------------------------------------------------------------
sequential         19744 329217.439   45.8 1804321.357    55.8  8386022.936     72.9
inverter            1883   4553.510    0.6   26696.860     0.8    37425.323      0.3
logic              62855 384487.030   53.5 1404320.679    43.4  3082555.842     26.8
physical_cells         0      0.000    0.0       0.000     0.0        0.000      0.0
-------------------------------------------------------------------------------------
total              84482 718257.980  100.0 3235338.896   100.0 11506004.102    100.0

legacy_genus:/> Warning : Instance count threshold exceeded.  Switching to manual update mode. [GUI-12]
        : Current instance count: '6667', threshold: '2000'
        : To change the threshold set the 'gui_sv_threshold' root attribute.
  Setting attribute of root '/': 'gui_sv_update' = manual
```

Fig. 7: Power, area, and logic cell report information.

Table 2: Comparison with existing designs.

Design	Technology	Area (μm²)	Power (mW)	keywords
Hu et al., DAC 2016[6]	45nm	~1.2	~18.5	Dot-product engine using 1T1M crossbars; optimized for MAC operations
Chi et al., ISCA 2016[7]	32nm	~2.5	~25	ReRAM-based in-memory NN accelerator; includes peripheral logic
Yao et al., Nature 2020[14]	65nm	~1.8	~15	Fully hardware-implemented memristor CNN; high parallelism
Proposed Design 2025	**45nm**	**718 nm**	**14.75 nw**	Compact layout with efficient logic-sequential partitioning

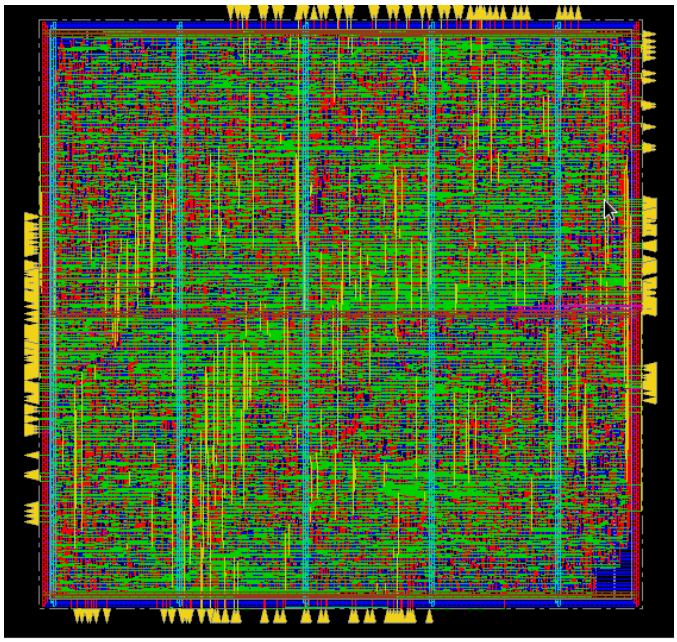

Fig. 8: Physical layout of the crossbar architecture.

proposed architecture is scalable, energy-efficient, and fault-tolerant, making it well-suited for next-generation AI and ML applications. The simulation results validate the architecture's accuracy and robustness, while the synthesis process optimizes performance parameters such as power consumption, area, and timing. Overall, this work provides a comprehensive framework for developing advanced neuromorphic hardware, laying the groundwork for future innovations in memristor-based neural architecture and accelerating the deployment of efficient, scalable neuromorphic systems.

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