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Energy Efficient and Radiation Hardening Dual Interlocked SRAM Cell Design Using Alternate Technology

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Abstract

Sources of radiation are packaging and the environment. Heavy ions, alpha, and protons constitute the radiation sources. Alpha particles are mainly involved due to the packaging materials of the circuits in the chip, while protons are involved due to the dopants used in semiconductors, caused by indirect ionization. The particles interact with electrons, leading to the charge deposition. The charge collection alters the functioning of the circuit nodes. Reliability of memories is affected by the particle radiation, which is responsible for Single Event Upsets (SEUs). The CMOS technology is prone to SEUs when fabricated for SRAM chips, which store information. The other problem is single-event multiple-node upsets, for which the circuit to be designed should have radiation-hardening features. In this work, different configurations based on negative feedback restoration of logic-based SRAM design, multinode structure with radiation suppression, storage node with pull-up NMOS transistor, multinode upset elimination circuit, and radiation-hardened circuits were designed and implemented. A dual interlocked storage cell SRAM is proposed, which has higher radiation tolerance. The percentage of error occurrence is less compared to the conventional circuit. The configuration provides better driving capability for an increased word line. The circuits were implemented in CMOS, FinFET, and CNTFET devices. Silicon on Insulation (SOI) substrates will reduce this effect, and FinFET devices will eliminate further problems in CMOS. But the results show that the carbon nanotubes perform better in power and delay when compared to FinFET and CMOS. The implementation was done in Synopsis with predictive technology models of the Stanford University and TSMC in 32 nm technology.

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Introduction

The rapid evolution of technology necessitates fast data processing capabilities. The high demand for IoT-based systems in the healthcare sector and multimedia has enabled the integration of human life functions with computing devices, and memory plays a very important role [1]. Rapid performance has driven the SRAM designs using advancements in in-memory technologies, which are essential for the requirements of various applications. SRAM is important for many applications, including embedded systems, biomedical applications, and IoT devices. [2]. The repeated usage of biomedical devices over time requires the reduction of SRAM variability during write operations. Low-voltage SRAMs are power-efficient and function for a longer duration using small batteries. However, low power supply SRAM in CMOS technology result in increased access times, degradation of stability, and worsening of write

variability [3,4]. Reduced supply voltage and technology node scaling impact Si-CMOS SRAM performance, causing short-channel effects and increased leakage. The objective of the memory device is to reduce power dissipation to improve battery life. This can be achieved by reducing the power consumption of the device. CMOS-based devices can be deployed in difficult terrains with low power supply, but minimal compromise is expected in access time and silicon space. In CMOS-based devices, instability in temperature due to node reduction, short channel effects (SCEs), and tunneling effects are high. FinFET technology must be used for designing SRAMs; this can be an effective approach for these issues [5]. In contrast to CMOS technology, the FinFET device eliminated the leakage current through its enhanced 3D gate structure. The 3D alignment helps in better control of the gate terminal, which enhances the working of the circuit at low voltage. The scaling process of devices does not affect their performance with voltage. The 3D gate configuration of FinFET devices provides enhanced channel control [6,7]. The errors due to charged particles in the memory are a problem if the values stored were altered. The voltage scaling may impact the error susceptibility. The soft errors in SRAM can be eliminated by considering the design structure and electrical parameters [8,9]. The increasing need for fast data processing requires the integration of memory within the processor in AI and IoT-capable edge devices, especially for machine learning to enable compute-in-memory (CIM) for the implementation of algorithms, which is effective in both energy use and performance [10,36]. During data processing, hierarchy is determined by two crucial parameters, namely data retention and access time. Machine learning is a computationally intensive approach for analyzing large datasets to identify trends and behavioral patterns. It involves feature extraction and classification. The datasets can be used to study the features and weight sets and can be further improved by optimizing the SRAM bit cell circuit to reduce the overall power consumption in memory systems [11,12]. The development in technology and computation units gave rise to SRAM with different classifications such as FRAM, RRAM, MRAM, PCM-RAM, and FLASH to improve retention time, density, and performance.

Key Contributions

A new device approach in the design of SRAM, which has radiation immunity.

The SRAM with a higher radiation tolerance with a lower percentage of error occurrence compared to the conventional circuit.

The configuration provides better driving capability for an increased word line.

Investigation of the CMOS, FinFET, and CNTFET SRAM devices.

Low Power Techniques For SRAM

The power can be minimized by reducing the operation. Nevertheless, performance and system requirements often limit operating voltage, necessitating the use of other techniques in SRAM. The Half Swing Pulse-Mode technique can be used to develop low-power SRAM without affecting performance by using a reduced input signal swing gate family. Memory bank partitioning is a method that enhances speed by dividing a memory array into smaller banks, enabling only the addressed bank to be activated. This method also enhances SRAM power efficiency by switching word line capacitance and reducing the number of bit cells activated. Additionally, hierarchical partitioning can be employed for smaller memory banks. The Quiet-Bitline Architecture aims to maintain low voltage on bit lines, and eliminating charging and discharging power are the main advantages. It uses two methods for write and read operations. In the write operation, excessive bit line swing elimination is used by the side-driving approach. In this technique, a “0” signal is applied to the cell by making one side floating, which allows data access on the other side, while the opposite side remains floating. In contrast, a pulling approach is employed during a read operation.

In a standard SRAM design, the bit lines typically swing from one voltage rail to the other during a read operation. For the conservation of power, it is necessary to limit the voltage swing on the bit lines. This can be accomplished by disconnecting the memory cells from the bit lines after differential sensing has been completed. This method prevents memory cells from altering bit line voltage and may require the isolation of bit line sense amplifiers from bit lines after sensing. This helps reduce voltage swings in bit line capacitance and saves power, and requires pulsed signals at word lines and sense amplifiers. Advancements in electronic design resulted in the development of portable and battery-operated devices, which have raised a primary concern about power consumption and speed of operation. High-performance handheld devices have power constraints due to the battery failing to meet chip demands. Technological advancements in data transmission are the reason for the increased functions of chips, with VLSI technology incorporating more circuits and systems

in a single chip. Despite MOSFET devices dominating integrated circuits, significant challenges and problems remain. The primary challenge is power consumption due to leakage current during device switching between digital logic values, which is the sudden drop in channel resistance due to sudden current flow.

SRAM Cell Design

The advancement in the implementation of edge devices enabled the integration of memory and computational units in edge devices. The Internet of Things (IoT) and machine learning (ML) units need integrated memory placed near the processing unit. The execution of compute-in-memory (CIM) for algorithm implementation is efficient in both energy and performance. During data processing, memory stores data either temporarily or permanently. The memory hierarchy is determined by two key parameters, data retention and access time. Machine learning is a computationally intensive approach for analyzing large datasets to identify trends and behavioral patterns. It involves feature extraction and classification. The datasets can be used to study the features and weight sets, and they can be further improved by optimizing the SRAM bit cell circuit to reduce the overall power consumption in memory systems.

Low Power Techniques for Sram

Reducing operating voltage is an effective method for lowering dynamic power dissipation in low-power applications. Nevertheless, performance and system requirements often limit operating voltage, necessitating the use of other techniques in SRAM.

Radiation problem

The main idea is to design and implement advanced SRAM architectures and techniques to prevent radiation-induced errors and maintain data integrity. In the process of enhancing the overall resilience of SRAM memory cells, innovative circuit designs, error correction mechanisms, and radiation-hardened materials are used [13,14]. Aerospace-based devices have SRAM cells with integrated circuits, which eliminates or frees them from radiation problems. Hardened cells achieve radiation tolerance but also sacrifice area, increasing power consumption [15]. Since scaling in nanometers reduces the size or space between devices, radiation problems are high. Multimode upsets are to be investigated in scaled devices to eliminate errors and power consumption [16]. Internal radiation in a chip, particularly in SRAM, is prone to single-event upsets (SEUs), leading to data corruption. Change in logic happens in the cell even though there is no physical damage to the circuit, and several methods are employed to prevent the impact [17].

Radiation particles can cause soft errors in conventional SRAM cells, causing them to reset stored logic values when an energetic particle strikes, potentially leading to failure [18,19]. In radiation-rich environments, charged particles can cause short voltage or current rap, also known as a single-event transient (SET). In the memory element, data changes at one node can cause data changes at another due to a memory element feedback mechanism. However, this error can be easily rectified through proper write operation. Technology scaling reduces supply voltage and circuit internal node capacitance. Error-correcting codes were used for these problems [20,21]. The SRAM used in terrestrial applications needs radiation-hardening structure and functions [22,38]. The stability and multiple failure elimination are the main factors for data confirmation [23,35]. FinFET-based circuits provide low leakage and low power operation [25–27]. The offset noise in analog circuits can also be eliminated using FinFET devices. In ML applications, there is a mixture of analog and digital circuits; the FinFET provides low power and low leakage [2–29]. The RHBD-14 SRAM memory cell is built to resist faults such as SEU and DNU that occur when struck by high-energy particles [28,30]. It uses extra support nodes that are connected to the main storage nodes, which help to recover the lost data and keep the system stable. This setup improves both read stability and write performance even under harsh conditions. Additionally, the proposed cell shows a clear advantage in write operations. The S8P9N SRAM cell was designed for energy-efficient, soft-error-tolerant, and provides better read stability with reduced write error rate [31]. It shows strong radiation tolerance, is fully protected against SEU at sensitive points, and is partly resistant to DNUs and TNUs. With the use of two sensitive nodes, the design operates at the low dynamic power of 1.25 W. This requires less energy for both read and write operations, which ensures the overall energy efficiency. The EWS-16T SRAM cell was created to avoid soft errors that are caused by radiation, such as SEUs and SEMNUs in space [37]. It uses the PMOS-NMOS for a special design, which allows quick and simultaneous control of the storage nodes and internal nodes. It makes the cell more reliable and faster in operation. The work of Li et al. introduces a 14T RHBD SRAM cell built with 65 nm CMOS technology, which is aimed at aerospace applications [33]. This design improves protection against soft errors in spacecraft and satellites.

It provides better stability and fewer errors by applying special circuits and layout methods. This controls the charge-sharing by boosting the critical charge. In both monolithic and chiplet ICs, designers must account for components from different process nodes [34]. There are some varying conditions, like temperature and supply voltage, which affect the single-event (SE) behavior and overall system reliability. This work studies a commercial bulk FinFET circuit with varying threshold voltage at nodes using standard D-FF designs.

Background Methodology

Previous Hardened Memory Cells

Figure 1A shows the standard cross-coupled inverter 6T SRAM. The stored values in one node trigger the other due to the feedback structure. The cell state is altered based on the triggering of the storage node. Thus, challenge arises in optimizing the design against the soft errors. This conventional unit suffers more when there are higher radiation problems, especially in space applications. Internal radiation problems also initiate the node triggering, thereby altering the state without any limit. The problem can be addressed using the other structures presented.

The negative feedback-based SRAM design is shown in Figure 1B. The Quatro-10T has four storage nodes. The feedback restores the correct value if any of the nodes is affected by the radiation. But the circuit has poor write ability and is difficult to recover from "0"-storing if affected by radiation. In Figure 1c, two transistors were added to manage the writing problem in the previous circuit. The 12T also stores the values in four nodes and is effective in suppressing the state change. The circuit faces stability issues and high-power consumption. The storage node with pull-up NMOS transistor is shown in Figure 1d. The radiation immunity is high for this circuit and can recover if any radiation-based data change has

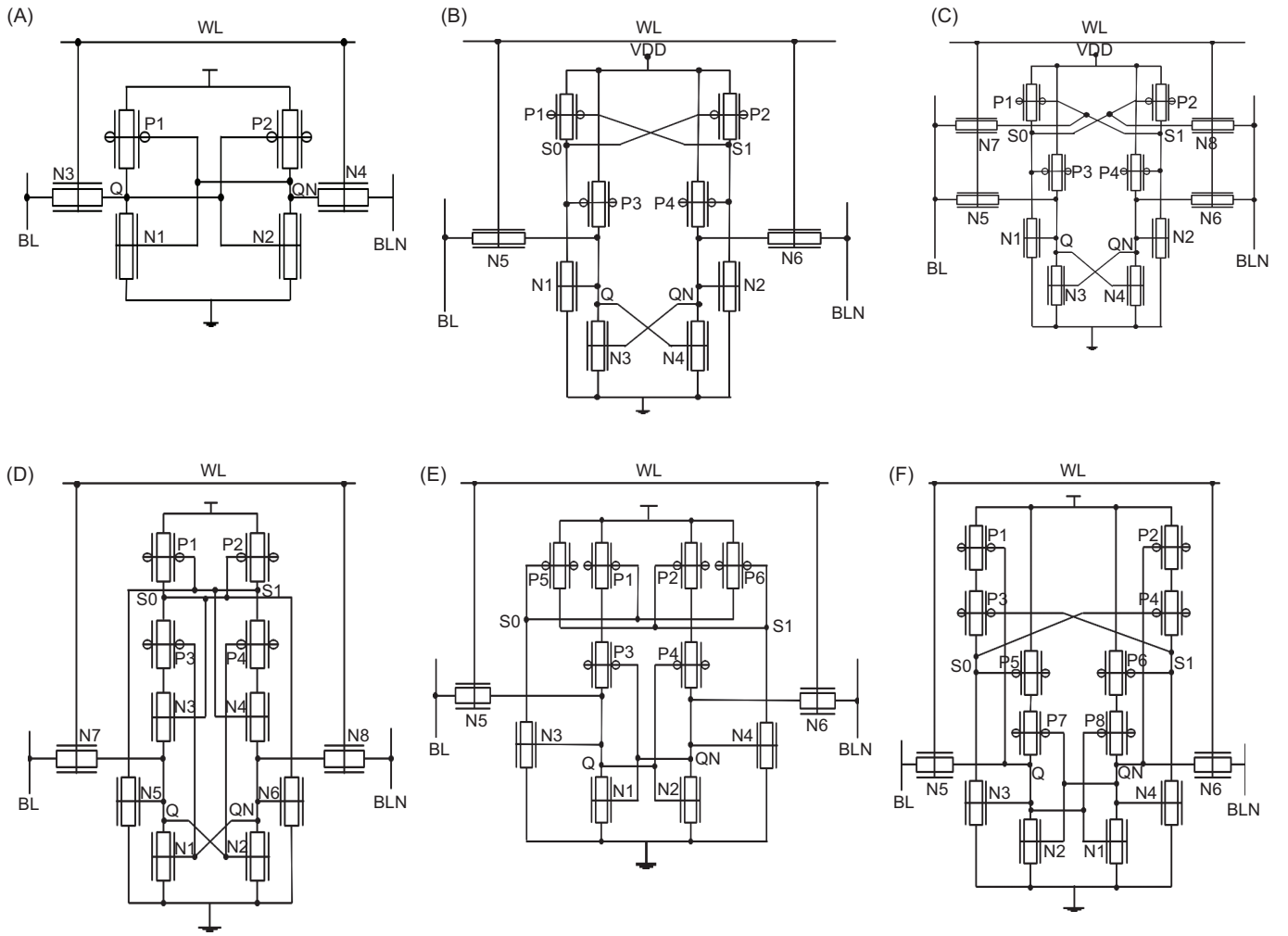

Fig. 1: FinFET-based radiation-hardening SRAM structure: (A) 6T SRAM; (B) Quattro-10T; (C) WE-Quattro-12T; (D) RHM-12T; (E) RHD-12T; (F) RSP-14T

occurred. The main problem of the circuit is the limitation in supply voltage scaling due to stacking issues. The circuit is shown in Figure 1.e can handle multinode upset. The power consumption is higher and is not capable of detecting stuck faults at the "0" storage node. The radiation tolerance improves using additional transistors in the circuit in Figure 1f. The circuit is faster in the data writing operation, but the power consumption is larger. These were the disadvantages and problems faced in the existing circuits implemented in MOS transistors.

A major obstacle for CNTFETs is producing only semiconducting nanotubes to achieve the chiral selectivity. Issues such as proper alignment and consistent fabrication also prevailed. This reduced scalability and integration with CMOS technology. Direct CVD growth on silicon offers a promising path for large-scale production and better quality management. CNT design shows potential for high performance with low power usage. These practical hurdles can still limit their wider application.

Manufacturability Challenges

Carbon nanotubes act as metals or semiconductors depending on their chirality, but controlling this property during growth is difficult. For circuit applications, only semiconductor nanotubes are useful, and separating them from metallic ones is a major problem. Another major problem is accurately aligning and positioning CNTs on a substrate for large-scale production. Even with direct growth on silicon through chemical vapor deposition (CVD), later processing steps may introduce defects that may affect the performance. These challenges in alignment, placement, and contact reliability make it hard to use CNTFETs in complex, high-density circuits on standard wafers.

Radiation-hardened SRAM (RH-SRAM) is built using design methods such as redundant nodes and feedback circuits that help prevent memory from soft errors caused by high-energy radiation. Such protection is essential in aerospace and is important in edge computing and IOT. For this, both reliable performance and secure data are required. Radiation-hardened-by-design (RHBD) focuses on improving SRAM strength through circuit and layout techniques. This can reduce the need for expensive process-level modifications.

Radiation-Hardening-by-Design

Cache Memory

RHBD SRAM protects the cache memory data from errors, which ensures the performance and reliability of systems. While operating in radiation-affected conditions and applications, safety is highly important.

Edge Computing and IOT

When devices process information at the source, they may run in an open environment where radiation can occur. RHBD SRAM ensures dependable performance so that the edge nodes work effectively.

Aerospace

Radiation hardening is most important in space missions, where satellites and spacecraft are exposed to intense radiation. To make sure they stay reliable over long periods, engineers use certain design methods and processes to make these parts resistant to radiation.

Proposed Radiation Hardened Sram Design

Reliability of memories is affected by particle radiations, which are responsible for Single Event Upsets (SEUs). The CMOS technology is prone to SEUs when fabricated for SRAM chips, which store information. The other problem is single-event multiple-node upsets. The circuit to be designed should have radiation-hardening features. Radiation affects the information stored in the SRAM cell, especially designed for space applications. Since modern VLSI circuits use smaller devices and a power supply, the device is highly prone to radiation effects; because of this, the critical data stored in SRAM is affected. If the data stored is less than the radiation potential, there will be information loss. The flipping of this data, SEUs, is eliminated. Due to the smaller size of devices in the circuit, the flipping of one node will affect the other, which will lead to complete data corruption or loss. This is referred to as Single Event Multiple Node Upsets (SEMNUs). The charge sharing in CMOS causes adjacent node variation, which leads to SEMNUs. By this, the multiple sensitive nodes will be affected. Error correction codes and other methods solve this problem of node flipping and multiple node variations. However, this method suffers from area overload. The power consumption is high for an error correction code, a node suitable for low-voltage applications.

Solutions

Silicon on Insulation (SOI) substrates will reduce this effect, and FinFET devices will eliminate further problems.

APPROACH 1

Requirement of an additional circuit for radiation hardening.

APPROACH 2
Negative feedbacks were used to protect from radiation hardening.

Sources of Radiation and its Effects

Sources of radiation are packaging and the environment. Heavy ions, alpha, and protons constitute the radiation sources. In this problem, alpha particles are mainly involved due to the packaging materials of the circuits in the chip, while protons are involved due to dopants used in semiconductors, caused by indirect ionization. The particles interact with electrons, leading to charge deposition. The charge collection alters the functioning of the circuit nodes. The charge transportation has a higher impact when the field is present, and the movements will be higher. The carrier concentration gradient, reverse biasing, and off-states affect the flipping process of the sensitive nodes. Radiation-induced current transient occurs due to the diffusion process, which causes the event. The particle switching the PMOS and NMOS during the switching state causes the upset, but flipping happens in the SRAM cell if these changes create voltage across the threshold voltage and make a bit-flip in the node. This problem is more prevalent in SRAM since it is in the hold state most of the time. The 6T SRAM cell is affected more by the radiation. This is overcome by the same or dual interlocked storage cell (DICE), which uses double the transistor count compared to a 6T SRAM cell. The circuit is shown in Figure 2. The four nodes at the connection point are the storage nodes. Even if there is a failed attempt, the value can be restored. The restoration of data is possible by interlocking configuration through unaffected nodes. This configuration is most tolerant of SEU. They are capable of multiple-node upset tolerance. Simultaneously, node flipping will affect the overall output, but the percentage of error occurrence is less compared to the conventional circuit. The configuration provides better driving capability for an increased word line.

Negative Feedback Configuration

This approach is tolerant to single-event upset but suffers from delay and power consumption.

Radiation Hardened By Design Sram

The design uses the delay phenomenon through the time elapsed of signal transition, which enables the flipping node to recover the cross-coupled inverter used to provide the delay for the signal, so the flipped node recovers from particle strike. Unaffected nodes through negative feedback recover the flipped node.

Active regions in the SRAM cells are isolated by using the FinFET devices. The leakage was also eliminated. The inverter connections provide the feedback and drive the regenerative process. The delay elements introduce an additional node, the slow degenerative process, and negative feedback eliminates the node upset. The circuit simulation was done using HSPICE Synopsys. Predictive technology models were used to develop the circuits for CMOS and FinFET. The delay and power consumption were evaluated. The SRAM cell was tolerant to radiation, consumes low power, and has optimized area over leads.

Results and Discussion

The hardness against radiation is achieved by the developed circuit. The FinFET and CNTFET SRAM circuits were designed and implemented in a 32 nm technology circuit configuration using a netlist by the predictive technology models. Below 32 nm, the circuits suffer from stability issues and high-power consumption at high switching frequencies above 3GHz. For the execution, the input was set as a bit stream for a frequency of 1 GHz. For the rest of the analysis, write and read bit values are given. The physical and electrical parameters of the FinFET and CNTFET devices are used according to the standard of the device. Tables 1–3 show the SRAM performance of various configurations using CMOS, CNTFET, and FinFET. The parameters taken into consideration were power current and delay. The power current and delay were measured for write and read together. From the analysis, it has been observed that there was mixed performance among the different configurations. The current driving capacity stabilizes the output logic, so it is important to consider the current. A nominal value is suitable for the same, but to make sure it is above the logic level of "1." The radiation hardening configuration, power, energy, and delay also differ. The overall investigation showed that certain configurations were suitable for applications where power was the dominant requirement, while in a few cases, speed mattered. Most devices today are battery-operated, and energy is an important parameter to be considered.

In Tables 1–3, we observe that the quattro-10T shows low power consumption for CNTFET. Except for RSP-14T, all circuits exhibited low power consumption for the CNTFET device. The RSP-14T showed an improved performance in CMOS compared to other devices. Additional experiments were carried out to verify the same with 2 GHz and 800 MHz, but the same performance was observed in the RSP-14T configuration. The lowest power consumed by RHM13-T in CNTFET when

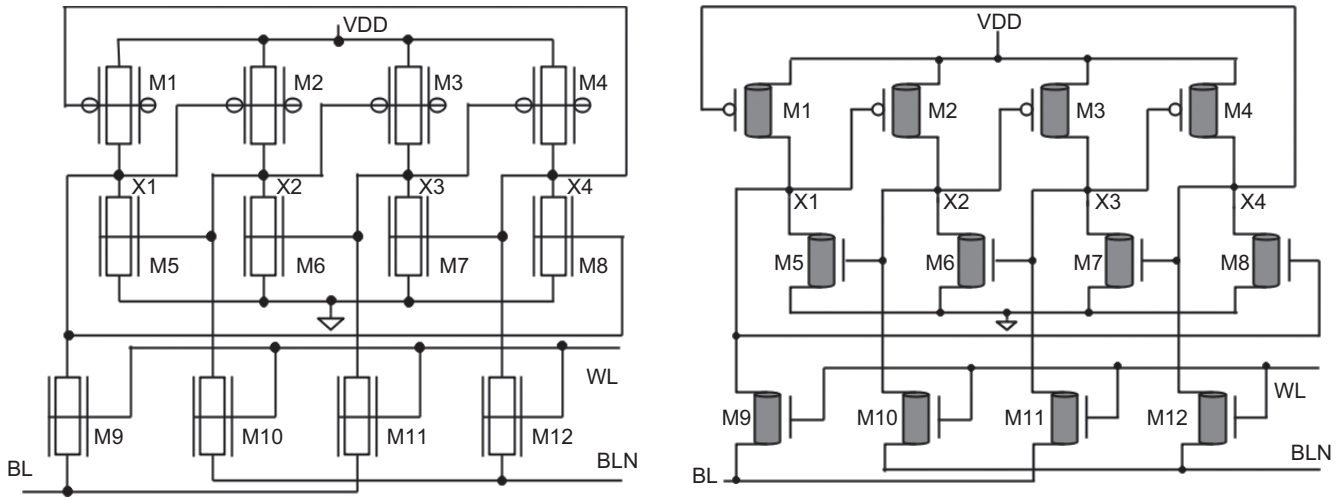

Fig. 2: Proposed FinFET and CNTFET dual interlocked storage cell (DICE)

Table 1: CMOS performance analysis for different configuration Vdd = 1V

	CIRCUIT NAME-CMOS	Current (A)	Power (W)	Energy (J)	Delay (S)
I	QUATTRO-10T	90.99u	54.65u	264.17f	1.99p
II	WE-QUATTRO-12T	122.4u	100.12u	494.19f	55.60p
III	RHD-12T	19.33u	11.75u	45.35f	6.03p
IV	RHM-13T	14.20u	4.71u	23.57f	343.44f
V	RSP-14T	35.85u	7.93u	39.24f	324.65f
VI	DICE	149.84u	96.93u	501.6f	1.88p

Table 2: CNTFET performance analysis for different configuration Vdd = 1V

	CIRCUIT NAME-CNTFET	Current (A)	Power (W)	Energy (J)	Delay (S)
I	QUATTRO-10T	34.23u	19.98u	134.95f	4.44p
II	WE-QUATTRO-12T	52.80u	52.74u	236.91f	2.54p
III	RHD-12T	15.66u	5.006u	26.93f	1.18p
IV	RHM-13T	16.79u	3.29u	14.83f	1.08p
V	RSP-14T	47.59u	24.006u	107.9f	419.59f
VI	DICE	256.24n	109.1n	609.76a	866.78f

compared to another configuration. When the current is concerning the FinFET is higher due to the rejection of leakage current through multigate control. CNTFET device configuration is three times lower in current when compared to FinFET and half that of CMOS. All SRAM configurations showed a lower delay when compared to CMOS and FinFET.

Tables 4–6 show the performance of various configurations for current, power, and energy. There were variations in power, energy, and delay for different SRAM circuits. The configuration, which was good in power consumption, showed a high delay. The figures show the detailed comparison of the configuration toward power, energy, and delay.

The netlist of FinFET and CNTFET circuits was written as per the device predictive technology models. The predictive technology models contain the electrical and physical models, which were used for the implementation. The tables show the device parameters used for the CNTFET and FinFET. For the CMOS, conventional model files were available as per the technology requirement.

Figures 3–6 show the performance comparison of different SRAM configurations for different devices. The investigation shows that the SRAM cells differ in the power consumption and delay. The CNTFET circuits consume low power when compared to CMOS and FinFET circuits. For high-current driving circuits and radiation hardening, the DICE circuit can be used, but with the tradeoff of high-power consumption. All the circuits designed and implemented can avoid radiation hardening in their own way. The power and current details make the design to choose between the applications. In biomedical applications, the information is very high, so current is an important parameter, but power can be compromised due to non-battery-operated devices.

Table 3: FinFET performance analysis for different configuration Vdd = 1V

	CIRCUIT NAME FINFET	Current (A)	Power (W)	Energy (J)	Delay (S)
I	QUATTRO-10T	266.34u	133.69u	692.47f	288.52f
II	WE-QUATTRO-12T	291.55u	104.57u	501.04f	3.62p
III	RHD-12T	35.49u	7.15u	32.78f	931.01f
IV	RHM-13T	61.71u	9.45u	47.31f	1.14p
V	RSP-14T	166.53u	43.16u	206.93f	1.37p
VI	DICE	274.1u	199.56u	884.51f	16.94p

Table 4: Performance analysis for the current different configuration Vdd = 1V

Sl. no.	CIRCUIT NAME	CMOS	FINFET	CNTFET
		Current (uA)		
I	QUATTRO-10T	90.99	266.34	34.23
II	WE-QUATTRO-12T	122.4	291.55	52.80
III	RHD-12T	19.33	35.49	15.66
IV	RHM-13T	14.20	61.71	16.79
V	RSP-14T	35.85	166.53	47.59
VI	DICE	149.84	274.1	0.256

Table 5: Performance analysis for power different configuration Vdd = 1V

Sl. no.	CIRCUIT NAME	CMOS	FINFET	CNTFET	Application
		Power (nW)			
I	QUATTRO-10T	54.65	133.69	19.98	Battery operated
II	WE-QUATTRO-12T	100.12	104.57	52.74	Multimedia
III	RHD-12T	11.75	7.15	5.006	Space
IV	RHM-13T	4.71	9.45	3.29	Battery operated
V	RSP-14T	7.93	43.16	24.006	Biomedical
VI	DICE	96.9	199.5	109.1	Biomedical

Table 6: Performance analysis for energy different configuration Vdd = 1V

Sl. no.	CIRCUIT NAME	CMOS	FINFET	CNTFET
		Energy (fJ)		
I	QUATTRO-10T	264.17	692.47	134.95
II	WE-QUATTRO-12T	494.19	501.04	236.91
III	RHD-12T	45.35	32.78	26.93
IV	RHM-13T	23.57	47.31	14.83
V	RSP-14T	39.24	206.93	107.9
VI	DICE	501.6	884.51	0.609

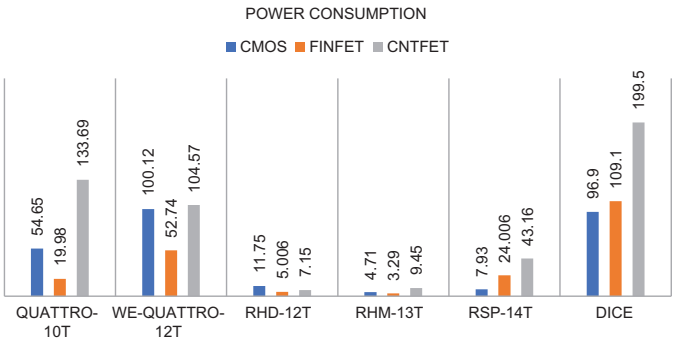

Fig. 3: Power comparison of different SRAM configurations for different devices

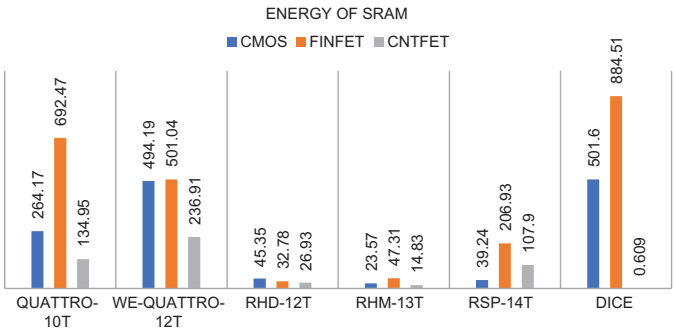

Fig. 4: Energy of different SRAM configuration for different devices

Table 7: Performance analysis for delay different configuration Vdd = 1V

	CIRCUIT NAME	CMOS	FINFET	CNTFET	Application
I	QUATTRO-10T	1.99	0.288	4.44	Multimedia
II	WE-QUATTRO-12T	55.60	3.62	2.54	Multimedia
III	RHD-12T	6.03	0.931	1.18	Space
IV	RHM-13T	0.343	1.14	1.08	Space
V	RSP-14T	0.324	1.37	0.419	Biomedical
VI	DICE	1.88p	16.94p	866.78f	Biomedical

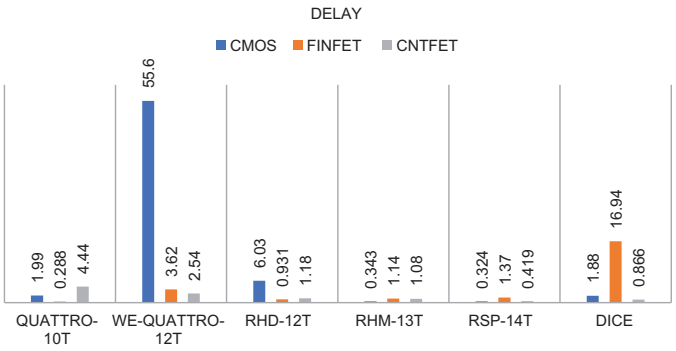

Fig. 5: Delay of different SRAM configurations for different devices

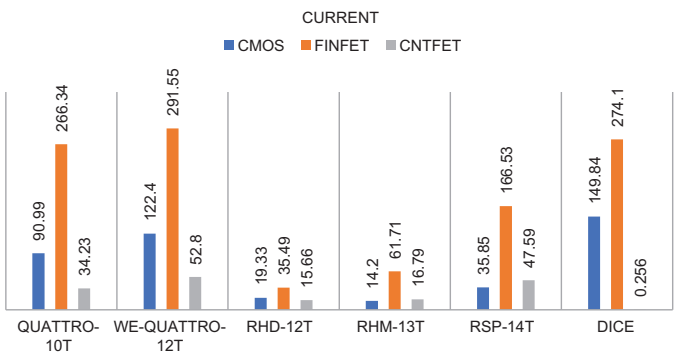

Fig. 6: Current of different SRAM configurations for different devices

Table 8: Primary parameters in PTM [29]

Parameters	Value n-type FinFET	Value p-type FinFET
Channel length	32nm	32nm
Fin height	40nm	50nm
Gate oxide thickness	1.4nm	1.4nm
Threshold Voltage	0.29V	-0.25V
Fin thickness	8.6nm	8.6nm
V_{DD}	1V	1V

Table 9: PTM Technology parameters for CNTFET [29]

Parameter	Description	Value
L_{ch}	Physical channel length	32.0 nm
L_{geff}	The mean free path in the intrinsic CNT channel region	100.0 nm
L_{ss}	The length of doped CNT source-side extension region	32.0 nm
L_{dd}	The length of doped CNT drain-side extension region	32.0 nm
E_{fi}	The Fermi level of the doped S/D tube	0.6 eV
K_{gate}	The dielectric constant of high-k top gate dielectric material	16.0
T_{ox}	The thickness of high-k top gate dielectric material	4.0 nm

Conclusion

This paper presents a detailed investigation of the sources of radiation and the configuration needed in SRAM to eliminate them. The logic values and the memory reliability were affected. An investigation on different semiconductor transistors, CMOS, FinFET, and CNTFET, was conducted in this work. Apart from all conventional circuits, radiation-hardened circuits were designed with a different configuration. The radiation affected in different nodes in the circuit can be rectified through different SRAM structures using multimodal and feedback concepts. The designs were implemented, and the performance was compared for the different devices. It was analyzed that the configuration shows different performance for different devices. The implementation was done in Synopsis with predictive technology models of the Stanford University and TSMC in 32 nm technology.

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