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Research Article

A New Blind Zone Free PFD in Fractional-N PLL for Bluetooth Applications

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ABSTRACT
This paper presents a new Phase Frequency Detector (PFD) used in the Fractional-N synthesizer PLL for the Bluetooth range frequencies using TSPC based D-FF. The PFD is designed by using 16 transistors. The operating frequency of the PFD can be modelled in between 2.2GHz-3.8GHz with an input reference frequency is applied of about 50MHz. The design of PFD is done by using GPDK 45nm CMOS technology on SPECTRE simulator with 1.8 V supply voltage. The designed PFD is having maximum operating range and free from blind zone. The results reported in this paper are compared and focused on the blind zone and minimum jitter contribution. The designed PFD consumes least power, minimum number of transistors and minimum jitter contributed by the transistors as compared with the reset free based PFD.

Keywords: PLL (Phase Locked Loop), VCO (Voltage Controlled Oscillator), CP (Charge Pump, PFD (Phase Frequency Detector)

1. Introduction

A Phase Locked Loop (PLL) is a sort of circuit that is commonly employed in communication systems and can be utilised in AM/FM radio receivers, frequency multipliers, frequency demodulators, divisions, and synthesisers, among other things. Recent improvements in IC design technology have resulted in the design of high-performance PLLs that have become more reliable and cost-effective. Now the entire PLL circuit can be summed up as part of a larger circuit on a single system on chip. The PFD's power usage accounts for a significant portion of the PLL's total consumption of power. As a result, by lowering the consumption of power in the PFD, the total consumption of power in PLL can be lowered. The major goal of the PFD design is to get a very high running frequency while using very little power. Many researchers have proposed various PFD designs to attain high efficiency with minimal power consumption. Many researchers have proposed various PFD designs to reach high working frequencies, although power consumption has been reported to be relatively significant [1-4]. This article proposes a novel PFD architecture with no blind zone, low energy dissipation, and high frequency operation.

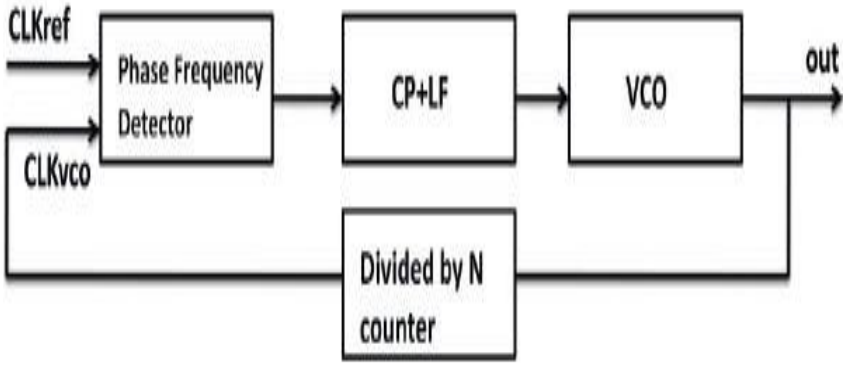

Fig.1: PLL Block Diagram

Figure.1 shows a traditional block diagram of a PLL. The primary goal of PLL is to obtain a signal with the same phase as a reference signal. After many repetitions of comparing the reference and feedback signals, this is achieved. One of the most important components in PLL circuits is the Phase Frequency Detector (PFD). The difference of phases between the feedback clock and reference clock is proportional to the error output signal produced by PFD. Another crucial component of PLL is the Charge Pump (CP). Phase or difference of frequency information of two input signals is converted into a current first by a filter section and then converted to voltage and utilised to tune a Voltage Controlled Oscillator (VCO) toward the input reference frequency via CP and Loop Filter & Low Pass Filter .Loop Filter (LF) and Low Pass Filter provides essential signal control for the VCO as well as to store the CP charge. VCO's job is to react as per speed up or slowdown of feedback signal depending on the PFD's mistake. If creates an up (UP) signal, the VCO speeds up and vice versa respectively and given back to the PFD, which recalculates the phase difference, resulting in a closed loop frequency control system.

2. Conventional Architecture of Phase Frequency Detector

Figure.2 depicts the conventional PFD architecture. The dead zone free, increased consumption of power at operating high frequency, and larger area due to the huge transistor count are the key disadvantages of this design.

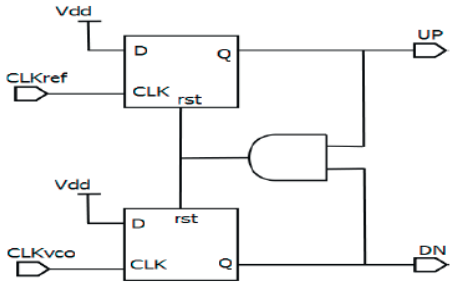

Fig.2: Conventional PFD with NAND based D Flip-flop

It is made up of 2 Edge-Triggered resettable D flip-flops with logical ONE to inputs of D and one AND gate. The CLKref ,CLKvco inputs serve as a clock for the flip-flops. Assuming UP=DN=0 at the start, UP rises as CLKref climbs. If CLKvco rises after this event, DN rises as well, and the AND gate resets both flip-flops. For a brief period of time, UP and DN are both high, but difference of the values represents frequency difference or input phase.

The non-ideal behaviour was demonstrated by Mozhgan Mansuri et al., who used the CKLref reference clock to lead the CLKvco output clock, resulting in a UP output [1]. Due to the finite reset delay, the next leading edge CLKref comes before the reset of D-flip-flops because the input phase difference is approaching 2 pi. The reset disables the UP signal and overrides the new CLKref edge. They also said that t_{reset} is not a function of input frequency and is determined by the latency of logic gates in reset circuit [1]. As a result, the new design was founded on the idea that if the reset delay could be eliminated, the enhancement of operating frequency of the PFD or PLL could be done. As a result, the proposed design focuses on eliminating reset latency in order to totally eliminate dead zones.

Proposed PFD Design

By adding TSPC logic, the reset path is eliminated, allowing the PFD to operate at a higher frequency. The suggested PFD uses only sixteen transistors, reducing the PLL's power consumption and size.

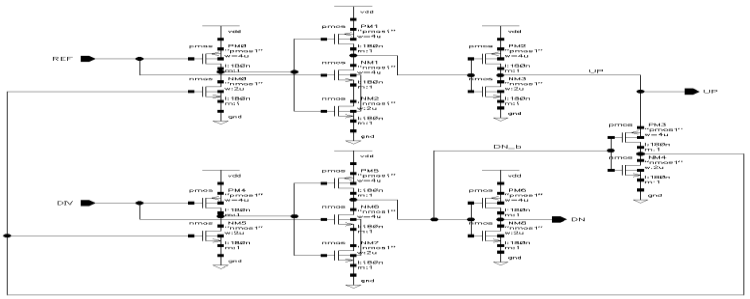

Fig.3: Proposed PFD Schematic

Figure 3 depicts a schematic of the planned PFD. PMOS transistors are P M0 through PM6, while NMOS transistors are NM0 through NM08. The operation's principle is outlined below. The two signals CLKref and CLKvco are initially set to logic ZERO. NM7, NM8, and NM2 switch ON at the edge of CLKref rising, and the UP signal goes to logic high. NM1, NM0, and NM2 turn on at the edge of CLKvco rising, were pushing DN to go high. When both UP and DN are high, the logic levels are pulled down to logic zero, allowing UP and DN to reset immediately.

Simulation Results

Transient analysis response of PFD

Figure 4 shows the timing diagrams for the proposed PFD. It shows that when CLK_{vco} is 3ns behind CLK_{ref}, the UP signal becomes high, and when both are high, both the UP and DN signals quickly go down. As a result, the planned PFD functions as a phase frequency detector in the same way that a traditional PFD does.

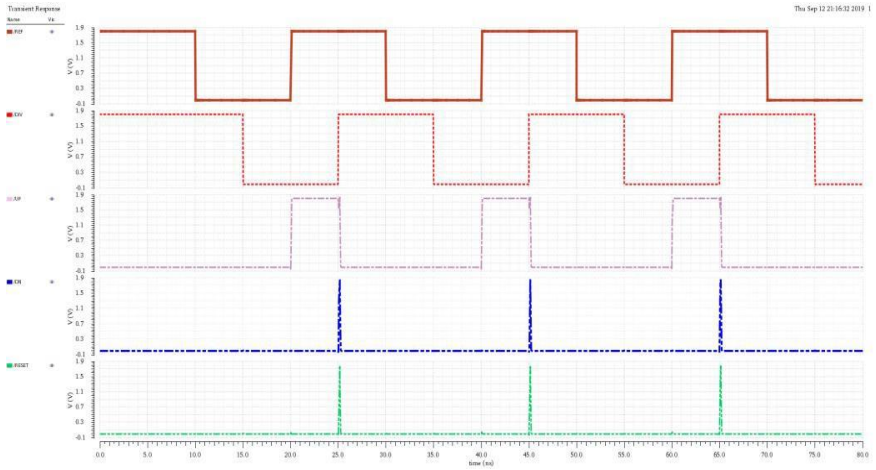

Fig.4: PFD Timing diagram with CLKref leading CLKout

Characteristics of Phase

In Fig.5, the output average value of PFD is shown against the phase difference between the CLKref and CLK_{vco} signals. Dead zones are freed in design since it do not rely on the reset and instead relies solely on the CLKref and CLK_{vco} signals arrival. When it comes to the linearity property, Fig.5 shows that the suggested PFD is almost linear throughout the time. It's worth noting that design of proposed circuit has a wider linearity range than the PFD documented in the literature [2].

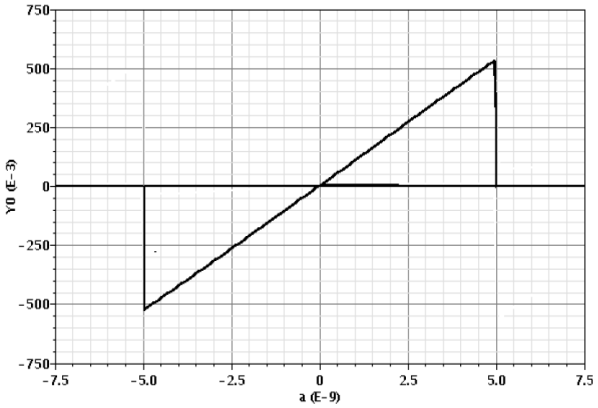

Fig.5: Phase Characteristics of PFD

Analysis of Phase Noise

Phase noise is a random variation in the phase of a signal. It is the frequency domain representation of jitter, which is created by time domain instabilities and causes fast, short- oscillations in the phase.

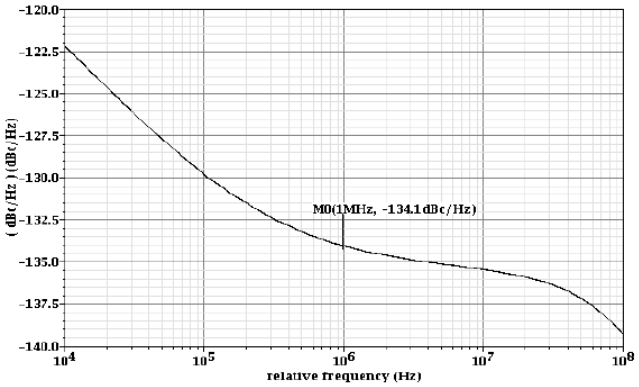

Fig.6: PFD Phase Noise Analysis

In Fig.6, simulation of phase noise for proposed PFD is presented, with CLK_{ref} ,CLK_{out} set to 100 MHz which are in phase. PFDs are subjected to noise from a variety of causes, including dead zone, transistors, and reset time delay. At 1 MHz offset, it can be shown that proposed PFD has reduced phase noise values of -132.44 dBc/Hz. Conventional PFD has a phase noise of -122 dBc/Hz [2]. As a result, the proposed circuit is suited for applications with low jitter.

Operating Frequency (Maximum)

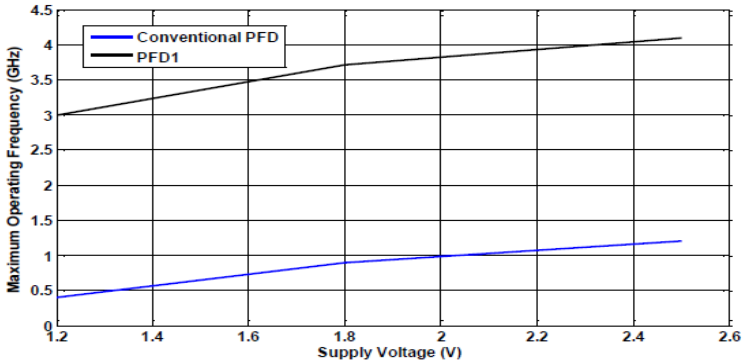

Fig.7: Conventional PFD and proposed PFD maximum operating frequency as a function of supply voltage.

Figure 7 shows the Conventional PFD and proposed PFD maximum operating frequency as a function of supply voltage. The highest typical PFD functioning frequency is 800 MHz, while that of PFD is 3.72 GHz at a 1.8 V supply voltage, as shown in fig.7.

Requirement of Area

The suggested PFD is implemented in 45nm technology utilising the GPDK045 library. PFD's chip arrangement is shown in Figure 8. PFD's final installation area measures 15.1356 micro metre wide by 8.23 micro metre long (Area= 124 micron^2).

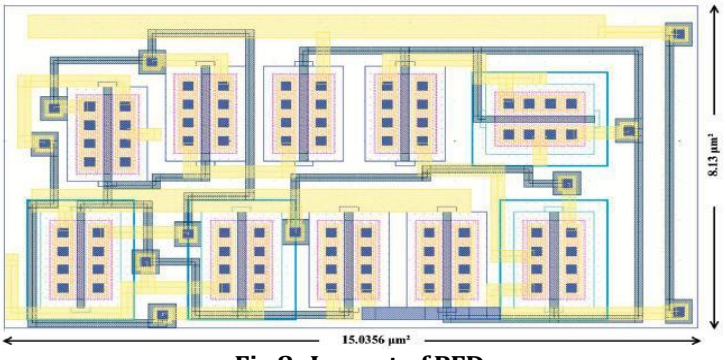

Fig.8: Layout of PFD

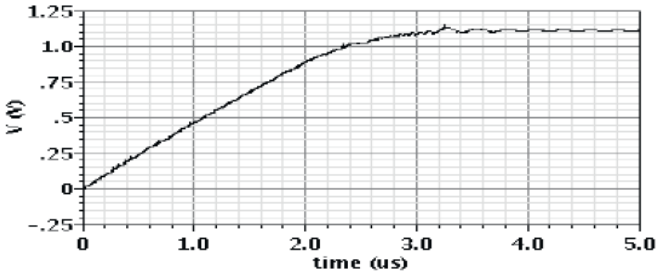

Fig.9: Response of PLL acquisition time using PFD

Discussion

Table I shows a comparison of various PFD architectures with various design parameters performance. The PFD is totally dead zone-free, and the PFD's Reset time is zero.

Table 1: Output Comparison of Simulated PFD

	Conventional PFD	**PFD**	[7]	[10]	[11]	[8]
Power consumption in µW	1650	**12.54**	76	351	5.4	134
No. of Transistor	54	**16**		-	20	20
Maximum Operating Frequency in GHz	0.8	**3.8**	4.1	2.4-2.48	2.3	3
Reset Time in ns	0.152	**0**	-	-	-	
Dead zone in ps	70	**0**	25	-	0	120
Phase noise dBc/Hz@1M Hz	-122	**-132.44**		-	-158.3	-
Area in µm2	452	**124**	250	350	-	-

PFD employs only sixteen transistors, where as a traditional PFD uses 54. PFD has a maximum operating frequency of 3.72 GHz, which is greater than previous PFDs [2, 3]. When comparing PFD to standard PFD, it is found that dissipation of power is reduced by 97 percent and area is reduced by up to 27 percent. Compared to traditional PFD, phase noise is reduced dramatically to -133.4 dBc/Hz @ 1 MHz. It is also noted that acquisition range of PLL utilising proposed PFD is 4.25 seconds, which is much better than PLL described in [6] (22.5 seconds).

Conclusion

This study proposes a simple and unique PFD with sixteen transistors. The removal of the reset path totally eliminates the dead zone, which is a big benefit of this design. These PFD have been shown to operate at frequencies up to 4.6 times higher than traditional PFD. When compared to other PLL published in the literature, the acquisition time of a PLL implemented using this PFD is quite short (4.6 s). As a result, PLL proposes that PFD is suited for applications requiring low power, low jitter, zero dead zone, and high speed.

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