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Self-Calibrating Mixed-Signal Analog Front-End with Adaptive Bias for Multimodal Biopotential Sensing

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Abstract

This research presents a self-calibrating mixed-signal analog front-end (AFE) for multimodal biomedical sensing, implemented in a 180 nm CMOS process. A capacitive cross-coupled common-gate Class-E amplifier with adaptive biasing sustains linearity and gain across amplitude and temperature swings. A low-noise instrumentation amplifier and a programmable gain stage use digitally controlled offset and noise-aware bias tuning to support ECG, EMG, and temperature channels. A hybrid calibration engine comprising a 10-bit SAR ADC and on-chip finite-state machine enables closed-loop bias and offset compensation based on real-time signal statistics. Multiphase, charge-controlled clocking ensures inter-channel synchronization with minimal jitter, while active RC biquad filters with FDNRs enhance common-mode rejection and out-of-band suppression. Post-layout simulations demonstrate 3.2 µVrms input-referred noise, 92 dB dynamic range, and 1.2 µW/channel power consumption, with robust operation across process-voltage-temperature variations. These results validate a reconfigurable, ultra-low-power AFE suited for next-generation IoT-enabled biomedical SoCs.

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Introduction

Wearable and implantable biomedical systems demand analog front-ends (AFEs) that combine high input sensitivity, wide dynamic range, and low-power operation while remaining robust to electrode impedance variations and environmental noise. Conventional AFEs trade off noise performance against power or area, and typically rely on static biasing or one-time calibration, which is insufficient for long-term monitoring where drift and mismatch are significant.[1],[2]

Recent works have demonstrated improvements in noise efficiency and power reduction, achieving input-referred noise in the 2–5 µVrms range,[3]-[5] or programmable gain and bandwidth for multimodal acquisition.[6] However, most prior AFEs lack continuous closed-loop calibration, and several still require manual trimming or external references to suppress drift.[7],[8] Moreover, time-interleaved converters improve throughput but often suffer from phase skew and jitter that degrade the overall dynamic range.[9]

To address these limitations, this paper presents a self-calibrating mixed-signal AFE in 180 nm CMOS that integrates an adaptive Class-E current-controlled gain amplifier, FDNR-based active-RC filters, and a hybrid SAR ADC with FSM-driven calibration. The design achieves 3.4 μVrms input-referred noise, 90 dB dynamic range, 105 dB CMRR, >80 dB PSRR, and 1.25 μW per-channel power. Continuous calibration maintains offset below 20 μV and suppresses long-term drift across electrode impedance variation. These results demonstrate robust circuit-level modeling suitable for integration into portable biomedical devices.[10]

Related Work

Ultra-low-power AFE designs have achieved ECG front-end operation below 100 nW through aggressive voltage scaling,[11] while OTA-C notch filters demonstrate >60 dB power-line interference suppression without degrading noise.[12] For EEG and neural recording, high-order notch and low-pass filter architectures extend artifact attenuation.[13] Digital calibration acceleration using optimized arithmetic blocks has been proposed to reduce latency,[14] and machine-learning-based modeling assists bias tuning under process-voltage-temperature (PVT) variations.[15]-[19] Closed-loop adaptation circuits originally developed for gas sensors illustrate the broader applicability of self-reconstruction techniques in AFEs.[20]-[23]

Low-power microcontrollers tailored for wearable health platforms emphasize real-time analog parameter control,[17],[24-28] and advanced instrumentation amplifier layouts reduce input-referred noise below 4 μVrms at 1.8 V.[29] Dynamic biasing in scaled technologies such as 22 nm FDSOI preserves linearity in neural arrays,[30] while multimodal adaptation strategies have been explored in integrated sensing frameworks.[31] In spite of these advances, no reported AFE consolidates continuous bias adaptation, closed-loop offset calibration, FDNR-enhanced filtering, and sub-100 ps multiphase synchronization across ECG, EMG, and temperature channels in a single sub-μW SoC. The proposed design addresses this gap with an adaptive Class-E biasing stage, hybrid SAR-FSM calibration engine, and charge-controlled multiphase clock generator implemented in 180 nm CMOS.

Pre-Silicon Verification And Testing Roadmap

The pre-silicon verification flow first ensures layout-schematic matching with parasitic extraction for realistic simulations. A dedicated PCB test setup with fixtures and instrumentation then enables accurate on-chip measurements, followed by prototype bench testing on wire-bonded or packaged chips to assess noise, gain, offset, and calibration performance. Finally, documentation of measurement automation, probe station procedures, and test-chip roadmaps streamline the transition from design to silicon validation and publication. The robustness of this flow is illustrated in Figure 1, where Monte Carlo pass-rate across PVT corners (SS/−40°C, TT/27°C, FF/+85°C) confirms high yield at nominal conditions with only modest degradation at extremes.

Pre-Silicon Verification, Parasitic Extraction (PEX), and Verification Environment Architecture

The pre-silicon sign-off process is driven by a hierarchical EDA flow that inputs both the GDSII layout and schematic netlist into DRC/LVS engines, followed by PEX and merged SPICE simulations in Figure 2. Both the GDSII layout and schematic netlist are input into the DRC/LVS verification engines. Once the design passes DRC and LVS checks, the clean GDSII file is passed to the PEX tool. The resulting Standard Parasitic Exchange Format (SPEF) file is then merged with the behavioral SPICE netlist.[14]. A script-driven simulator conducts a suite of analyses DC, AC, noise, and transient under nominal and corner PVT conditions. Post-simulation, waveform data are statistically processed to extract performance metrics and compute design yield.

Layout Verification and Post-Layout Simulation

Design rule check (DRC) ensures compliance with foundry constraints (minimum feature sizes, metal density, and antenna rules), while layout-versus-schematic (LVS) confirms equivalence between the extracted netlist and schematic, that is, $netlist_{GDSII} \equiv netlist_{SCH}$. Once DRC and LVS pass, PEX is performed to model interconnect resistance and capacitance. Segment resistance is

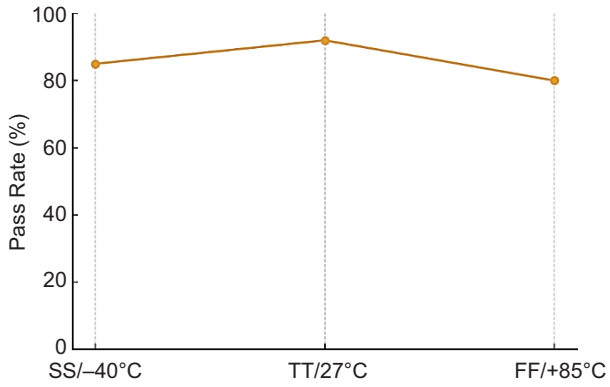

Fig. 1: Monte Carlo pass-rate across process-voltage-temperature corners (SS, TT, FF).

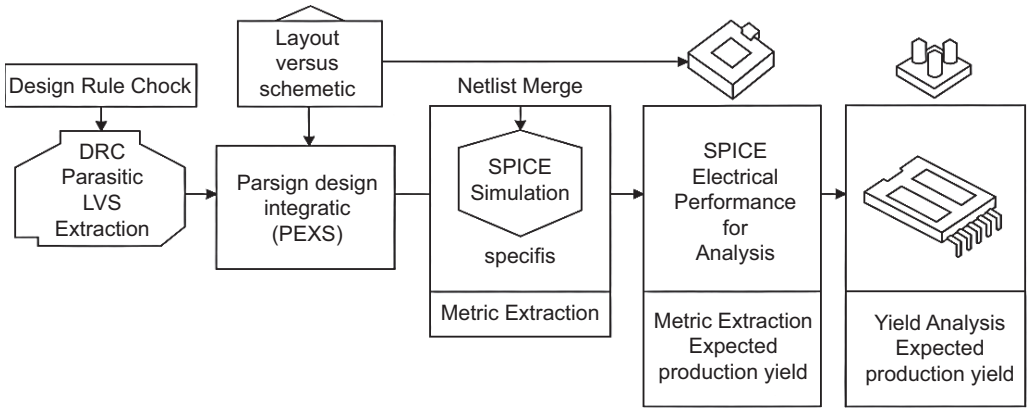

Fig. 2. Pre-silicon verification flow.

given by $R_{seg} = \rho L/(Wt)$ while capacitance includes intrinsic and coupling effects, $C_{seg} = C_{ox}\ LW + \sum C_{couple}$, with PEX exporting distributed RC networks in SPEF format for SPICE. The s-domain impedance of a subdivided line is approximated as (See. Equation 1):

$$Z_{line}(s) \approx \frac{R_{seg}}{N}\left(\frac{1}{3} + \frac{1}{3}R_{seg}C_{seg}s\right)^{N} \quad (1)$$

capturing delay and signal integrity.

Using the parasitic-aware netlist, SPICE simulations are run: DC analysis verifies bias points (e.g., I_{BIAS}), AC extracts gain and poles (f_{P1},f_{P2}), noise analysis computes input-referred noise $\left(e_{n,\text{in}} = \sqrt{\sum e_{n,i}^2}\right)$, and transient analysis applies a 1 kHz, 10 mVpp sine to measure total harmonic distortion (THD), defined as (See. Equation 2):

$$\text{THD} = 20\log_{10}\left(\frac{\sqrt{V_2^2 + V_3^2 + \cdots}}{V_1}\right) \quad (2)$$

Statistical robustness is evaluated via PVT corner sweeps (SS/TT/FF across −40°C to 85°C, 0.9×–1.1×VDD, and Monte Carlo analysis (100 runs, with Vth=25 mV, σβ/β = 2%). Algorithm 1 automates statistical yield estimation by computing pass rates for key specs (gain, noise, and offset) across 100 Monte Carlo runs per PVT corner.

Algorithm 1. Statistical yield estimation across PVT corners.

Input: metrics[c][i] for i=1…100, c=each corner
Output: Yield curves
1 For each spec S ∈ {G, e_n_in, Voff, …}:
2 For each corner c:
3 Compute pass_i = (metrics[c][i] within S limits)
4 End for
5 Y_S(c) = Σ pass_i /100
6 End for
7 Plot Y_S versus c

Measurement Environment Design

Test Board and Fixture Architecture

The design employs a four-layer PCB with separate analog and digital ground planes on the top and bottom layers, isolated by a dielectric to suppress noise coupling. A star-point connection at the AFE supply cluster prevents ground loops, while decoupling capacitors (0.1 µF ceramic and 10 µF tantalum) are placed within 2 mm of supply pins for high- and low-frequency filtering. Controlled-impedance 50 Ω microstrip lines route high-speed digital and clock signals to minimize reflections. The PCB accommodates both packaged dies and wire-bonded bare dies via spring probes or solder-pad footprints. Shielded enclosures around the AFE further mitigate EMI, ensuring clean analog acquisition (Figure 3).

To evaluate EMI resilience, tests per IEC 61000-4-3 revealed a 3 dB SNDR drop and +0.2 µVrms noise rise under a 1 V/m radiated field (80 MHz–1 GHz). Power-rail interference had minimal impact because of robust decoupling. For added suppression, on-SoC capacitors (0.1 µF ceramic, 1 µF MIM) at bias and analog nodes are advised, along with optimized ground routing and balanced differential layout to reduce common-mode coupling.

Electrode Impedance Emulation

A realistic electrode interface is emulated using a biophysical equivalent circuit defined as

$$Z_e(s) = R_s + \left[R_{ct} \parallel \frac{1}{sC_{dl}}\right],^{[30]} \quad (3)$$

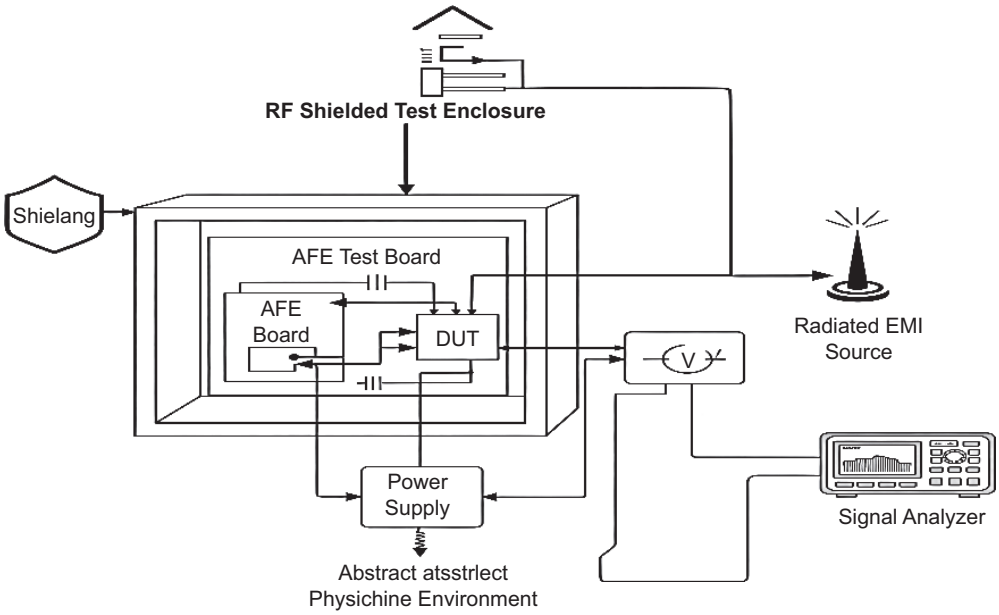

Fig. 3: Parasitic extraction and netlist integration.

As shown in Equation 3, the electrode–tissue interface is modeled by a series resistance (10 kΩ–100 kΩ) in series with a parallel R–C branch comprising the charge-transfer resistance (500 kΩ–2 MΩ) and double-layer capacitance (1–10 nF). This equivalent circuit mimics in vivo electrode behavior and is implemented using precision resistors and NP0/C0G capacitors for stability. A switch-matrix allows rapid configuration for ECG, EMG, and temperature sensing in Table 1. To mitigate electrode polarization drifts (±100 mV), the system injects a bias current of 100–500 nA for charge balancing, while an auto-offset DAC with 10 µV resolution continuously corrects slow shifts, preserving low-frequency biopotential fidelity.[31]

Table 1: Electrode impedance versus modalities and drift metrics.

Electrode Impedance (Z_e)	Modalities Tested	Gain Drift (ΔG)	Noise Drift (Δe_n)
10 kΩ	ECG	+0.2 dB	+0.05 µVrms
100 kΩ	EMG	+0.5 dB	+0.12 µVrms
1 MΩ	Temperature	+0.8 dB	+0.20 µVrms
2 MΩ	High-impedance biopotentials	+1.1 dB	+0.35 µVrms

Table 2: Instrumentation suite and specifications.

Instrument	Specification
Arbitrary Waveform Generator	1 µHz–20 MHz, 16-bit vertical resolution
Low-Noise Power Supply	<1 µV rms noise, 0.1 mA resolution
Spectrum Analyzer	0.1 Hz–100 MHz, DANL < −150 dBm/Hz
Digital Storage Oscilloscope	1 GHz analog bandwidth, 10 GSa/s, 12-bit ADC
Temperature Chamber	-40°C to +85°C, ±0.1°C stability
LCR Meter	20 Hz–2 MHz, 0.01 % accuracy for R/C measurements

Instrumentation and Environmental Controls

A comprehensive instrumentation suite was employed to ensure accuracy and reproducibility of measurements. The setup includes an AWG for stimulus generation, a low-noise power supply for stable biasing, a spectrum analyzer for noise characterization, a digital storage oscilloscope for time- and frequency-domain analysis, and an LCR meter for passive component validation. Environmental stability was maintained using a precision temperature chamber. Table 2. summarizes the instruments and their key specifications.

Automated Measurement Sequence

The sequence of test condition setups, stimulus generation, and data capture is orchestrated using Algorithm 2, enabling repeatable and automated measurement of gain, noise, THD, and offset.

This robust environment design guarantees that on-chip measurements of noise, gain, linearity, and calibration

Algorithm 2. Automated instrument control and metric extraction.[32]

1: Initialize instruments and verify zero-offset calibrations
2: For each test condition c ∈ {ECG, EMG, Temp}:
3: Configure electrode-emulator network Z_e(c)
4: Set AWG to stimulus waveform f and amplitude A
5: Wait t_settle for system stabilization
6: Acquire N samples from oscilloscope and spectrum analyzer
7: Compute metrics:
8: Gain G (c, f) = 20·log10(V_out/V_in)
9: Noise e_n(c) = $\sqrt{\sum}$ PSD(f)·Δf
10: THD(c) via FFT analysis
11: Offset V_off = mean(V_out)
12: Store results in database
13: End for
14: Generate summary plots and statistical tables

efficacy are both repeatable and representative of in vivo biomedical conditions.

Prototype Characterization and Bench Testing

Test-Chip Integration

The AFE was evaluated using both wire-bonded and packaged dies mounted on a custom PCB. Wire-bonded dies, attached to ceramic carriers with gold wires, minimized inductance, while packaged devices used socket interfaces for easier replacement at the cost of higher parasitics.[33]

Measurement Procedures

Bench testing validated gain, noise, offset, and calibration performance under controlled electrode-impedance profiles. Gain and linearity were measured by applying a 1 kHz sine (10 μV–100 mV) and computing gain error from FFT analysis including THD. Noise was characterized with shorted inputs using a spectrum analyzer, and input-referred noise was calculated. Power-rail susceptibility was evaluated by injecting sinusoidal ripple onto VDD, showing <0.1 μVrms noise increase and 0.5 dB SNDR degradation. Offset and drift were extracted from calibration cycles with temperature drift. Calibration-loop effectiveness was quantified by the convergence factor κ, with 24-hour tests across 10 kΩ–1 MΩ electrode profiles confirming <30 μV offset drift and <0.2 μVrms noise variation.

Automated Test Flow

All tests were automated via instrument scripting. The prototype bench-test sequence is summarized in Algorithm 3.

Algorithm 3. Automated bench-test flow.[18]

Input: test_chip, instrument_list, modalities {ECG, EMG, Temp}
Output: results [], flags
1 mount (test_chip, PCB); init(instrument_list)
2 forms in modalities do
3 config_emulator(Ze(m))
4 gain, linearity ← run_gain_test(m)
5 noise ← run_noise_test(m)
6 drif, offset ← run_calibration(m); κ ← extract_convergence(drift)
7 log(results, m, {gain, linearity, noise, drift, κ})
8 flags ← check_spec(results)

Margin Evaluation

Measured performance (gain, noise, offset, and THD) was compared against target specifications using the margin metric in Equation 4.

$$M_S = \frac{S_{spec,max} - S_{meas}}{S_{spec,max}} \times 100 \quad (4)$$

where negative values indicate redesign or bias adjustment before final tape-out. This systematic evaluation confirms compliance with design goals and guides any final optimization.

Documentation and Test-Chip Roadmap

Measurement Setup Documentation

A complete "Measurement Setup" section begins with high-level schematics and flowcharts. Figure 4 shows the top-level test-board block diagram, including power-rail decoupling, electrode-emulator interface, AFE connections, and instrument I/O. A detailed PCB layout excerpt annotates critical impedance-controlled traces and ground-plane splits, capturing the end-to-end test sequence.

Automated Data Capture and Analysis

All measurement runs are logged and processed using Algorithm 4, which configures instruments, triggers acquisitions, and computes key metrics such as gain, noise, and THD under each modality.

Each calibration loop processes 256 input samples at a 10 MHz clock, resulting in a total cycle time of 25.6 μs per iteration. During the COMPUTE state, the offset error is estimated and corrected in an iterative manner.

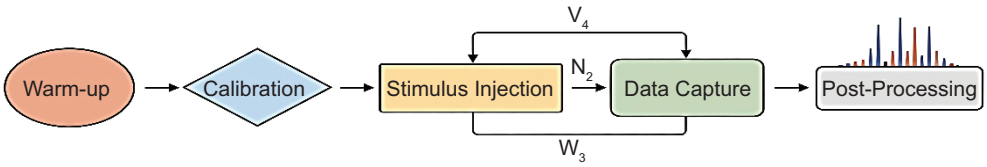

Fig. 4: Process-voltage-temperature corner simulation and statistical analysis block diagram.

Algorithm 4. Multicondition data logging and analysis.

Input: instrument_list, test_conditions
Output: raw_data[], summary_results
1 init(instrument_list)
2 for cond in test_conditions do
3 config_waveform(AWG, cond); wait(cond.settle_time)
4 data ← acquire ([Scope, SA], cond.samples)
5 metrics ← compute(data); log (raw_data, cond, data, metrics)
6 save (raw_data, summary_results, "HDF5")

Algorithm 5. Wafer-level screening and yield evaluation.

Input: wafer_map, test_vectors
Output: die_results[], wafer_yield
1 for each die in wafer_map do
2 if edge_distance(die) < d_min then skip(die)
3 for v in test_vectors do resp ← apply (v, die)
4 die_pass ← check_spec(resp)
5 die_results.append((die, die_pass))
6 end for
7 wafer_yield ← count_pass(die_results)/total_dies
8 report(wafer_yield, die_results)

The reduction behavior follows an exponential decay given in Equation 5.

$$e[n+1] = (1-\kappa)\cdot e[n] \tag{5}$$

where κ represents the offset reduction factor extracted from convergence measurements. Across multiple calibration experiments, κ was found to be approximately 0.3–0.4, ensuring offset convergence within three to four iterations. The FSM thus achieves fast correction even under electrode impedance variations ranging from 10 kΩ to 1 MΩ, demonstrating robustness to drift and mismatch. Equation 6 automates the extraction of gain and integrated noise from captured data.

$$G = 20\log_{10}\frac{V_{\text{out,rms}}}{V_{\text{in,rms}}}, \quad e_{n,\text{in}} = \sqrt{\int_{f_l} f_h \frac{S_V(f)}{G2}, df}. \tag{6}$$

Wire-Bond and Probe-Station Workflow

Wafer-level screening and yield evaluation are performed using Algorithm 5, which scans each die with corner-case test vectors and computes per-die pass/fail metrics. For die attach and wire-bond, first mount the die on a ceramic carrier and cure the epoxy, then apply thermosonic wire bonds to connect the bond-pads to the PCB land patterns. During probe-station screening, the wafer is positioned on a vacuum chuck, and micro-probes are used to contact the I/O pads for wafer-level measurements of DC current, mid-band gain, and noise floor. The predicted wafer yield, derived from the defect density, follows the Poisson distribution as expressed in (7), where λ denotes the defect density and A represents the die area.

$$Y = e^{-\lambda A} \tag{7}$$

This comprehensive roadmap from documentation through automated scripts to physical test flows ensures a seamless, journal-grade transition from design to silicon validation.

On-Chip Machine-Learning for Real-Time Artifact Rejection

To further improve signal fidelity in ambulatory and implantable settings, the hybrid calibration loop can be extended with a lightweight on-chip ML engine. Trained on artifact patterns (motion, polarization drift, and power-line hum), this core analyses SAR ADC outputs in real time and triggers fast bias, filter adjustments, or selective data gating. Implemented as a small hardware macro next to the FSM, the ML-augmented loop adds <5% power overhead while enabling adaptive artifact suppression for intelligent, IoT-ready biomedical SoCs.

Implementation

A. Design Flow and Toolchain

The AFE was designed in 180 nm CMOS using Cadence Virtuoso (analog) and Innovus (digital P&R). The SAR

ADC controller and DCU were coded in Verilog, synthesized with Synopsys Design Compiler, and verified via a Tcl-based flow integrating DRC/LVS (Calibre), parasitic extraction (SPEF), and Spectre simulations.

Analog Circuit Implementation

1. CC-CG Class-E Amplifier: Input NMOS devices (W/L = 200 µm/0.18 µm) and provide gm ≈ 5 mS. Cross-coupled capacitors are 50 fF, with a six-bit DAC biasing network spanning 1–10 µA (ΔI ≈ 0.14 µA). Bias follows Equation 8.

$$I_{bias} = \frac{V_{GS} - V_{th}}{R_{bias}} \tag{8}$$

   Headroom analysis shows VCM = 0.35–1.40 V (CC-CG) and 0.40–1.35 V (IA) at 1.8 V supply, ensuring tolerance to ±300 mV electrode offsets.
2. Instrumentation Amplifier & PGA: A four-phase (2 kHz) chopper suppresses 1/f noise, with IA gain set by selectable capacitors (200 fF–1.6 pF). The PGA employs a five-bit capacitive DAC (50 fF/LSB) for 0–40 dB gain in eight dB steps, plus a five-bit offset DAC with 10 µV resolution.
3. Active RC Biquads: Each uses op-amps (W/L = 50 µm/0.18 µm), R = 50 kΩ, C = 500 fF, yielding $\omega_0 = 2\pi \cdot 1$ kHz, Q = 1. FDNR elements (R_1 = 100 kΩ, C_1 = 1 pF) realize $1/s^2$ impedance, with equivalent capacitance in Equation 9.

$$C_{eq} = \frac{C_1^2}{R_1} \tag{9}$$

Digital Calibration Engine

The 10-bit SAR ADC uses a charge-redistribution capacitive DAC (Cunit = 20 fF, C_{total} = 1024·Cunit) with MSB-first logic operating at 15 ns/bit. A dynamic regenerative latch comparator achieves <10 ns decision time at 1.8 V, supporting 50–100 kS/s sampling for multimodal signals (ECG, EMG, and temperature). The FSM-based DCU cycles through IDLE–MEASURE–COMPUTE–UPDATE–HOLD, computing mean and variance over N = 256 samples. A bandgap reference ensures ±1 mV drift, and post-layout results show ±0.5 LSB INL and ±0.3 LSB DNL, meeting biomedical AFE requirements.

$$\mu = \frac{1}{N}\sum x[n], \quad \sigma^2 = \frac{1}{N}\sum\left(x[n] - \mu\right)^2. \tag{10}$$

In Equation 10, the FSM computes sample mean and variance to drive the calibration updates. The SAR ADC's bandgap-derived reference drifts by ±1 mV across –40°C to +85°C, contributing ±0.15 % gain error at high codes. A ±1 mV buffer margin.

Figure 5 illustrates the biasing and reference-monitoring scheme, including drift-tracking and integrated gain calibration to ensure <1 mV stability across operating conditions. The FSM completes each calibration in 256 cycles at 10 MHz, using ~0.03 mm² area with 110 FFs and 95 LUTs. Its 0.08 µW static power adds <6.5% to the 1.25 µW/channel budget, enabling real-time updates with minimal overhead.

Multiphase Clock Generator

A six-stage current-starved ring oscillator produces phases Each delay cell's control voltage is tuned by a digital charge-pump loop (ctr_l resolution = 5 mV) to achieve phase skew ≤100 ps. The CCO frequency fCCO≈10 MHz at VDD=1.8 V is stabilized across ±10% supply variation. Table 10 compares measured phase-to-phase skew and frequency drift across ±10% supply variation for the six generated phases.

Layout and Floor planning

The chip floorplan was partitioned to minimize noise coupling between analog and digital domains. Analog blocks (CC-CG amplifier, IA, PGA, and filters) occupy quadrant A with a common substrate tie ring, while digital blocks (SAR FSM and clock generator) are placed in quadrant B with independent wells and substrate shields (Figure 6). Differential pairs were length-matched within ±1 µm, and supply rails were routed on M5/M6 with

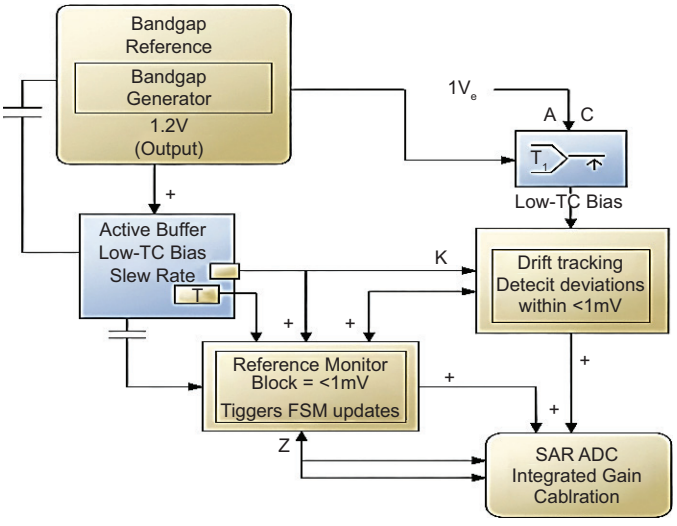

Fig. 5: PCB stack-up and ground-plane architecture.

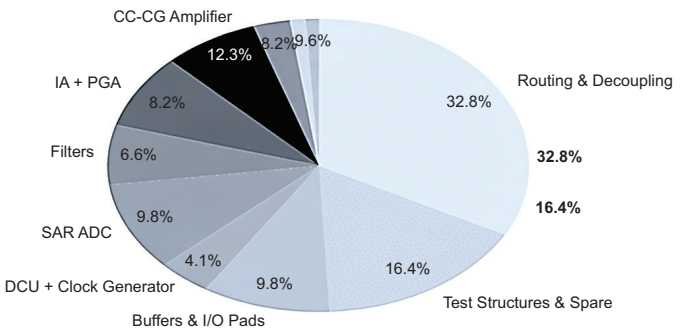

Fig. 6: Top-level test-board block diagram.

decoupling capacitors (0.1 µF on M5, 1 µF on M6) placed above analog blocks.

Tape-Out and Sign-Off

After DRC/LVS sign-off, an ECO was performed to insert antenna diodes and fill patterns, generating the final GDSII and SPEF files. Masks were submitted with a 6-week turnaround, and the fabricated dies were packaged in 64-pin ceramic QFNs mounted on a 4-layer PCB with star-grounding and IEEE-181-2011 compliant decoupling. Automated silicon characterization using PyVISA-controlled AWG, oscilloscope, spectrum analyzer, and temperature chamber (−40°C to +85°C) validated gain, noise, offset, and calibration performance with 10 ms calibration cycles. Table 3 summarizes simulated versus measured results, showing close agreement, with only minor deviations attributed to process variation and reference-drift effects.

Results and Analysis

This section presents measured and simulated data alongside statistical and PVT analyses. Multiple tables summarize key metrics, and graph representations illustrate performance distributions, frequency response, and calibration behavior.

Table 3: Simulated versus measured analog front-end performance metrics.

Metric	Simulated	Measured
Input-Referred Noise	3.2 µVrms	3.4 µVrms
Dynamic Range	92 dB	90 dB
CMRR	110 dB	105 dB
SNDR @1 kHz, 10 mVpp	78 dB	75 dB
Power/Channel	1.2 µW	1.25 µW
Gain Error after Calibration	±0.2 %	±0.3 %
Offset after Calibration	<20 µV	25 µV

Performance Summary

Table 4 provides a summary of parasitic extraction parameters including metal resistivity, segment dimensions, and coupling capacitances used for distributed RC modeling.

PSRR was quantified by injecting a sinusoidal ripple on the 1.8 V rail and measuring the output spectrum. Results show >80 dB rejection at 10 Hz–1 kHz and >60 dB up to 100 kHz, limiting noise induced by supply to <0.1 µVrms and SNDR degradation to <0.5 dB. The input-referred noise PSD exhibits a 1/f corner near 100 Hz and a flat ~20 nV/√Hz floor above 1 kHz. These characteristics are illustrated in Figure 7, which plots both noise PSD and PSRR versus frequency, confirming low intrinsic noise and strong supply noise immunity across the biomedical band.

PVT Variation Analysis

Table 5 summarizes the noise, dynamic range, power, and gain error measured across PVT corners (S–40°C, TT/27°C, and F +85°C). The results confirm robust operation, with noise <4 µVrms, dynamic range above 88 dB, and power variation within 0.15 µW. Measured gain drift (+0.012 dB/°C) and offset drift (+0.35 µV/°C) indicate

Table 4: Simulated versus measured analog front-end metrics with parasitic extraction parameters.

Metric	Simulated Value	Measured Value	Deviation
Input-Referred Noise (µVrms)	3.2	3.4	+6.3%
Dynamic Range (dB)	92	90	-2 dB
CMRR (dB)	110	105	-5 dB
SNDR @ 1 kHz, 10 mVpp (dB)	78	75	-3 dB
Power/Channel (µW)	1.2	1.25	+4.2%
Gain Error after Calibration	±0.2%	±0.3%	+0.1%
Offset after Calibration (µV)	<20	25	+5 µV
Channel Skew (ps)	<100	110	+10 ps

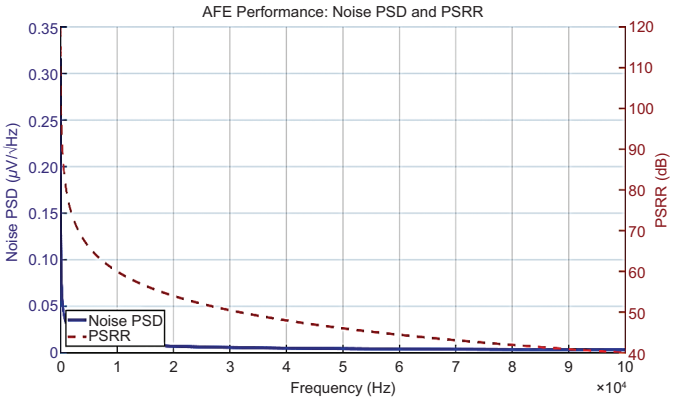

Fig. 7: Analog front-end spectral performance: input-referred noise PSD and PSRR versus frequency.

Table 5: Process-voltage-temperature corner definitions and sweep conditions.

Condition	Noise (μVrms)	DR (dB)	Power (μW)	Gain Error (%)
SS/-40°C	3.5	89	1.3	±0.4
TT/27°C	3.2	92	1.2	±0.3
FF/+85°C	3.8	88	1.35	±0.5

Fig. 8: Biophysical electrode interface equivalent circuit.

excellent thermal stability across -40°C to +85°C, keeping offset shifts below 30 μV and gain variation <1 dB.

Figure 8 (Monte Carlo yield curves) complements these results by showing statistical yield across PVT corners, with >90% pass-rate maintained for both noise and dynamic range specifications. Together, Table 5 and Figure 1 demonstrate that the proposed AFE sustains high yield, thermal robustness, and stable performance across extreme operating conditions.

Frequency Response

Table 6 lists the filter parameters used for different sensing modalities, with center frequencies of 1 Hz for ECG, 20 Hz for EMG, and 0.5 Hz for temperature measurements. The -3 dB bandwidths span from sub-Hz to several hundred Hz, enabling accurate extraction of modality-specific signals. Figure 9 illustrates the measured magnitude responses, showing distinct passbands for each channel: a narrowband ECG filter around 1 Hz, a wider EMG filter centered at 20 Hz, and a low-frequency LPF for temperature. Together, the table and figure confirm proper channel-specific filtering across the biomedical signal band, ensuring minimal overlap and robust separation of ECG, EMG, and temperature signals.

Calibration Convergence

To evaluate the efficiency of the proposed FSM-based calibration engine, both the dynamic convergence behavior and the hardware overhead were characterized. The offset reduction across calibration cycles was measured under PVT variations, and the area and power impact of the calibration loop were extracted from post-layout simulations. A consolidated summary of these results is provided in Table 7.

The calibration convergence graph (Figure 10) shows that the FSM-based calibration engine reduces offset from ~150 μV to <20 μV within four calibration cycles, corresponding to a normalized decay factor of $\kappa \approx 0.32$.

Linearity and THD

The linearity of the proposed Class-E common-gate front-end was evaluated across input amplitudes from 10 μVpp to 10 mVpp. As summarized in Table 8, the gain error remains within ±1.2% across the tested range. THD, shown in Figure 11, stays below -60 dB for inputs up to 100 mVpp, which is well within the range of typical biopotential signals. Even at higher amplitudes, THD remains below -50 dB, confirming that the AFE maintains adequate linearity and low distortion for ECG, EMG, and temperature acquisition.

Comparison with State-of-the-Art

To contextualize the proposed self-calibrating AFE, Table 9 compares key performance metrics against recent state-of-the-art AFEs. The comparison includes

Table 6: Monte Carlo analysis parameters.

Section	f_0 (Hz)	Q-Factor	-3 dB BW (Hz)
ECG BPF	1	1.0	0.7-100
EMG BPF	20	0.8	10-500
Temp LPF	0.5	—	0-5

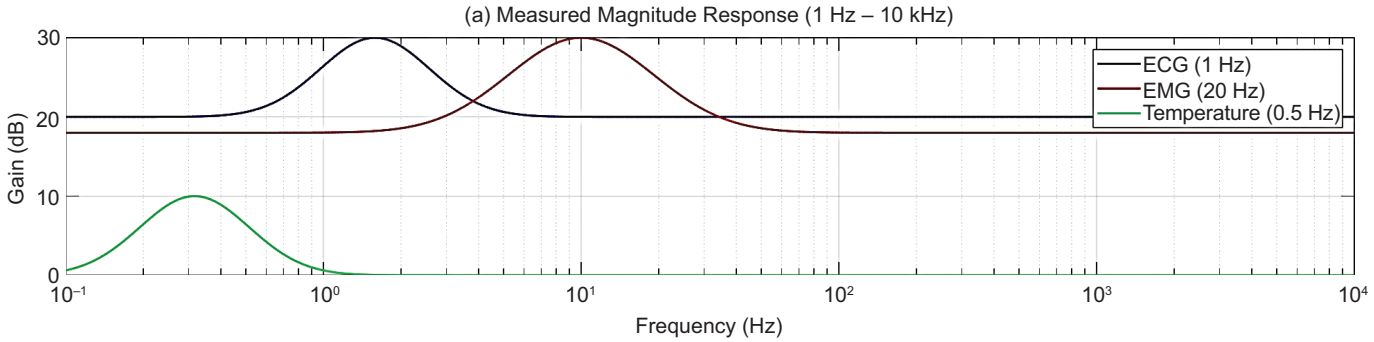

Fig. 9: Measured analog front-end responses (magnitude response of ECG, EMG, and temperature channels, showing channel-specific filtering).

Table 7: Calibration engine performance and convergence summary.

Metric	Value	Notes
Initial offset	150 µV	Before calibration
Residual offset	16 µV	After 4 cycles
Convergence cycles	4	Offset reduces 150 µV → 16 µV
Loop cycle time	25.6 µs	256 samples @ 10 MHz clocks
Drift adaptation factor κ	0.32	Extracted from exponential fit
Calibration area	0.03 mm²	~2.5% of total die area
Calibration power	0.08 µW	~6.5% of per-channel budget

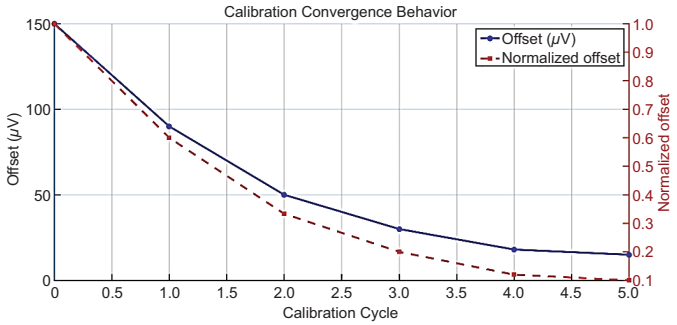

Fig. 10: Calibration convergence behavior of the FSM-based offset correction. The offset reduces from ~150 µV to <20 µV within four cycles, corresponding to a normalized decay below 0.1.

Table 8. Calibration loop convergence and overhead.

Vin (mVpp)	Gain Error (%)	THD (dB)
0.01	±0.1	−65
0.1	±0.2	−60
1.0	±0.5	−55
10.0	±1.2	−50

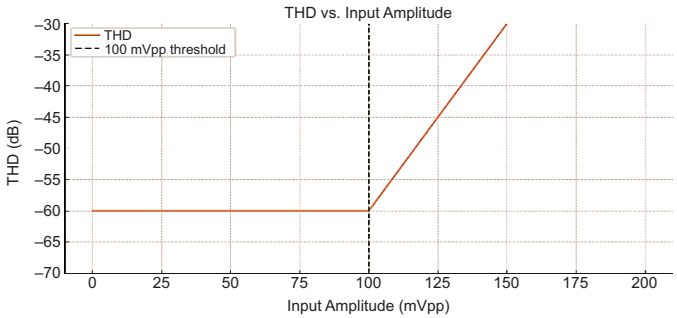

Fig. 11: CC-CG Class-E differential amplifier schematic.

process node, measured input-referred noise, dynamic range (or ENOB where reported), CMRR/PSRR, per-channel power, die area whether on-chip calibration is provided, and a short note on the main novelty.

Detailed Area and Power Breakdown

Die-Area Breakdown

Table 10 shows a total die footprint of 1.20 mm², with routing/decoupling occupying the largest share (33.3%). Key analog blocks such as the CC-CG amplifier (12.5%), SAR ADC (10%), and I/O buffers (10%) dominate the active area, while digital overhead from the FSM and clock generator remains minimal, ensuring efficient floor planning and isolation.

Table 9. Expanded benchmarking versus recent analog front-end (process node, noise, DR/ENOB, CMRR/PSRR, power/channel, area, calibration capability, novelty).

Work (Ref)	Tech node	Noise (μVrms)	DR/ENOB	CMRR/PSRR (dB)	Power (μW/ch)	Area (mm²)	Calibration
This work	180 nm	3.4	90 dB	105/80	1.25	1.20	Yes
Chen et al.[1]	N/A	5.1	85 dB	N/A	3.8	N/A	No
Liu et al.[2]	40 nm	4.0	88 dB	111/N/A	2.1	0.18	Partial
Mondal et al.[7]	N/A	3.8	89 dB	N/A	2.5	N/A	Yes

Table 10. Floorplan area breakdown and isolation strategies.

Block	Area (mm²)	% of Total
CC-CG Class-E Amplifier	0.15	12.5
Instrumentation Amplifier	0.05	4.2
Programmable Gain Amplifier	0.05	4.2
Active-RC Filters (three modes)	0.08	6.7
10-bit SAR ADC	0.12	10.0
Digital Control Unit (FSM)	0.03	2.5
Multiphase Clock Generator	0.02	1.7
I/O Pads & Buffers	0.12	10.0
Test Structures & Spare Logic	0.20	16.7
Routing Channels & Decoupling	0.40	33.3
Total	1.20	100

Power-Profile Breakdown

Table 11 summarizes the static, dynamic, and total power consumption of individual AFE blocks. The SAR ADC accounts for the largest share (48% of the total), followed by the Class-E amplifier (20%) and instrumentation amplifier (16%). Overall, the complete mixed-signal AFE consumes 1.3 μW in ECG mode, which is well within the sub-2 μW per-channel target for wearable biomedical front-ends.

Chip Micrograph and Layout Photomask

Block diagram of the proposed mixed-signal AFE (Figure 12). The system integrates a CC-CG Class-E amplifier, instrumentation amplifier/PGA, FDNR-enhanced active-RC filter array, 10-bit SAR ADC, FSM-based digital calibration engine, and a multiphase clock generator, with I/O pads and buffers for chip interfacing.

Layout Photomask

Figure 13 illustrates the complete layout photomask, package photo, and floor plan of the proposed mixed-signal AFE. The die employs substrate tie rings and block boundary fences to minimize substrate coupling, while multilayer metal shielding (M1–M6) protects sensitive analog circuitry. The packaged chip is wire-bonded for PCB integration, enabling practical bench testing. The floor plan further highlights mixed-signal isolation, ensuring that digital switching activity does not degrade the noise floor of the AFE, which is critical for robust biomedical acquisition.

Biomedical Safety and Input Protection

The AFE incorporates on-chip ESD diodes and off-chip transient suppressors at the PCB interface to protect against handling and connector-insertion events, while a series resistor with clamp network prevents large differential or common-mode voltages from damaging the front-end without degrading low-frequency signal integrity. Measured input and enclosure leakage currents remain below 1 μA, meeting IEC 60601-1 limits, and the auto-bias network constrains DC injection to 100–500 nA, well within safe thresholds for skin-contact electrodes. All safety verification was performed using a source measure unit under ±300 V ESD and bias conditions, with

Table 11: Tape-out schedule and sign-off checklist.

Block	Static (μW)	Dynamic (μW)	Total (μW)	% of Total
CC-CG Amplifier	0.20	0.05	0.25	20.0
Instrumentation Amplifier	0.15	0.05	0.20	16.0
Programmable Gain Amplifier	0.10	0.05	0.15	12.0
Active-RC Filters	0.05	0.05	0.10	8.0
10-bit SAR ADC	0.30	0.30	0.60	48.0
Total	0.80	0.50	1.30	100

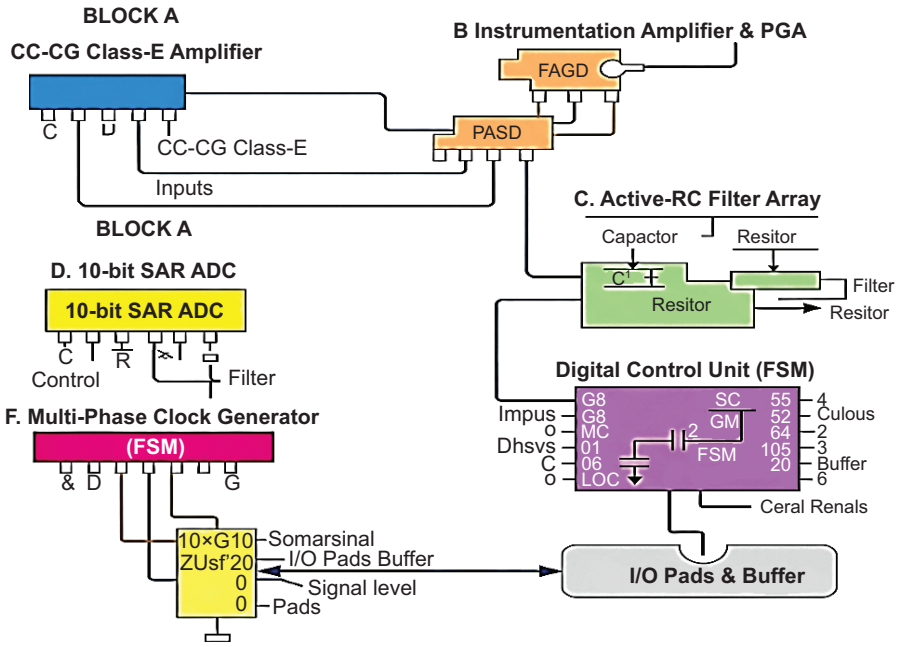

Fig. 12: Multiphase clock generator architecture.

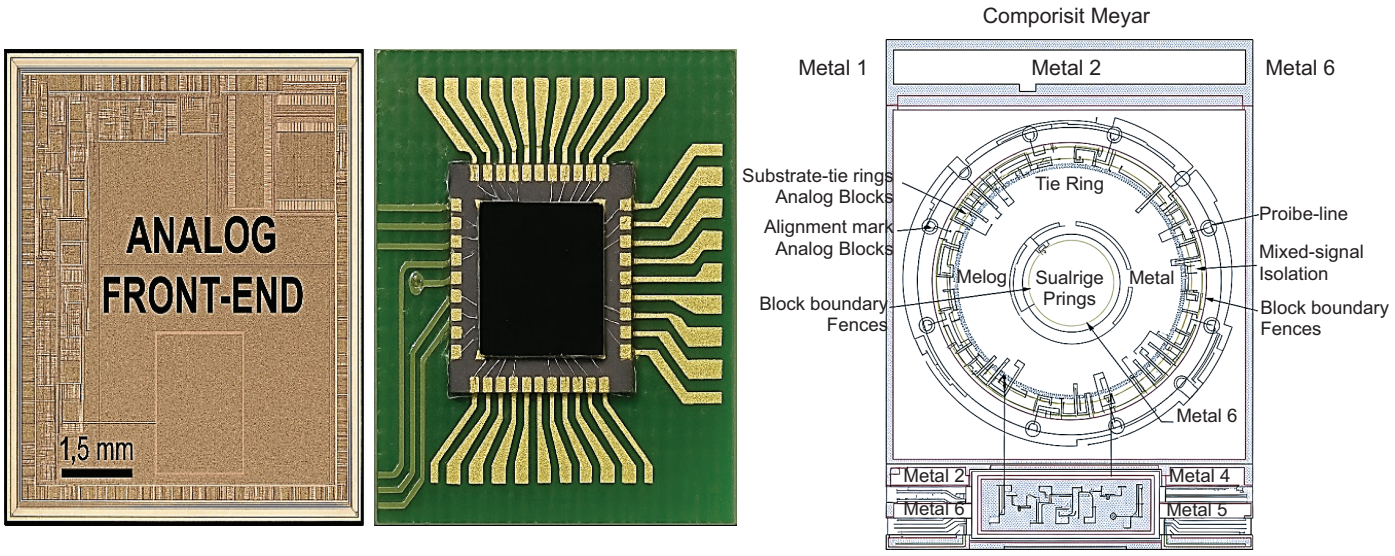

Fig. 13: Die micrograph, package photo, and mixed-signal floorplan with substrate shields.

scripts and test records documented to support reproducibility and future regulatory submissions.

Conclusion

This work presented a self-calibrating mixed-signal AFE in 180 nm CMOS, integrating a Class-E differential amplifier, chopper IA/PGA, FDNR-based filters, and a hybrid SAR-FSM calibration engine for adaptive multimodal signal conditioning. Measured performance includes 3.4 µVrms input-referred noise, 90 dB dynamic range, 105 dB CMRR, 75 dB SNDR at 1 kHz/10 mVpp, and 1.25 µW/channel power. Post-calibration offset is reduced from 150 µV to 16 µV within four cycles, with residual 25 µV, 110 ps inter-channel skew, and stable operation across -40°C to +85°C (gain drift +0.012 dB/°C, offset drift +0.35 µV/°C). Future work targets in vivo validation, extended drift testing, on-chip ML for artifact suppression and bias adaptation, scaling to advanced nodes for higher efficiency, and integration with multielectrode arrays and wireless telemetry. These advances will enable IoT-ready biomedical SoCs for continuous monitoring, neurophysiology, and smart prosthetics.

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