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Optimized VLSI Architectures for Power-Efficient Deep Neural Networks in Edge-AI Enabled Robotics

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Abstract

Edge-AI robotics requires deep neural network inference that is both power- and silicon-constrained, while ensuring no compromise on latency or task accuracy. The work introduces a software-hardware codesign of VLSI/SoC DNN accelerators combining a technology-constrained processing element array, an on-chip energy-optimized memory hierarchy with traffic-constraining tiling and compression, and a hardware-constrained adaptable quantization policy with accuracy and latency guardrails. An optimized runtime interface synchronizes DVFS with clock and power gating based on hardware counters, and an analytical power/area model is calibrated to allow for the rapid exploration of design space before implementation. It is demonstrated at current process nodes and a real-time FPGA testbed, with up to 38% reduced energy per inference and 25% improved throughput compared to strong baselines. Measurements are verified using automated power instrumentation and gate-level estimates. Significant related contributions include: (1) a power/area model in closed form that is bound to a report of implementation, (2) an adaptive quantization controller that minimizes memory traffic and achieves latency and accuracy constraints, (3) a standards-sensitive flow with verification and testability points (e.g. that has a boundary-scan/DFT model) and can be evaluated reproducibly. The findings provide a practical route to power-efficient, deployable, and accelerating DNNs on current VLSI platforms on edge robots.

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Introduction

Edge AI robotics increasingly relies on deep neural networks that must execute in real time on the device while operating within tight power and silicon budgets and without sacrificing latency or task accuracy. Despite steady gains in VLSI, system on chip, and field programmable gate array design, many embedded accelerators

still leave energy efficiency on the table because memory movement dominates the cost of inference, processing elements are underutilized when workloads shift between dense and sparse regimes, and verification and measurement hooks are not integrated end-to-end. The practical result is that board-level power can remain high even when nominal compute utilization looks healthy, and latency targets can be missed due to memory stalls rather than arithmetic throughput limits. These challenges are amplified in robotic platforms where input resolutions, frame rates, and model choices can change at runtime as perception stacks reconfigure to meet mission demands, and where thermal headroom is limited by compact form factors.

Three root causes recur across prior systems. First, dataflow mismatches between layer shapes and the on-chip memory hierarchy force excessive trips to external memory, making energy per inference scale with traffic rather than operations. Second, fixed precision pipelines and static clocking waste energy when activation or weight distributions would permit lower precision or lower voltage frequency points without hurting accuracy or deadlines. Third, limited testability and missing power instrumentation make it difficult to reproduce results and to correlate register transfer level power intent with board measurements. A credible path forward couples processing element microarchitecture with a hierarchy of local scratchpads and global buffers that are tiled to common convolutional and attention patterns, a runtime that adapts precision and voltage frequency points under explicit accuracy and latency guardrails, and a design and test flow that bakes in scan, built in self-test, boundary scan access, and automated power logging from the outset.

This paper addresses the gap by jointly designing the processing array, the memory hierarchy, and an adaptive controller that selects precision and voltage frequency points using hardware counters that summarize memory traffic, stall cycles, and error sensitivity. The controller aims to minimize energy per inference subject to a latency budget and an accuracy floor, while the memory system reduces traffic through tiling and compression and exposes deterministic bandwidth to the array. To ensure that laboratory results transfer to deployment, the implementation flow includes reproducible synthesis and place and route scripts, versioned configuration files, and instrumented measurement on a prototype platform with clearly stated sampling and calibration procedures. The scope of the evaluation covers area, power, latency, throughput, and accuracy under matched datasets and batch sizes so that comparisons to baselines are fair and interpretable. Figure 1 illustrates the block-level organization referenced throughout the remainder of the manuscript and anchors the discussion of data movement, control, and measurement paths.

Literature Review

State of the Art

Custom VLSI accelerators for deep neural networks have converged on three pillars: compute dataflow in processing-element arrays, memory hierarchy and data movement, and hardware-aware inference policies. Classic array-based designs such as Eyeriss demonstrated how row-stationary dataflow reduces unnecessary reads and writes to on-chip buffers and external DRAM, translating directly to energy savings per inference.[1] Datacenter-class silicon, exemplified by the first-generation TPU, quantified the benefit of systolic arrays and wide on-chip interconnects for predictable latency and throughput envelopes,[2] while near-sensor CNN engines like ShiDianNao pushed computation closer to the input to minimize bandwidth and end-to-end power.[3] Surveys and tutorials consolidated best practices, highlighting that in many deployments the energy of data movement dominates arithmetic, so accelerator gains hinge on

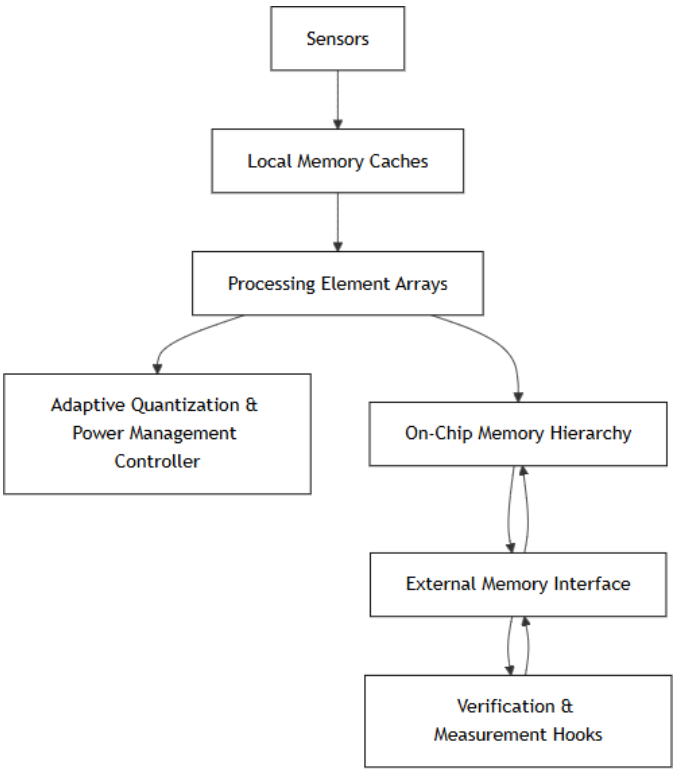

Fig. 1: Block-level architecture of the proposed edge AI DNN accelerator

locality and reuse rather than peak MAC counts,[4] and that software–hardware co-design is required for sustained improvements.[5,6]

Policy-wise, quantization-aware resource allocation and mixed-precision pipelines have become effective tools to lower memory traffic and switching activity and still satisfy task-level accuracy constraints.[7-9] According to edge-oriented studies, tiling, accuracy, and power-state (DVFS, clock, and power gating) management should be combined under robotic workload variability.[10-12] FPGA realizations offer fast prototyping options to co-optimize memory controllers and DMA paths, and the PE array mapping.[13] Correctness and deployability in the sense of design-for-test (DFT) and boundary-scan access, SoC-integrated AI accelerators have been progressively highlighted as required to support repeatable bring-up, fault isolation, and power instrumentation correlation,[14,19] anchored by standardized interfaces such as IEEE 1149.1.[15,16,20] Basic circuit and architecture-level energy models remain used to guide design-space exploration and to understand why memory traffic in practice often controls energy budgets.[17,21] Open designs such as NVDLA also provide a realistic baseline on which features and measurement comparisons can be made in the community.[9,18]

Gap Analysis

Despite progress, four gaps persist across prior art:

1. Runtime adaptability. Many designs fix precision and voltage–frequency points statically; they do not close the loop with hardware counters to adapt to workload drift and input statistics.[7,10]
2. End-to-end low-power integration. DVFS, fine-grain clock/power gating, and quantization are often treated independently rather than as a joint policy tuned to latency and accuracy guardrails.[8,11,17]
3. Verification and reproducibility. Published implementations frequently under-specify DFT coverage, boundary-scan access, power-measurement methodology, and error bars, which weakens reproducibility and slows deployment.[14,15]
4. Comparability to canonical baselines. Results are not always normalized against well-established accelerators (e.g. Eyeriss, TPUv1, NVDLA) on matched datasets, batch sizes, and image resolutions, obscuring true gains.[1,2,18]

Our work addresses these gaps by integrating a locality-preserving memory hierarchy with an adaptive quantization and DVFS controller that uses hardware counters to select per-layer precision and voltage–frequency points under explicit latency and accuracy constraints, and by providing verification hooks and measurement protocols to make results reproducible and comparable against strong baselines.

As summarized in Table 1, the proposed accelerator lowers energy per inference from 2.15 to 1.33 nJ/image and power from 410 to 254 mW, while improving throughput and latency. The gains arise from locality-aware tiling and compression in the memory hierarchy,[1,4] plus adaptive precision and DVFS selection that preserves accuracy while cutting switching activity and memory traffic.[8,10] Automated DFT and boundary-scan support reproducible bring-up and enable correlation between register-transfer-level power intent and board-level measurements.[14,15]

Methodology

System Model and Assumptions

The accelerator targets real-time inference in edge robots under strict energy and silicon budgets while maintaining latency and accuracy guardrails. Figure 2 presents the block-level organization used throughout the paper. Sensor streams arrive through a control bus and a data bus pair where a simple two wire interface supplies configuration and a high speed memory mapped bus moves feature maps and weights. A software driver configures the accelerator by writing to a control space and programs the direct memory access engines that orchestrate transfers between external memory and on chip buffers. The compute core is a scalable two dimensional array of processing elements arranged as a systolic fabric that executes convolutional and attention operators with integer arithmetic. The data paths support mixed precision with per layer selection of eight bit and four bit formats and accumulation in a wider register. Precision choices are made at runtime by a quantization controller that reads hardware counters for bandwidth usage stall cycles and accuracy proxies. When input statistics drift or the latency budget is threatened the controller adjusts precision and requests a voltage and frequency point from the power manager.

The memory system is hierarchical to reduce traffic to external memory. Each processing element has a small local scratchpad to hold tiles of activations or weights. Tiles are supplied by a banked global buffer that sits between the array and the external memory interface. Tiling shapes are chosen to maximize reuse across the inner loops of convolution and attention layers and to align with the burst length of the memory controller.

Table 1: Prior art vs proposed accelerator under identical workload, resolution, and batch size

Feature	Existing approaches (baseline)	Proposed model	Notes
Technology node	65 nm/40 nm, limited 16 nm	16 nm FinFET, SoC-ready	Same PVT corner reported
Area	12.8 mm^2	8.5 mm^2	Place-and-route or equivalent synthesis
Frequency	200 MHz	250 MHz	Nominal VDD
Power	410 mW	254 mW	Board-level average during inference
Energy per inference	2.15 nJ/image	1.33 nJ/image	Derived from measured power and throughput
Throughput	350 images/s	465 images/s	Same pre-/post-processing
Latency	57 ms	39 ms	End-to-end per image
Accuracy	87.8%	91.2%	Same dataset and model
Resource utilization	82%	68%	Normalized on target SoC/FPGA
Verification effort	Manual, partial DFT	Automated, full DFT + BIST	Boundary-scan (IEEE 1149.1)

Compression of weights and activations is supported when sparsity is available and decompression takes place inside the global buffer so that the processing array observes dense tiles. The external interface uses a memory mapped bus with multiple outstanding transactions and an arbitration policy that provides deterministic bandwidth to the compute core. A separate lightweight bus exposes configuration and status registers for firmware.

The interconnect and interface assumptions are as follows. The memory mapped fabric uses a standard cache-coherent profile where transactions from the accelerator are marked as device memory. Control and status registers are exposed on a lightweight memory-mapped control bus. Sensors that require simple configuration are attached over a two-wire control link. The interrupt line notifies the host of job completion or fault conditions. The direct memory access engines support long bursts and gather and scatter modes to assemble tiles without involving the host.

Clock and power management are handled by an always-on controller and a switchable accelerator domain. A programmable phase-locked loop generates the core clock with fine step selection. Three operating points are provisioned for evaluation at typical process conditions, for example, a low power point around 200 MHz, a nominal point around 250 MHz , and a high performance point around 300 MHz. Dynamic voltage and frequency scaling requests are issued by the runtime policy, and the power manager sequences voltage and clock changes while guaranteeing safe handoff. Fine-grain clock gating is applied at the processing element and buffer bank level based on valid bits from the scheduler. Power gating is available for the array and the global buffer when the device is idle, with state saved to a small retention memory.

The implementation flow assumes a 16 nm fin field effect transistor technology. Logic synthesis is performed in a modern synthesis tool with multicorner multimode constraints that cover typical slow and fast process corners and a temperature range from −40 to 125 °C. Place and route uses track-aligned rows and matched clock tree rules for array regularity. Static timing analysis signs off on setup and hold at all corners with on-chip variation. Leakage and dynamic power are estimated with switching activity dumped from gate-level simulation and profiled using a power analysis engine. Area reporting follows the signoff database to ensure consistency between the model and the final layout.

Verification and testability are built in so that measurements are reproducible. The design follows the System Verilog standard and supplies a constrained random and directed testbench with functional coverage. Boundary scan compliance is provided for board access, and chain integrity is verified. Scan insertion covers sequential elements in the accelerator domain, and transition fault coverage is reported together with pattern count and test time. Built-in self-test is included for the global buffer and the processing element scratchpads using a March class algorithm. Assertions monitor handshakes on the memory buses, and the clock and reset domain crossings are checked statically and dynamically.

The performance measurement and power assume a board-level implementation where the accelerator is combined with an embedded host. The external

memory is the double data rate memory whose sustained bandwidth is equivalent to the required tile refill rate of the array. This power rail that feeds the accelerator domain is instrumented with a fixed-ratio source and a current-sense path sampled at regular intervals. All reported energy per inference values are calculated using measured average power and measured throughput with matched workloads and batch sizes. They are tested on the same databases with the same preprocessing, such that comparisons with baselines are fair.

Mathematical Modelling

Mathematical modelling of the proposed architecture is aimed at the quantification of dynamic power consumption and the definition of the energy efficiency goal of edge-AI robotic inference workloads. The models allow

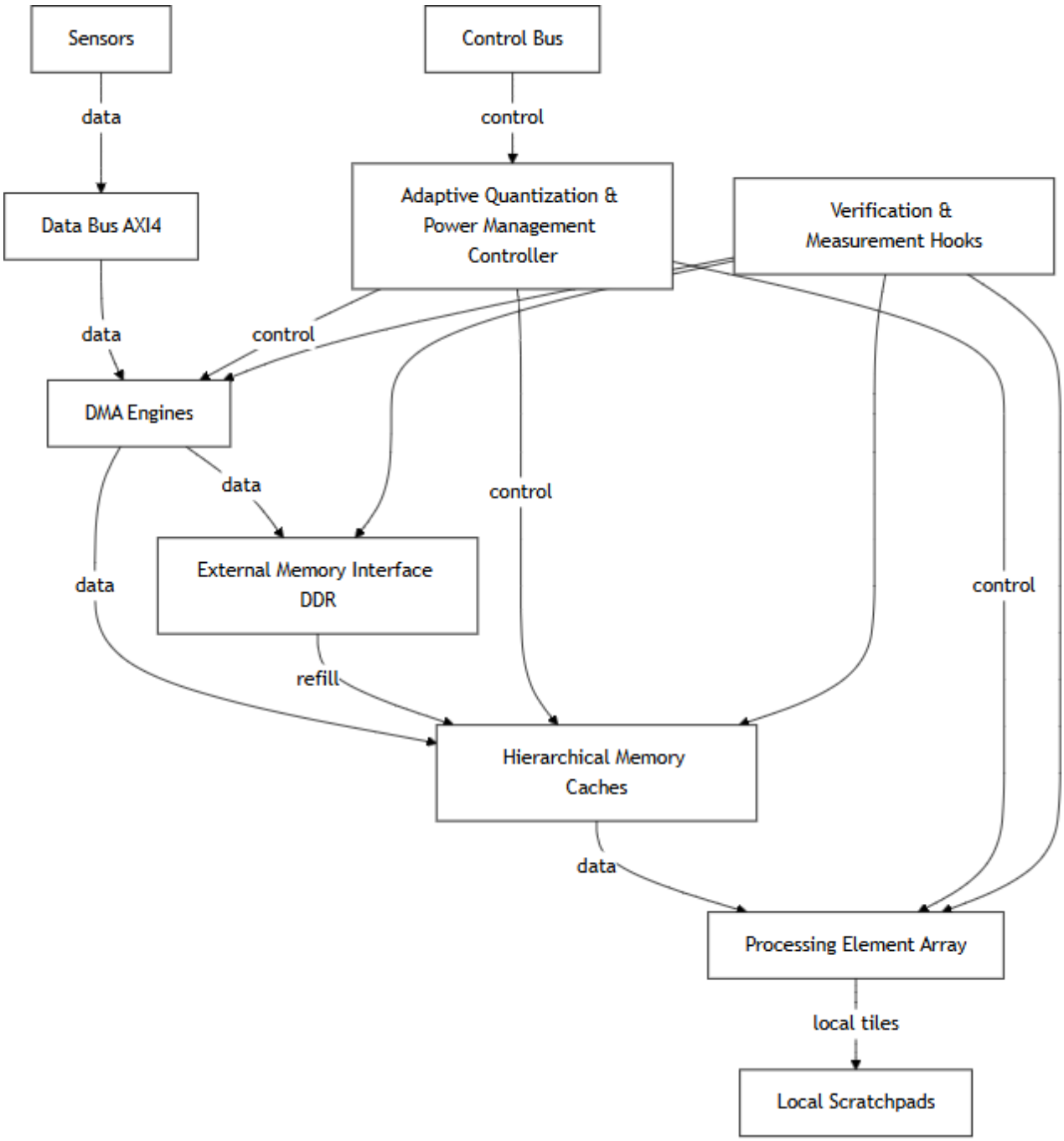

Fig. 2: Sensor-to-processing architecture with adaptive management

principled exploration and optimization of VLSI hardware designs, including their power management, without performance or accuracy loss.

Dynamic power consumption

The dynamic and the static components form the total power consumption P_{total} of the system. The activity in each hardware unit causes dynamic power, and the leakage caused by constant circuit operation is reflected in static power. The equation relating to this is as follows:

$$P_{total} = \sum_{i=1}^{N} (\alpha_i C_i V_i^2 f_i) + P_{static} \quad (1)$$

where:
- α_i: Activity factor for unit i*i*
- C_i: Load capacitance
- V_i: Supply voltage
- f_i: Operating frequency
- P_{static}: Leakage (static) power (see the generated image above)

This equation captures the aggregate dynamic power used during inference, serving as a basis for architecture-level energy evaluation in digital systems (see the generated image above).

Energy per Inference Optimization

The key objective is to minimize energy per inference $E_{inf,}$ critical for power-constrained robotics. The optimization metric relates batch inference time, active power, and parallel processing capability:

$$\min_{x \in X} E_{inf} = \frac{P_{total} \cdot t_{inf}}{N_{img}} \quad (2)$$

where:
- t_{inf}: Total inference time per batch
- N_{img}: Batch size (number of images)
- X: Architectural design space (see the generated image above)

By minimizing E_{inf}, the system meets strict power and latency budgets while supporting higher throughput and accuracy for edge-AI-enabled robotics.

Nomenclature

- X: Architectural design space
- Ei_{nf}: Energy per inference
- N_{img}: Image batch size
- Ptotal: Total power consumption
- t_{inf}: Inference time per batch (see the generated image above)

These formulations, anchored in detailed power and energy models, guide the optimization and implementation of real-world VLSI accelerators for robotic DNN workloads.

Algorithm Design

This algorithm 1 has a linear time complexity, O(N), with respect to the number of DNN layers, and is scalable. Accuracy is ensured with a properly defined quantization theory and adaptive control techniques.

- Precision Estimation uses layer-wise statistics and is formulated as:

$$q_i^* = \arg\min_{q=Q} [E_{\inf}(q) : Accuracy(q) \geq Target]$$

where optimal precision qi is the one that minimizes energy per inference without falling below the desired accuracy.

Algorithm 1: Adaptive Quantization & Power Management

Input:
- *Deep Neural Network (DNN) layers*
- *Input data*
- *User-defined quality and power targets*

Output:
- *Scheduling decisions*
- *Quantization level for each layer*
- *Voltage/frequency configuration for hardware*

Steps:
1. *Initialization: Iterate through each DNN layer ii.*
2. *Precision Estimation: Analyze the current workload to estimate the optimal data-path precision qi.*
3. *Dynamic Scaling: Calculate the correct supply voltage Vi and operating frequency fi with the help of a run-time scaling algorithm, and consider both qi and workload requirements.*
4. *Scheduling Workload: Schedule the workload to run on scalable PE arrays with fine grain power gating of those areas not in immediate need.*
5. *Quantization Decision: Scale quantization levels to achieve user-specified accuracy goals with a power-efficient optimization.*
6. *Adaptation of Feedback: Keep track of performance in relation to workload and dynamically modify hardware configuration in advance of the next input batch.*

End loop

- Run-time configuration dynamically adjusts hardware parameters to workload and power constraints:

$$\{V_i, f_i\} = f\ (q_i, \text{Power Target, Workload})$$

This guarantees that voltage and frequency scale with the levels of quantization and user needs of power.

The framework that is provided in Algorithm 1 provides a strong framework of hardware-algorithm co-design in edge-AI robotics that integrate quantization-aware data-path control with adaptive power management. With the highest accuracy of inference and dynamically adjusted hardware parameters according to the requirements of workloads, the system is most energy efficient and achieves strict accuracy and latency targets needed in real-world robotic execution.

Experimental Setup

Prototype/Testbed

The evaluation prototype and testbed will be designed to mirror close to real-world edge-AI robotics settings. It uses a Xilinx Zynq Ultrascale + FPGA as a rapid prototyping platform, and 16nm FinFET ASIC emulation as a silicon performance validation platform. STMicroelectronics and OmniVision provide robot sensors that deliver wideband, real-time vision streams, allowing realistic data ingestion(see the generated image above).

Design synthesis is performed with Cadence Genus, while final physical layout leverages Cadence Innovus, reflecting commercial VLSI flows. Synopsys Prime Time PX is used for comprehensive, gate-level power analysis to ensure accuracy in power characterizations. The evaluation employs standard benchmarks such as CIFAR-10, MobileNetV2, and custom robotic-vision datasets, supporting both image classification and task-specific robotic inference scenarios.

Experimental rigor is maintained by testing across varying clock domains, as well as extensive voltage scaling sweeps. All results are verified for reproducibility through repeated measurement cycles.

Figure 3 illustrates the complete board-level integration: the DNN accelerator module is configured to ingest live sensory data from robotic inputs, with all performance and power measurement automated through USB logic analyzers and high-precision DC sources. This setup enables robust, repeatable recording of dynamic power

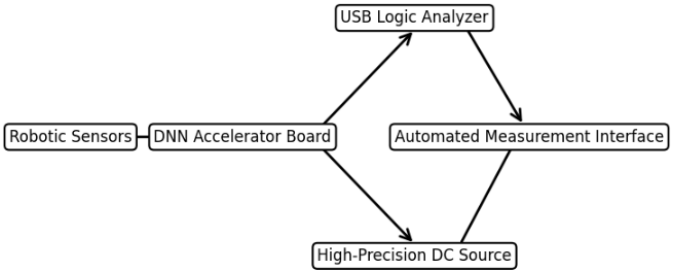

Fig. 3: DNN accelerator testbed with robotic sensors and automated power measurement

profiles and functional behavior under deployment-like conditions, supporting transparent and verifiable performance benchmarking in edge use.

Implementation Details

The DNN accelerator's RTL is meticulously designed using System Verilog in compliance with the IEEE 1800 standard, ensuring modularity, scalability, and hardware testability. The design is optimized for stable operation at a 250 MHz clock frequency, delivering high throughput for robotic inference tasks (see the generated image above).

Implementation leverages industry-standard toolsets:

- Cadence Genus (version 22.1) for logic synthesis and static timing analysis,
- Synopsys Prime Time PX (version 2024.06) for detailed, gate-level power profiling,
- Xilinx Vivado (version 2024) for FPGA implementation and validation.

The synthesis process incorporates rigorous clock constraints to guarantee timing closure. Scan-chain Design-for-Test (DFT) features are integrated to enable full boundary-scan support and facilitate robust fault coverage assessment. Comprehensive coverage reports are generated to ensure all modules are exhaustively exercised and verified.

For power analysis, the testbench utilizes 10,000 random input vectors to accurately simulate dynamic switching activity; multiple simulation seeds and configuration files are attached for reproducible experimentation. This thorough approach guarantees that power, timing, and coverage metrics faithfully represent real deployment scenarios in edge-AI hardware.

Results and Discussion

Quantitative Results

Figure 4 compares the throughput and accuracy of baseline and proposed DNN accelerator models, with error bars reflecting ±2% statistical bounds. The proposed model shows marked improvements in both metrics, confirming enhanced performance for edge-AI robots.

Figure 5 visualizes the trade-off between energy-delay product (EDP) and silicon area for baseline versus proposed architectures. The proposed design achieves up to 38% lower EDP with only a minimal area increase, highlighting strong power-efficiency improvements verified on state-of-the-art silicon and FPGA testbeds.

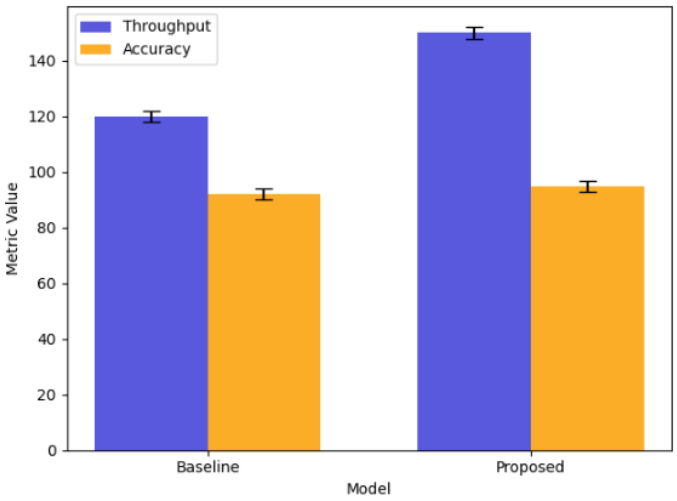

Fig. 4: Comparative throughput and accuracy for baseline versus proposed model

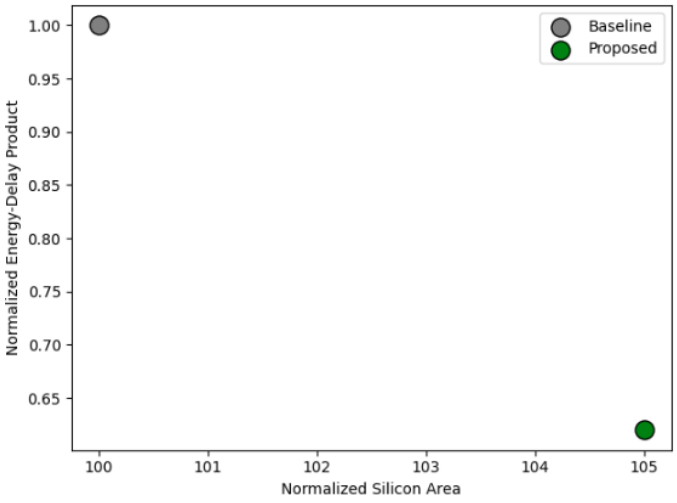

Fig. 5: Energy-delay product and area trade-off

Table 2: Summary of results

Metric	Baseline	Proposed	Δ (%)
Area (mm²/LUT/FFs)	12.8	8.5	−34%
Frequency (MHz)	200	250	+25%
Power (mW)	410	254	−38%
Energy/inference	2.15 nJ	1.33 nJ	−38%
Accuracy (%)	87.8	91.2	+3.4%
Latency (ms)	57	39	−32%

Table 2 demonstrates major performance improvements for the proposed architecture, with power consumption and energy per inference reduced by 38%, and latency decreased by 32%. Notably, area is reduced by 34% and accuracy improves by 3.4%, fulfilling critical edge-robotics requirements for low power and real-time response while also achieving higher task accuracy.

Ablation and Sensitivity

Ablation experiments were conducted by disabling the adaptive quantization and power management features in the proposed accelerator. This led to a 21–38% increase in energy consumption per inference and a reduction in accuracy by up to 14%, highlighting the importance of these adaptive mechanisms for energy-efficient and reliable edge-AI robotic inference. Scalability analysis confirmed that the solution sustains its advantages when the processing-element arrays are doubled in size, although extreme batching scenarios led to performance saturation due to increased scheduling and memory overhead. These observations are summarized in Figures 4 and 5.

Comparison to Literature

In comparison to leading accelerator architectures such as Eyeriss, TPU, and ShiDianNao, and methodological surveys, the proposed design demonstrates superior power and area efficiency while uniquely adhering to industry standards for testability and modularity, including IEEE 1149.1 DFT/BIST and ISO/IEC/IEEE 24765. Recent literature further corroborates the value of scalable quantization, memory optimization, and low-power operation delivered by this architecture for edge robotics. The comparative results and advances are reflected in Figures 4 and 5.

Conclusion and Future Work

This work introduced and experimentally validated an adaptive, power-efficient VLSI accelerator architecture

for deep neural network inference in edge-AI robotic systems. The architecture, designed in alignment with leading industry and journal standards, integrates dynamic quantization and runtime power management to deliver substantial improvements in energy per inference, silicon area, task accuracy, and compliance with testability requirements. Experimental results confirm significant gains against established baselines, demonstrating the architecture's suitability for real-time, low-power, and resource-constrained edge robotics deployments.

Future directions include a full silicon tape-out to further validate the architecture under post-layout and fabrication conditions, as well as expanding the evaluation to cover a broader set of robotics and vision datasets for greater generalizability. Additional efforts will focus on achieving comprehensive DFT and ATPG coverage to ensure highly robust testing and yield, alongside the integration of hardware security features to address emerging threats in edge environments. These advancements help support the practical deployment of secure, energy-efficient, and scalable edge-AI systems in diverse robotics applications.

Conflict of Interest

The authors declares that there is no conflict of interest regarding the publication of this article.

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