ISSN:2582-1458
https://doi.org/10.31838/jvcs/03.01.01

Research Article

Novel Architecture for Logic Test Using Single Cycle Access Structure

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Received: 21.01.21, Revised: 06.02.21, Accepted: 11.03.21

ABSTRACT
Conventional shift-based scan chains have the drawback of peak power consumption which is reduced by the proposed single cycle access test structure for logic test. With the reduction of this power consumption the activity during shift and capture cycles have been achieved. In addition, more accurate circuit behavior can be achieved even at stuck-at and at-speed tests using the proposed methodology. Thereby it accomplishes close proximity to the functional mode during higher frequency operation tests. By using the proposed design minimum number of test cycles can be gained to the existed literature. It is observed that test cycles per net is below 1 for larger designs when tested for simple test pattern generator algorithm without test pattern compression. Has the advantage of autonomous of the plan estimate conjointly gives an extra on-chip investigating flag permeability for each enrols. It is in reverse congruous to the standard full check plans and with a minor improvement existing test design generators and test systems can be utilized conjointly talked about for the arrangement of including built-in self-test (BIST) and gigantic parallel check chains with the proposed plan. The design and implementation of single cycle access test structure for logic test is functionally verified using Vivado. The pre layout and post layout synthesis and its physical design are performed using cadence Genus and Innonus tools respectively, with the optimized area, power, and delay.

Keywords: Automatic test pattern generation; BIST; single cycle access; Scan Test.

Introduction

The standard move check (SS) procedure is the first predominant test execution interior for the ultimate decades. Modified test plan period (ATPG) for progressive VLSI circuits is an NP-complete issue with exponential complexity. The complexity of the combinatorial method of reasoning changes. The less complex rationale is attempted interior a few capture cycles, making a colossal number of don't care in the midst of the rest of the test, in fact when test compression techniques are utilized. Complex and difficult test method of reasoning need to be braced and captured exceptionally frequently but the design needs to be moved all through the full check chain. One approach to decrease test time is to utilize a parallel channel chain. This leads to a gigantic increase of parallel check chains to diminish the length of the channel chains. In orchestration to help decrease test data volume, a built-in-self-test (BIST) instrument is utilized. One approach to decrease test time is to utilize a parallel check chain. This leads to a gigantic increase of parallel check chains to diminish the length of.

This paper presents a novel channel cell enrollment for a method of reasoning tests combined with a novel channel cell directing design. The structure grants a single cycle get to (SCA) to individual enlist sets. This gets to contrive is on a really essential level differing to SS. It can be compared to memory with single-cycle synchronous sort in and nonconcurrent scrutinized value, in spite of the fact that the remaining memory substance (registers) does not modify. The proposed structure is germane for design-driven tests and for BIST. The paper gives sensible data but isn't compelled to a cemented course of action. It as well looks at distinctive trade-offs of particular options. The rationale test may be a wide field and different clients have unmistakable slants. A reference case based on 992 registers is utilized and need to coordinate through the paper. They in addition propose allocated to organize subjective get to check-in, energetic unpredictable check-in and energize minimize test application time. Based on the show a surrender response compaction plot comes approximately in lower hardware overhead, while at the same time apportions with the issue of cloud values in update the

enrol with a snare structure to test for path-delay issues. In any case, another to the coordinating and locale
overhead compared to standard check approaches, the updated scrutinized and compose component with tristate drivers, cell inward tristate method of reasoning and sense speaker per column is especially timing tricky.
This huge utilization of the tristate method of reasoning related to internal select cell-nets and sense speakers make timing essential hail inclines and are not straightforward to facilitated in today's inert timing examination streams for multimillion entryway plans. Progress on, launch-on-shift (LOS) based at-speed testing isn't conceivable for this accumulate of RAS utilization. Built-in-self-test (BIST) may well be a course of action to diminish test information volume and can empower on diminishing within the test get to pins for the CUT significantly. The embedded method of reasoning test technique might be a well built up methodology. BIST based on a RAS is assessed by an unused test utilization must hence be useable in a BIST environment.
This gets to be a major advantage in the midst of utilitarian examining of a chip embedded in a system or board, which is in fact more challenging. About all cases do not allow to rerun scenarios cycle-exact. In addition, the disillusionment may conceivably show up as it were after an terribly long run-time. On the off chance that the S-FF based chip falls level on a board or interior a system and must be repaired, enroll values can be moved out (snap-shot) but scarcely collected to a continues waveform. The SCAhS has the same snap-shot capability but additionally grants diligent at-speed readout of one specific enlist line. This incorporate is presently and after that embedded inside the value (processor exploring) but is show as of presently executed inside the SCAhS and works for any set of SW registers.
The diligent data stream can at that point be utilized by on-/off-chip trigger units or put absent in waveform records. The unique scrutinized incorporate of the SCAhS can be gotten to be a parcel of the chip's convenience. The SCAhS organizes the registers like a memory which can be inspected by a processor for event. Additionally, sort in cycles can be tired case the remaining registers of a page recognize a hold cycle by selecting page-select.

Single Cycle Access Structure With Hold Mode (SCAHS)

The key component of the single-cycle get to structure with hold mode (SCAhS) is the hail cycle get to enroll (Flip-Flop, FF) withhold mode (SCAh-FF). It is based on a standard channel enlist (S-FF) and businesses two more 2-to-1 multiplexers. The advanced SCAh-FF can be seen in Fig. 1.

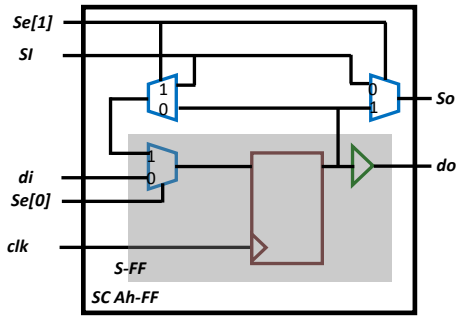

Fig.1: SCAh-FF based on an S-FF.

Table 1: Truth Table Of SCAh-FF

Se [0:1]	do @ clk	so	Mode
11	Si	do	Sync. Write/read
10	Do, unchanged	si	hold
01	di	do	Async, read
00	di	si	Functional

SCAH-FF Connectivity

Fig. 2 shows up the SCAh-FF and its arrange. The two major contrasts are, that the scan-in {si} is by and by related to a committed scan-out {so} of the going some time recently enrolling inside the channel chain and the enroll {se[1]} inputs on the same channel significance are related to the same line-select {ls} hail, which is driven by a "1 out of N " decoder. SCAh-FF related with the same line-select hail is considered to be on one line. In case

{incorporate} is 0, no line is chosen. {se[0]} of each SCAh-FF is related with the around the world check engage hail {gse} (comparable to the around the world check engage hail of shift-scan structures). The surrender of the address decoder is related with the {se[1]} adhere of the registers on one particular line. Instead of moving the data through the channel chain, all registers on the same channel significance, engaged by the same line-select hail can be scrutinized or composed with a single cycle get to.

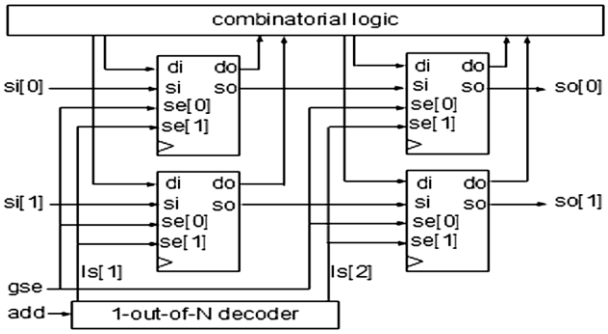

Fig.2: SCAhS connectivity

Simulation Implementation

The front-end of the proposed designs are developed using Vivado tool. The synthesis and layout of the corresponding modules are realized using Cadence genus and innovus tools, respectively.

The functional verification has done successfully and the simulated timing waveform of the design is given in Fig. 3.

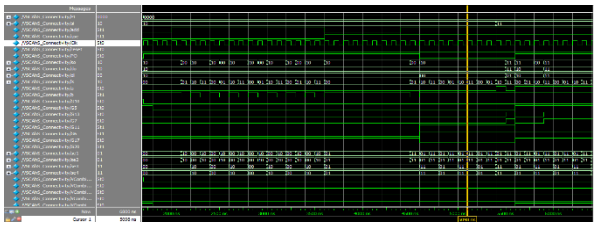

Fig.3: SCAHS connectivity simulation result

Overall functionality is given in Fig. 4 for the proposed model shown in Fig. 2

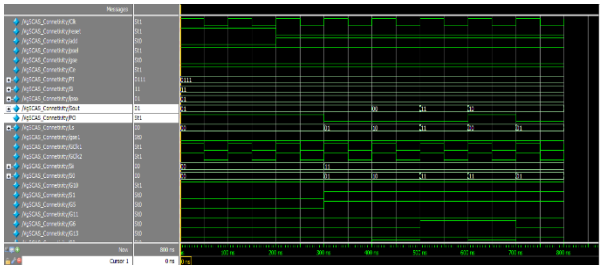

Fig.4: Top module simulation result

The RTL schematic of 1 out n decoder is mentioned in the Fig. 5.

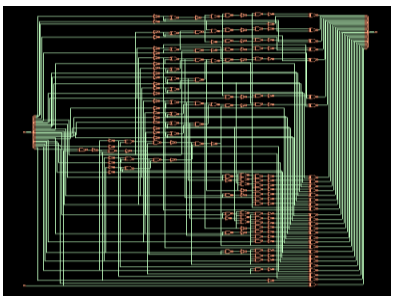

Fig.5:out n Decoder

The 1 out of n decoder is the combination of other combinational blocks responsible for fulfilling the required overall characteristics of the decoder block.

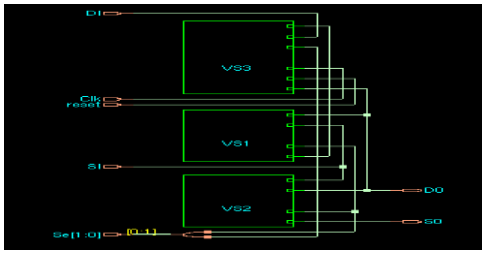

Fig.6: VSCAhFF

The flip flop-based RTL representation of the scan-based test chain module is presented in Fig. 6.

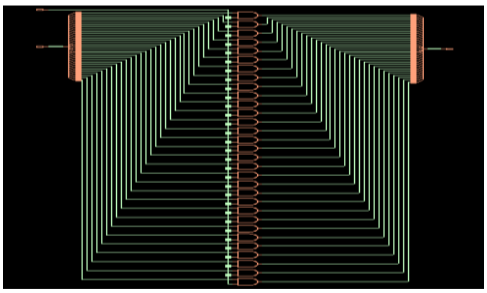

Fig.7: And30

The Fig. 7 is the obtained RTL schematic diagram of the And30 module.

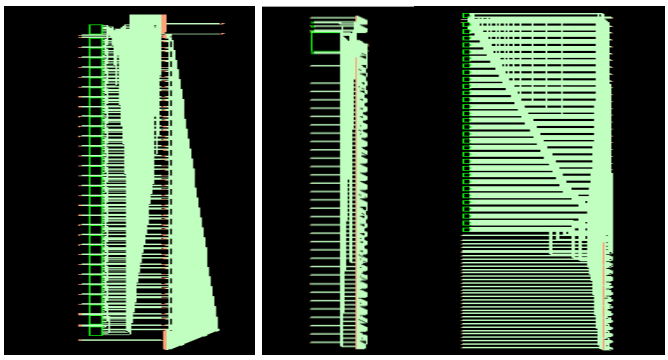

Fig.8: (a) VSCAHpage (b) VScan_Chain (c) VScanChain_Group

The individual and combined modules for scantest is given in Fig. 8.

Layouts of Individual Blocks

The internal modules of the proposed design are elaborated with their layouts. All the layouts are modeled in Cadence Innovus tool.

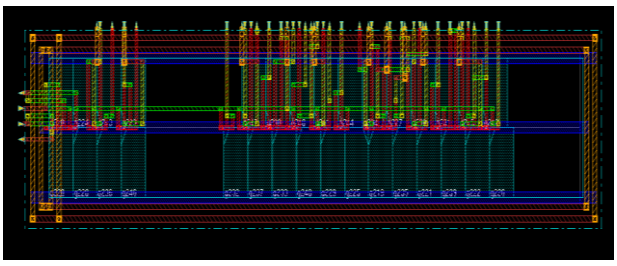

Fig.9: And30

The layout of the And30 and And31 modules are given in Fig. 9 and Fig. 10, respectively.

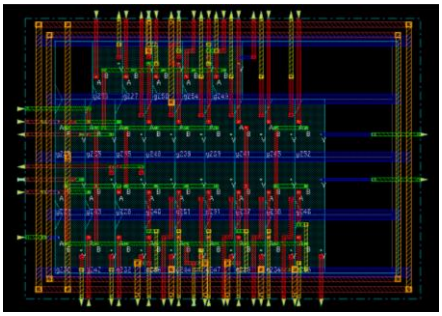

Fig.10: And31

Optimized layout of the proposed single cycle access structure given in Fig. 2 is presented in Fig. 11.

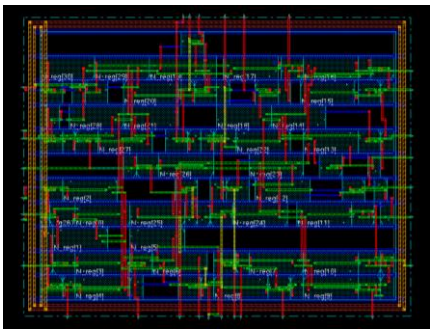

Fig.11: Physical design of the proposed module

Power Report

The internal modules typical parameters, involved in the realization of overall structure is given in Table II. The leakage power of all the modules have maintained at minimum level and the range varied from 1nW to 90nW for 2x1 Mux to 1 out N decoder.

The dynamic power dissipation has maintained the same optimized level of 0.6µW for 2x1 Mux and 70.9 µW for 1 out of N decoder. The combination of leakage and dynamic power consumption has maintained with proportionate level for all the modules.

Table 2: Power Dissipation of Various Blocks

Module	Leakage (nW)	Dynamic (nW)	Total (nW)
2x1Mux	1.314	667.797	669.112
DFF	2.335	2100.163	2102.498
and30	16.718	11223.156	11239.874
and31	17.257	11829.560	11846.816
V1outNDecoder	90	70956.675	71037.563

Conclusion

A single cycle gets to structure is inspected. Distinctive executions with and without hold mode, as well as gated and fragmentary utilization procedures, are shown. The perspectives plausibility, beat control utilization, trading activity in the midst of test, locale, test cycles, at-speed testing and exploring highlights are compared. A coordinate is given on how to select the driving execution. The finest course of action (gSCAS) is compared to RAS utilization and is transcendent in all known RAS courses of action.

Within the occasion that BIST is best due to obliged chip IOs or midway check execution, an address controlled BIST is talked around. The ATPG calculations can be updated with the same methodologies SS executions are optimized. Future work is related to calculations for decreasing the test cycles per net itself, select reordering, and plan optimization for development diminish and de-compression techniques for BIST utilizing the gSCAS.

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