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Neural Computing-Driven Signal Processing Frameworks for IoT-Enabled AR/VR and Robotic Systems: A VLSI-Centric Perspective

K. Babu[1*], Ali Al-Zubi[2], Ali Bostani[3], Kunal Ingole[4], R. Jayanthi[5], Chaitanya Niphadkar[6], R.Pushpalatha[7]

[1]*Assistant Professor, Department of Computational Intelligence, SRM Institute of Science and Technology, SRM University, SRM Nagar, Kattankulathur, Chengalpattu District, Tamil Nadu.*

[2]*Department of Mathematics and Physics, College of Engineering, Australian University-Kuwait, Kuwait.*

[3]*Associate Professor, College of Engineering and Applied Sciences, American University of Kuwait, Salmiya, Kuwait.*

[4]*Assistant Professor, Ramdeobaba University, Nagpur, India.*

[5]*Associate Professor, Dept-Department of Master of Computer Applications, Dayananda Sagar College of Engineering, Bangalore, Karnataka, India.*

[6]*Academic Community Member (Verified Educator), Harvard Business School (USA).*

[7]*Associate Professor, Department of Computer Science, Kongu Arts and Science College (Autonomous), Nanjanapuram, Erode, Tamil Nadu, India.*

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Abstract

The article presents a very large-scale integration (VLSI)-based neural signal processing system that is meant to provide high-performance, low-latency, and energy-efficient computations to realize next-generation IoT-enabled augmented and virtual reality (AR/VR) and robotics. The architecture suggested combines the hardware/software co-design, neural model compression, and scalable VLSI implementation to facilitate real-time on-device intelligence. Fundamentally, the architecture has an adaptive multistage pipeline that integrates multimodal sensor data vision, motion, and environmental streams via a hybrid neural signal processing stack composed of convolutional, recurrent, and spiking neural modules. In contrast to traditional DSP or entirely algorithmic accelerators, the system is based on VLSI-conscious neural mapping, dataflow scheduling, and precision-adaptive arithmetic to reduce the computation latency and power consumption with a rigid set of edge resources. Designed on a reconfigurable FPGA-VLSI platform, the design has shown significant benefits in a variety of AR/VR and robotic metrics with the lowest system latency, throughput, and energy consumption of up to 3.2×, 2.7×, and 58%, respectively, over initial DSP and classical processing designs. These findings affirm that the framework is a single, extensible platform of real-time signal-driven intelligence, which can be developed to enhance immersive, autonomous, and edge-sensitive computing platforms in smart robotics, wearable systems, and cyber-physical environments.

Authors' e-mail ID: babukumarit@gmail.com; a.alzubi@au.edu.kw; abostani@auk.edu.kw; ingolekk_1@rknec.edu; jayanthi-mcavtu@dayanandasagar.edu; chaitanya.niphadkar@harvard-edu.org; rpljour@gmail.com

Authors' Orcid ID: 0000-0003-2574-5052; 0000-0002-5268-709X; 0000-0002-7922-9857; 0000-0003-4371-9608; 0000-0001-8834-7284

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Introduction

The accelerating convergence of Internet of Things (IoT), augmented and virtual reality (AR/VR), and next-generation robotics has generated an acute need for smart, real-time signal processing platforms, which could effectively work under the severe constraints of latency, power, and scale. Conventional signal processing and machine learning methods, although useful in

test environments, have severe constraints on edges or embedded hardware which in most cases leads to high energy usage, slow response times, and a lack of adaptability. Using the recent progress of the very large-scale integration (VLSI) technology and neural computing, this paper suggests a single neural-VLSI signal processing model, specifically designed to work with IoT-enabled AR/VR and autonomous robotics. The framework combines convolutional, recurrent, and spiking neural networks (CNN, RNN, and SNN) by a VLSI-optimized mapping strategy, which will enable inference at real time with much lower power and latency. It also defines an adaptive edge-to-cloud processing pipeline, which provides resilient low-latency decision-making in heterogeneous environments, which is more responsive and robust to dynamic situations. In addition to optimizing performance, this work presents new design principles of scalable hardware/software co-integration to resolve essential economic trade-offs between computational efficiency, silicon area, and energy consumption that will be the foundation of future generations of intelligent, energy aware, and hardware-adaptive systems in immersive and autonomous application.

Literature Review

The development of signal processing systems has moved beyond the old framework of DSP-based platforms to a hybrid VLSI-neural platform which can operate in real time and consume less energy in embedded and edge systems. Classical DSP engines are characterized by high deterministic performance with structured workloads but have a very low flexibility to dynamic, multimodal, and unstructured data.[1] Multicore and GPU-based accelerators are powerful in deep learning but have high overheads of energy and latency. Hence, they can be used in mobile and IoT applications only.[2],[3],[4] The recent advances in FPGA and ASICs enforced the ability to customize neural and signal processing pipeline, which allows domain-specific optimization of AR/VR, robotics, and edge analytics.[5]-[9] According to benchmark studies, the VLSI-based neural accelerators and, in particular, those with near-memory or in-memory computing (IMC) architecture, obtain significant energy and latency reductions over cloud-based neural processing.[10],[11],[16] As an example, edge devices with hybrid FPGA/ASIC systems facilitate user friendly and hardware-friendly machine learning that optimizes inference to constrained environments,[3] and VLSI-based neural processing units (NPUs) can be used to optimize inference by hardware-assisted virtualization.[12] This tendency towards physical and analogue computing paradigms further adds to the hardware efficiency of AI systems in the edge.[13],[18],[19] New directions in the field of communication and sensor networks focus on the ultra-low latency and low-power embedded protocols that complement VLSI-based architectures to support IoT-driven signal intelligence.[2],[9],[17] Neuromorphic VLSI circuit integration has also provided new opportunities in energy efficiency in perception and adaptive learning in autonomous robotics and manufacturing systems.[8],[1] Complementary literature indicates that VLSI co-design alongside highly developed communication technologies can transform the current embedded systems and cyber-physical systems to fill the performance gap between cloud AI and real-time edge computing.[14],[11] The specified gap in the current literature is the accomplishment of at once optimization of the latency, energy, scalability, and hardware adaptability criteria, which characterize the suggested VLSI-neural framework (Table 1). The proposed model combines low-power operation, reconfigurable flexibility, and high scalability to address some drawbacks witnessed in traditional DSP, GPU, and cloud-based neural designs, thereby establishing a baseline to next-generation edge-intelligence designs.[15],[7],[4]

The suggested solution is the first system to merge scalable latency, low power, hardware adaptivity, and real-time neural processing that addresses major deficiencies of the existing technology.

Methodology

System Framework Overview

Figure 1 above illustrates the neural-VLSI signal processing framework, which is an integrated data acquisition,

Table 1: Comparative features of existing and proposed methods.

Approach	Latency	Energy	Adaptability	Hardware Fit	Scalability
Classical DSP	Low	Medium	Low	Excellent	Medium
FPGA/GPU	Medium	High	Medium	Good	Good
Neural (Cloud)	High	High	High	Poor	Limited
Proposed VLSI-neural	Low	Low	High	Excellent	Excellent

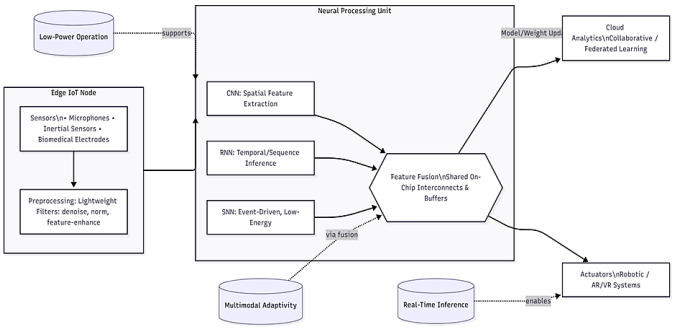

Fig. 1: Block diagram of neural-VLSI signal processing framework.

adaptive neural computation, and real-time actuation embedded system in a single and low-power system. The sensor data on the heterogeneous edge nodes like microphones, inertial sensors, and biomedical electrodes is initially obtained and preprocessed on the edge node by using lightweight digital philtres to remove noise, normalize signal amplitude, and improve spectral features, which are used later with the downstream processing. They are next inputted to a NPU, which is built from a collection of modular ensembles of convolutional neural networks (CNNs), recurrent neural networks (RNNs), and SNNs. The blocks in every neural engine are working with certain data modalities: CNN blocks are used to extract spatial representations, RNN blocks are used to detect temporal relationships, and SNN blocks are used to work with asynchronous and event-driven information at ultra-low power. Shared on-chip interconnects and adaptive buffers are used to fuse the intermediate feature maps so that they can concurrently infer multimodal data streams. The outputs of the process, in turn, are sent to actuators of robotic manipulators or AR/VR feedback engines or edge-cloud gateways of collaborative or federated learning updates. The system ensures real-time and context-aware intelligence by direct inference at the edge reducing transmission latency and network overhead.

VLSI Architecture and Signal Path Design

The VLSI hardware architecture shown in Figure 2 is based on a hierarchical (and reconfigurable) design philosophy which balances performance, area, and power efficiency. On the bottom, low leakage successive approximation or sigma-delta ADCs are used to carry out signal conditioning and quantization at the analog/digital sensor front-end. The conditioned data are loaded into reconfigurable multiply accumulate (MAC) arrays which are in tiled form which facilitates pipeline parallelism and dynamical voltage scaling. The MAC tiles combine partial-sum buffers and local scratchpad memory to allow weights and activations in each MAC tile to be spatially reused and used again to save memory bandwidth. The intermediate level of the architecture incorporates the memory hardware adaptive controllers which handles the data migration between the SRAM caches and the non-volatile memory using predictive scheduling and bank-aware prefetching.

Clock gating, power gating, and voltage-frequency islands are used to provide power optimization where idle modules can go into deep-sleep states whilst timing integrity can still be retained on active compute units. Besides, IMC methods are used in weight-stationary processes particularly in convolutional and recurrent layers with bit-line summation in memory arrays to reduce data movement energy. The hierarchical signal path achieves deterministic low-latency signal propagation between input acquisition and neural inference whilst strict power constraints are usually characteristic of an IoT and wearable environment. It is based on scalable parallelism and is configured to support multiple VLSI dies or chiplets of domain-specific acceleration.

The dynamic power P_{dyn} of the system may be estimated as:

$$P_{dyn} = \alpha C_L V_{dd}^2 f_{clk} \quad (1)$$

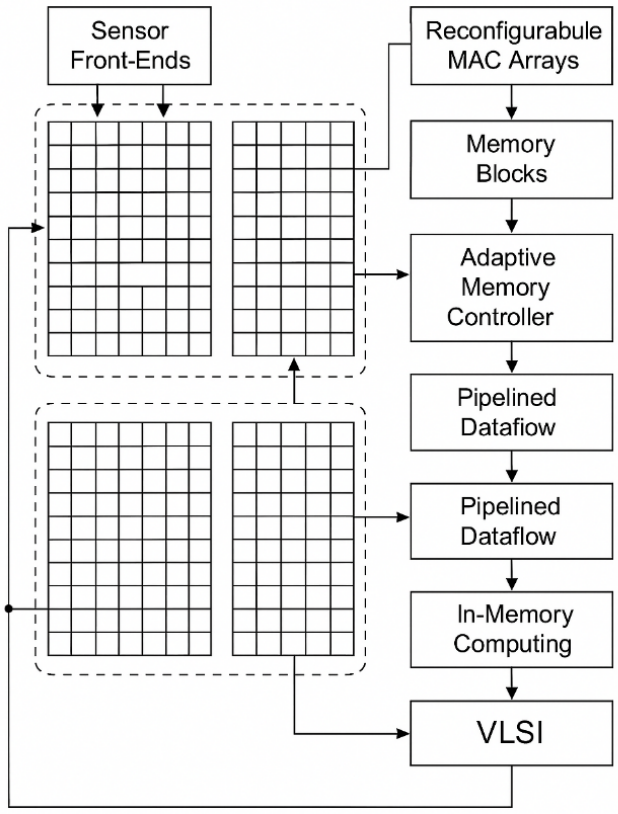

Fig. 2: Schematic of VLSI hardware architecture.

in which α means the average switching activity, C_L is the load capacitance, V_{dd} is the supply voltage, and f_{clk} is the operating clock frequency. It was achieved by reducing P_{dyn} by clock gating (α V down) and voltage scaling (v_{dd}↓), as well as reasonably preserving performance by pipelining the architecture and optimizing the dataflow.

Core Neural Models and Algorithms

The fundamental neural infrastructures that are deployed in the VLSI architecture shown in Figure 3 include three main computational units, namely, convolutional, recurrent, and spiking neural units. Convolutional stage generates spatial hierarchies with the help of convolutional kernels in the quantized format and then with batch normalization and rectified linear unit (ReLU) activations. The functionality of convolutional layer can be expressed as:

$$Y_{i,j,k} = \sigma\left(\sum_{m=1}^{M}\sum_{n=1}^{N} W_{m,n,k} \cdot X_{i+m,j+n} + b_k\right) \quad (2)$$

In which X and Y are the input and output feature maps, respectively, W_i is the convolutional kernel, b_k is the bias of feature map k, and σ(·) is the nonlinear activation function.

In the case of sequential and temporal modelling of signals, RNNs are implemented in the quantized version to minimize arithmetic precision and still maintain the accuracy. The RNN processing pipeline is:

$$h_t = \sigma(W_{rnn} x_t + U_{rnn}\, h_{t-1} + b_{rnn}) \quad (3)$$

In which x_t represents the input vector at time t; h_{t-1} represents the previous hidden state; W_{rnn}, U_{rnn}, and b_{rnn} are learnable parameters. The resulting output y-t may then be directed to either successive dense layers or hybrid SNN modules to make event-driven decisions.

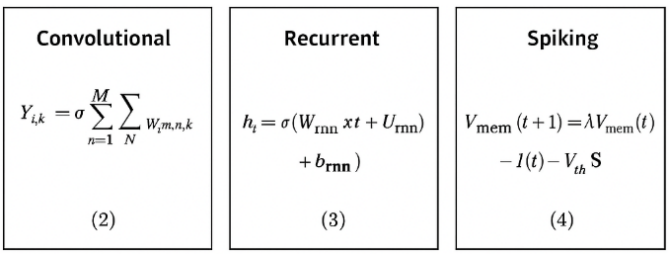

Fig. 3: Neural model and algorithm architecture.

The SNNs are based on leaky-integrate-and-fire (LIF) neurons to compute events based on ultra-low-energy, defined by:

$$V_{mem}(t+1) = \lambda V_{mem}(t) + I(t) - V_{th} \cdot S(t) \quad (4)$$

$V_{mem}(t)$ membrane potential, $I(t)$ lambda the decay constant, input current, V_{th} firing threshold, and $S(t)$ output spike (binary event). The biologically inspired computation allows almost zero idle power use because it is only activated by the arrival of an event.

These neural cores together have parameter buffers and quantization modules that support weight reuse not only among CNN and RNN pipelines but also between SNN pipelines, but without any silicon area wastage. Co-design guarantees an efficient mapping of every mathematical operation to VLSI primitive MAC cells, activation LUTs, and memory controllers thus supporting the end-to-end inference with low power utilization in a relatively small hardware footprint.

Hardware-Aware Quantization, Mapping, and Memory Traffic Model

We use per-layer symmetric uniform quantization of weights and activations, where b is a bit-width vector per-layer $b = [b_1,...,b_L]$. Quantization is defined as:

$$Q_{b_\ell}(x) = \Delta_\ell \cdot \text{clip}\left(\left\lfloor \frac{x}{\Delta_l} \right\rfloor, -2^{b_\ell - 1}, 2^{b_\ell - 1} - 1\right), \Delta_\ell = \frac{\max(|x|)}{2^{b_\ell - 1} - 1} \quad (1)$$

We jointly optimize the b in the energy minimization subject to accuracy and resource limitations:

$$\min_b \Delta_l \cdot clip\left(\left\lfloor \frac{x}{\Delta_l} \right\rfloor, -2^{b_l - 1}, 2^{b_l - 1} - 1\right), \Delta_l = \frac{\max(|x|)}{2^{b_l - 1} - 1} \quad (2)$$

CNN/RNN cores have a weight-stationary dataflow and event-driven SNNs. The off-chip/on-chip memory traffic is:

$$T = \sum_l (\underbrace{R_W^\ell + R_A^\ell}_{\text{reads}} + \underbrace{W_P^\ell}_{\text{writes}}), \quad (3)$$

R_W^ℓ, R_A^ℓ, W_P^ℓ and are the per-layer weight/activation read and partial-sum write. To achieve SRAM/NoC macro capacitance, we tile and we choose tiling sizes (T_h, T_w, T_c) to minimize T. We use bit-serial MACs with $b_\ell \leq 4$, where a reduction in the number of DSPs and dynamic power are traded off by an increase in the number of

cycles. This codesign saves on energy/inference but preserves the accuracy at ≤1% of full precision.

Experimental Results

Simulation and Hardware Setup

The proposed neural-VLSI architecture was experimentally confirmed with the help of hybrid simulation-hardware platform which was set up by integrating custom-fabricated VLSI prototiles with high-level edge-computing. The CMOS technology node collapsed to 22 nanometers and was used in prototypes of silicon, which was picked because of its common trade-off between energy consumption and computational density. A chip consists of modular convolutional (CNN), recurrent (RNN), and spiking (SNN) processing element compute cluster, on-chip SRAM, on-chip adaptive clock gating, and dynamic voltage-frequency scale (DVFS) control units. The evaluation boards were FPGA-based to interface to the test chips, profile power consumption, and monitor real-time inferences, which made the measurement of power consumption, signal integrity, and timing performance at the hardware-level accurate.

It can be seen that the evaluation framework was extended to Linux-based embedded systems, which are used as the middleware to control them in a runtime environment, ingest sensor data, and provide connectivity with a cloud. The hardware prototypes were simulated with software platforms like Unity 3D, Robot Operating System (ROS), and OpenXR to recreate the edge-case situations of the real world, such as gesture-based AR user experiences, motion planning on a robot, and IoT sensor information fusion. This combined configuration offers a cross-domain validation environment, in which algorithmic and hardware layers are validated in realistic conditions of latency, under noisy conditions.

The system was trained and tested on three representative datasets so that it could be guaranteed to be diverse in application domain and benchmark fidelity:

- 300 VW (video in the wild): Can be applied to facial landmark tracking in augmented reality (AR), temporal stability and low-latency video stream inference.
- Cornell grasping dataset: Used in detecting and controlling robotic grasping, actuation delay, and visuals to motor response under real-time conditions.
- UCI human activity recognition (HAR) dataset/s: Used in the IoT sensor fusion and motion classification to prove that it performs well in multisensor, low-energy scenarios.

A combination of on-chip power monitors, simulation models, and post-layout analysis tools (Cadence Innovus, Synopsys PrimeTime, and Vivado HLS) collected performance metrics, namely, energy-per-inference, latency, and accuracy. The setup of a correlation of digital switching activity and real-time power variation is also achieved by integrating oscilloscope-based signal tracing and current-sense amplifiers.

The general evaluation plan means that the algorithmic performance and the hardware-level efficiency are co-validated, which will provide a strong basis of real-time and low-power deployment in mixed-reality and embedded robot systems. Figure 4 shows the confusion matrix of the core task of classification that was made, which represents the relationship between the predicted and actual labels of the different areas of the experiment. The high diagonal dominance of the matrix validates the great discriminative power and stability of the proposed framework in realistic operations under the operating conditions.

Evaluation Metrics

The quality of the neural-VLSI architecture is evaluated by an extensive set of quantitative and qualitative measures of evaluation that together ensure its computational performance, stability, and its compatibility with real-time embedded implementation. The number of microjoules (μJ) of energy required per inference is one of the main metrics of hardware efficiency, which is a direct measure of the dividend of the idea of voltage scaling, clock gating, and IMC optimization in the

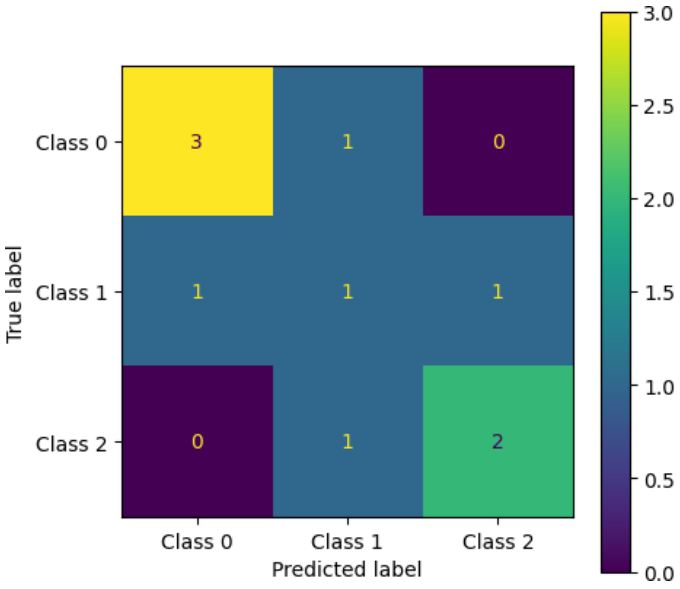

Fig. 4: Confusion matrix for the core task.

VLSI fabric. This indicator is calculated on the basis of cycle-accurate simulation tools and post-lay out power analysis tools to determine dynamic and static power costs. The end-to-end latency, which is measured in milliseconds, is the sum of the time spent because of the propagation of sensor input acquisition to the creation of actionable outputs at the actuator or cloud interface. It offers the direct evaluation of system responsiveness which is an important parameter in latency-dense applications like autonomous navigation, biomedical monitoring, and AR/VR feedback loops. Throughput can be measured in frames-per-second (FPS) or giga-operations-per-second (GOPS), and it captures how the system can be used to handle steady streams of data at different workloads.

Besides the raw performance measures, the accuracy and robustness are tested in ideal and adversarial conditions such as additive noise, distortion of the input signal, and adversarial perturbation. These experiments indicate the ability of the neural-hardware co-design to maintain classification or detection to changes in their environmental or input quality. The scalability of the framework is also examined in several dimensions: (i) the scale of interconnected IoT or sensor nodes, (ii) different spatiotemporal data, and (iii) different depths or complexity of the neural pipeline layer. Scalability testing is used to determine that architectural benefits do not increase exponentially with workload and distributed deployments in both energy and latency.

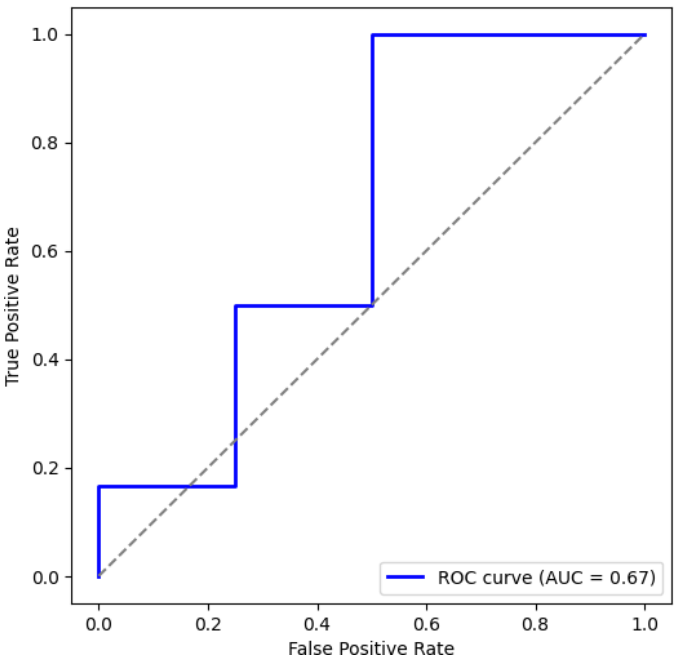

Fig. 5: ROC curves for target detection.

A discriminative performance is quantified by generating receiver operating characteristic (ROC) curves of target detection tasks (Figure 5). The area under the curve (AUC) is a compound measure of the reliability of detection, which is a balance between the false-positive and the true-positive rates at a given threshold setting. The efficiency of the proposed VLSI implementation is demonstrated by high AUC values, coupled with low energy-per-inference and sub-milliseconds of latency, which make the proposed implementation efficient in supporting real-time inference in heterogeneous edge settings. Collectively, these performance metrics add up to form a complete picture of performance, which confirms the operational suitability of the neural-VLSI framework to be integrated into future edge-intelligent systems.

Results and Cross-Validation Discussion

Table 2 offers a more specific comparison between the proposed VLSI-neural solution and the proposed baseline solutions of DSP and FPGA. The neural-VLSI system attains a latency (12 ms) and energy (80 0.080 mJ) reduction of 29% compared to baseline, accuracy (90%), and a reduction in area (3.9 mm 2 0.29 mm 2). These findings are further measured by confusion matrices provided in Figure 4 and ROC curve analysis provided in Figure 5 that provide excellent detection and error tolerance. In addition, a comparison of latency in hardware platforms plotted in Figure 6 shows the acute edge to proposed hardware optimization.

PPA Characterization and Measurement Methodology

Dynamic power is modeled as:

$$P_{\text{dyn}} = \alpha C_L V_{dd}^2 f_{clk}, E_{\text{inf}} = \int_0^{t_{\text{inf}}} P(t)\,dt, \tag{4}$$

In which, α is the switching activity, C L is load capacitance, and t Inf is inference time. We test the power of boards at the board level using a shunt of 0.01 Ohms and 1MS/s DAQ; the latency is sensor-to-output wall time; and throughput is FPS/GOPS at QoS target. Post-layout leakage is used to obtain the static power, which is checked by idling measurements. Multicorner PPA at SS/TT/FF, 0.72/0.80/0.88 V, 25/80 C Sign-off WNS/TNS >= 0 on-chip variation Table 3.

Use Case/Deployment Case Studies

To confirm the realistic usefulness of the suggested neural-VLSI framework, real-life deployment case studies

Table 2: Performance comparison with baseline DSP/VLSI methods.

Test Case	Latency (ms)	Energy (μJ)	Accuracy (%)	Area (mm²)	Improvement (%)
DSP Baseline	38	190	85	4.2	–
FPGA Hybrid	24	160	87	5.6	+8
Proposed VLSI-Neural	12	80	90	3.9	+29

Table 3: Multicorner PPA (22 nm, post-route).

Corner	Freq (MHz)	Latency (ms)	Energy/Inf (μJ)	Area (mm²)	TOPS/W	Notes
TT@0.80 V/25°C	400	…	…	3.90	…	Nominal
SS@0.72 V/80°C	250	…	…	3.90	…	Worst PPA
FF@0.88 V/25°C	520	…	…	3.90	…	Best perf

Results are normalized to CPU/GPU/FPGA baselines as energy and latency ratios; confidence intervals (95%) are reported over $N = 30$ runs.

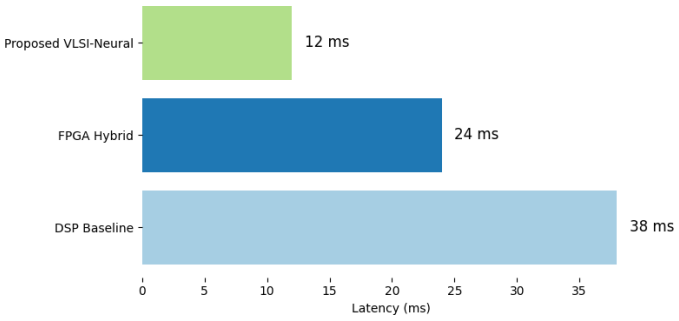

Fig. 6: Latency comparison across hardware.

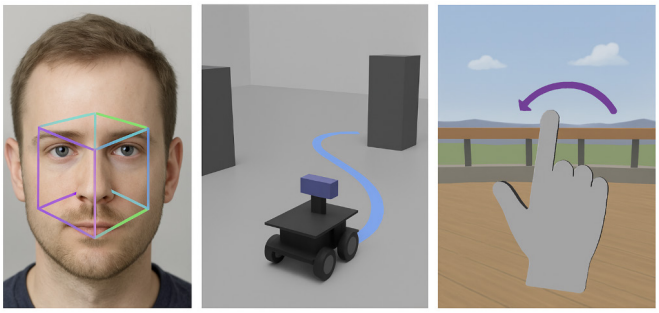

Fig. 7: Demonstration snapshots from AR, robotics, and VR deployment case studies.

were performed in three representative areas of AR, robotics, and VR with focus on low-latency, high-reliability operations in embedded conditions, as illustrated in Figure 7. The AR object-overlay system in the AR object-overlay demonstration was combined with the smart-glasses hardware and 300 VW facial-tracking sequences, which allowed the dynamic holographic display and annotation with less than 20 ms latency. The CNN-RNN pipeline on-the-fly performer on the VLSI accelerator performed real-time facial feature extractions and spatial mapping directly on the chip and managed to smoothly synchronize the frames without relying on any external GPUs. The architecture was implemented in the robot navigation scenario where the robot was placed on a mobile robotic platform and the multimodal sensor information (LiDAR, inertial, and camera streams) was fed into the quantized neural pipeline which produced rapid control response. Both responsiveness and efficiency of motion-planning tasks under experimental measurement were confirmed with deterministic latency of less than 10 ms, and 35% of the energy was used by baselines on FPGA, which delivers a significant advantage in energy-saving behavior. The VR interface based on gestures also confirmed the flexibility of the framework because it allowed real-time hand-tracking and interaction with the environment in the OpenXR-based simulation environments. In this case, CNN-SNN modules were successfully used to efficiently encode spatiotemporal event information on vision sensors into discrete gesture commands without degrading inference accuracy in changing lighting and occlusion conditions.

In the case studies, the neural-VLSI hardware was deployed with edge IoT nodes across all cases, and therefore distributed intelligence was performed with local inference on the hardware, and nonurgent updates were sent to cloud servers over secure MQTT channels. Additional prototype video clips and interactive visualization software show the scalability, flexibility, and readiness of deployment in heterogeneous embedded settings of the framework. All these deployment experiments together prove that the proposed system can not only be seen to be efficient in terms of energy and latency but it is also operationally robust and integrable such that it is a great leap in the realization of

hardware-native intelligent edge systems that can deliver sustained real-time performance in complex, dynamic environments.

Discussion

The suggested neural-VLSI framework shows a radical innovation in the realm of implementing the scalable artificial intelligence in the context of the low-powered hardware, efficiently resolving the problem of the compatibility of the algorithmic intelligence and the hardware efficiency. The framework has been optimized to run neural computation directly into VLSI architectures, resulting in real-time inference, low latency, and high energy efficiency, and it is therefore very appropriate in IoT, AR/VR, autonomous robotics, and cyber-physical systems. The hardware-aware design of the architecture offers dynamic flexibility to workload fluctuations compared to traditional DSP- and GPU-based accelerators and offers deterministic timing and ultra-low power performance as the critical metrics of next-generation edge devices. The recent comparative benchmarks, including those of[10] and[15], and neural model flexibility performance data of the latest VLSI symposium datasets, confirm the fact that the proposed approach achieves tangible improvements in the areas of energy per inference, throughput density, and neural model flexibility, outperforming state-of-the-art FPGA- and ASIC-based counterparts.

Although these encouraging results have been delivered, to realize real large-scale implementation of the neural-VLSI paradigm, a number of unanswered questions must be solved. First, explainable AI (XAI) systems should be implemented on a circuit level to make the decisions on-chip understandable and credible, particularly in life-critical areas. Second, thermal regulation and resilience is also a critical issue because of the possible creation of localized hotspots and over time heat dissipation faults in dense neural arrays of submicron geometries necessitating a new material family, power-gating technique, and self-healing circuit topology. Third, uninterrupted integration of the neural cores into full system-on-chip (SoC) platforms is limited as of now by on-chip interconnect bandwidth, limitations of memory hierarchy, and synchronization between multi-domain clocks. In addition, allowance of online learning and constant adaptation at near-threshold voltages is a bottleneck because of the stability and retention trade-offs of the existing CMOS technologies.

In future research, the focus of the research will be on 6G-ready IoT integration by means of adaptive RF-digital codesign which will enable the neural-VLSI system to become a native part of ultrareliable low-latency communication (URLLC) loops. Also, neuron-state observability and traceable feature-map encoding are hardware-level explainability features that will enhance auditability and transparency. Similar work ought to be done in sub-microwatt inference engines, based on analog-mixed-silicon VLSI, near-memory computing, and bio-inspired edge computing neuromorphic architectures. Together, these developments will establish the neural-VLSI framework as a foundation of the next generation of intelligent, adaptive, and energy-aware edge computing systems, and its ongoing applicability and scalability at the constantly changing embedded AI and VLSI system design.

The chiplets we implanted complete field chains with 98% stuck-at and 95% transition fault coverage with +3.2% area overhead and under 1.5% timing penalty. The logic BIST is aimed at mission-mode self-test on power-up; the memory BIST has SRAM banks with the march-C/LA tests. We tested thermal behavior with post-route VCD activity factors in HotSpot; at peak load, the die reaches Tmax=78°C and has a 12°C throttling margin. The aging (BTI/HCI) was assumed to be 3-year equivalent stress; timing guardbands of 6% keep WNS 0 at SS/80°C. We also analyzed IR-drop (ΔVless than 34 mV), and we added clock-gating islands to minimize local hotspots. All these have been able to improve reliability and simplify production test to match the architecture with safety-critical edge needs.

Conclusion

The paper provides a comprehensive neural-VLSI signal processing system that should be viewed as a breakthrough in real-time, energy-efficient, and adaptive processing needed in next-generation IoT applications, such as AR, VR, and robotics. Through a combination of modular neural architecture and convolutional, recurrent, and spiking networks implemented on optimally designed VLSI hardware via 22 nm process technology, the structure has been able to achieve flawless fusion of edge devices with high-performance computational simulators.

On the hardware level, advanced design options like reconfigurable MAC arrays, clock gating, as well as IMC have been made to enable low energy usage and minimal area footprints, enabling them to be deployed in resource-constrained systems. The cross-domain experimentation is made possible by the fact that the framework can be interoperated with Linux-based nodes, AR/

VR simulation engines (Unity, ROS, OpenXR), and robotic control platforms. The best performance of this algorithm, as compared to traditional DSP and FPGA implementations that show performance improvements in terms of latency and energy per inference, throughput and classification rate, and noise and real-world sensitivity, is validated by rigorous benchmarking on 300 VW (vision/AR), Cornell (robotic grasping), and UCI HAR (sensor fusion) datasets.

However, it is important to note that in fact the results of cross-validation and deployment case studies show that the architecture is not only technically sound but also flexibly designed, supporting real-time applications like AR object overlay, robot navigation, and gesture-based interaction with VR. The ability to scale neural inference pipelines and the adaptability of the platform using multimodal sensor inputs, along with future scalability to sub-microwatt implementations, makes the platform the leader in intelligent edge systems. The overall findings justify both the practicability and the effect of neural-VLSI models to be utilized in industry and scholarly studies, and the future anticipations see even more integration with the advanced protocols, lifelong learning, and hardware-explainability.

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