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SWS-FET-Based Quaternary Magnitude Comparator: Design and Simulation

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Abstract

This article presents a quaternary magnitude comparator (QMC) implemented using spatial wavefunction-switched FETs (SWS-FETs). The native multistate conduction of SWS-FETs eliminates binary-quaternary conversion overhead and reduces transistor count, delay, and power. A one-digit QMC (two-bit) is validated in Cadence at the 180 nm node, achieving 0.14 ns delay and 96 µW total power. A 64-bit instance achieves 0.46 ns delay at 4.84 FO4, where FO4 denotes the fan-out-of-4 inverter delay used as a normalized timing metric, with only 0.79 µW/MHz power. The architecture scales efficiently up to 1024 bits, exhibiting near-linear delay growth from 0.14 ns to 0.72 ns and controlled power up to 12.67 µW/MHz. Compared to CMOS implementations, the proposed SWS-FET QMC demonstrates lower delay, reduced area, and improved energy efficiency, confirming its suitability for compact multivalued arithmetic systems.

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Introduction

The increasing demand for high-performance digital systems has intensified the challenges posed by conventional binary logic, including interconnect congestion, excessive power dissipation, and propagation delay as device scaling approaches physical limits.[1] Multivalued logic (MVL) has been investigated as a potential solution because it increases information density per interconnect and reduces device count and wiring complexity.[2-4] Among various radices, quaternary logic provides a practical tradeoff between information density and implementation feasibility, transmitting twice the information of binary logic over the same number of lines.[5] Magnitude comparators are fundamental arithmetic blocks that determine whether one operand is greater than, less than, or equal to another.[6,7] They are widely applied in processors, memory systems, and scientific computations.[8] In quaternary systems, a comparator generates three outputs (Greater than GT, Less than LT, and Equal EQ), which are directly required by arithmetic units such as adders, subtractors, and multipliers.[8,9] Despite the advantages of MVL, CMOS-based implementations of quaternary comparators are constrained by the binary nature of the devices. They often require multiple supply voltages, complex thresholding circuits, and large transistor counts, which increase area, power consumption, and delay.[10] These limitations reduce the benefits that MVL is intended to deliver.

Spatial wavefunction switched field-effect transistors (SWS-FETs) provide an alternative platform for MVL design. By controlling charge carrier distribution within the channel, a single SWS-FET can natively represent multiple logic states.[5,11] This property enables compact, efficient quaternary circuits, avoiding the overhead of binary-to-quaternary conversion. Prior work has explored the use of emerging devices such as CNTFETs, but the potential of SWS-FETs for quaternary comparators has not been fully addressed.[12,13]

This article presents a quaternary magnitude comparator (QMC) implemented using SWS-FET technology. The proposed design introduces a compact comparator architecture, verifies GT, LT, and EQ outputs in quaternary operation and evaluates its performance in terms of transistor count, delay, and power consumption. A comparison with CMOS and CNTFET implementations demonstrates the superiority of the proposed approach in area efficiency and power delay products.

The proposed circuit and other SWS-FET implementations are modeled and validated in Cadence Virtuoso using the SWS-FET model at the 180 nm technology node.

Background and Applications

This section provides a foundational understanding of MVL systems, the role of magnitude comparators in digital arithmetic, and an overview of SWS-FETs. It concludes with a review of existing QMC implementations and their limitations.

SWS-FET and MVL Overview

MVL extends conventional binary logic by using more than two discrete signal levels to encode information, addressing key VLSI challenges such as interconnect complexity, chip area, and power dissipation.[14,15] As technology scaling advances, interconnections increasingly dominate system area and energy consumption, making MVL an attractive approach for improved efficiency.[16] Among MVL radices, quaternary logic (radix-4) offers a practical tradeoff between information density and implementation complexity.[17] A quaternary signal carries twice the information of a binary signal, reducing wiring requirements; for example, an 8-bit binary word can be represented using four quaternary lines.[18] Voltage-mode implementations typically map the four logic states to 0 V, VDD/3, 2VDD/3, and VDD,[10] enabling compact data representation.[19]

Spatial wavefunction-switched field-effect transistors (SWS-FETs) provide a device-level mechanism for implementing multilevel logic. These devices employ vertically stacked quantum wells that allow spatial control of carrier wavefunctions. Figure 1 illustrates the structure of complementary n-type and p-type SWS-FETs, where gate-voltage modulation confines carriers to different wells, producing multiple conduction states within a single device.[11,20,21] Quantum-mechanical simulations, shown in Figure 2, confirm distinct conduction channels at specific gate voltages for both n-type and p-type devices, supporting stable quaternary operation.[22] Key structural parameters are summarized in Table 1.

Experimental and simulation results further validate SWS-FET behavior. Figure 3 presents measured ID–VD characteristics of a fabricated n-type SWS-FET, while Figure 4 shows simulated IDS–VGS characteristics for both device types, demonstrating clear four-level conduction.[23] At the circuit level, a quaternary inverter implemented using SWS-FETs is shown in Figure 5, with transient operation verified in Figure 6. Prior studies report that SWS-FET-based quaternary logic elements exhibit stable voltage separation and favorable gate-level power and area characteristics without external thresholding circuitry.[11,24-26,27] This foundation motivates the use of SWS-FET technology for higher-level MVL and arithmetic structures, which are explored in the following sections.

Literature Review: Existing QMC Implementations

The development of QMCs has been investigated across several device technologies, each offering advantages but also facing critical limitations.

CMOS-based QMCs have been widely studied due to the maturity of the technology, yet they face fundamental challenges in implementing MVL. Generating and distinguishing four distinct voltage levels typically requires multiple power supplies, voltage dividers, or

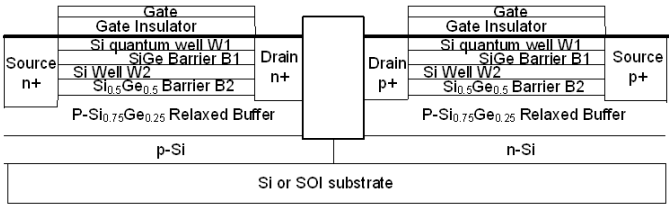

Fig. 1: Cross-section of complementary n-type and p-type SWS-FETs[22]

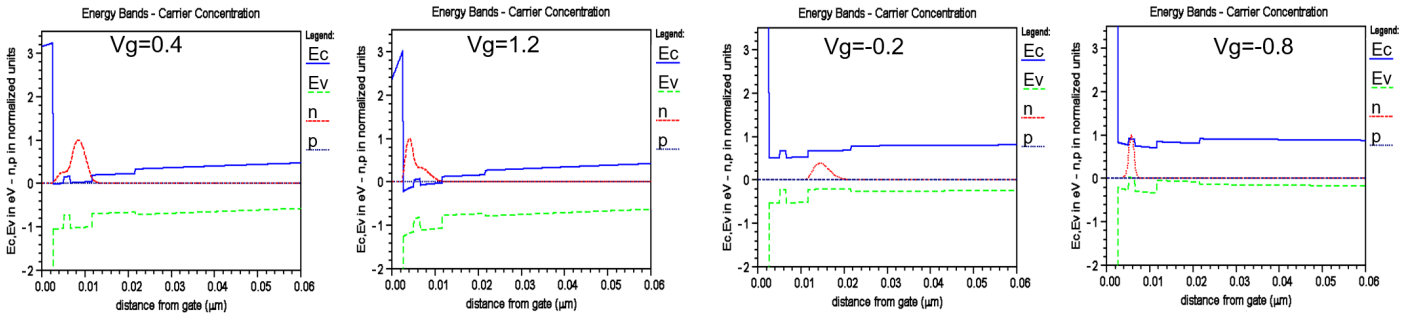

Fig. 2: Energy band diagrams of the SWS-FET showing multicarrier confinement[22]

Table 1: Quantum-Well Parameters Used in SWS-FET Simulations.[22]

Layer	Thick nm	X-nSWS eV	*X*-pSWS eV	Eg eV	me	mh	εr	Nd cm-3	Na cm-3
SiO2	2.5	0.9	0.9	9	0.5	0.5	3.9	0*100	0*100
Si QW1	2.5	3.7	4.15	1.04	0.19	0.49	11.9	0*100	0*100
SiGe(.5)	1.5	4.0	4.0	0.89	0.13	0.38	14	0*100	0*100
Si QW2	5.0	3.7	4.15	1.04	0.19	0.49	11.9	0*100	0*100
SiGe(.5)	10	4.0	4.0	0.89	0.13	0.38	14	0*100	0*100
SiGe(.75)	50	3.95	3.9	1.05	0.13	0.38	14	0*100	1*1016
Si	100	4.0	3.8	1.1	0.19	0.49	11.9	0*100	1*1016

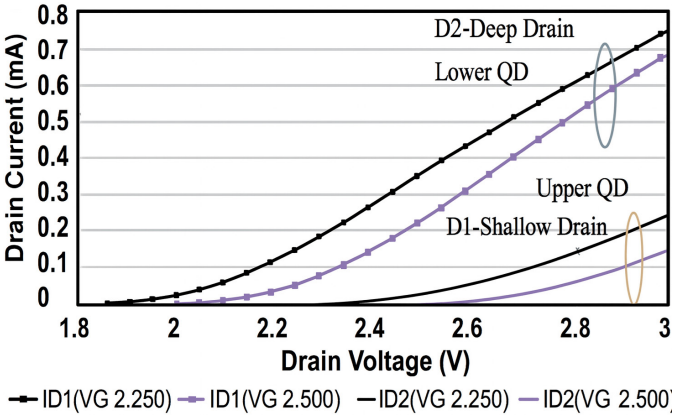

Fig. 3: Measured ID-VD characteristics of a fabricated n-type SWS-FET[23]

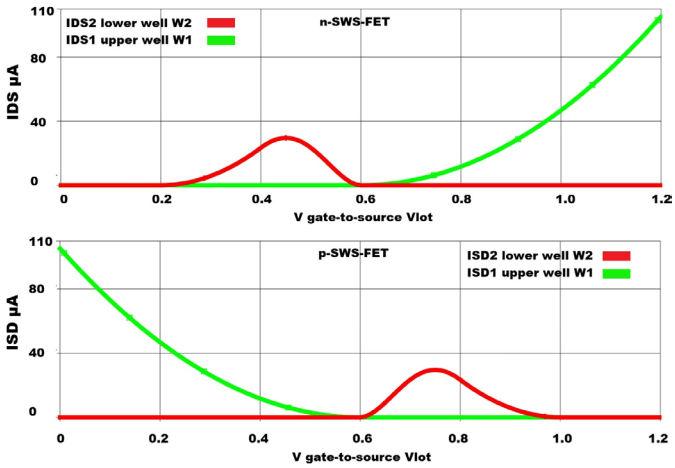

Fig. 4: Simulated IDS-VGS characteristics of n-type and p-type SWS-FETs

level shifters.[10,16,19] Such additions increase transistor count, chip area, and power dissipation compared to binary designs.[10] For instance, a 4-bit CMOS comparator may require substantially more transistors and higher power than its gate diffusion input (GDI)-based counterpart.[28,29] In mixed-signal systems, additional decoders are often needed to convert between multivalued and binary domains, introducing overhead and susceptibility to noise.[30,31]

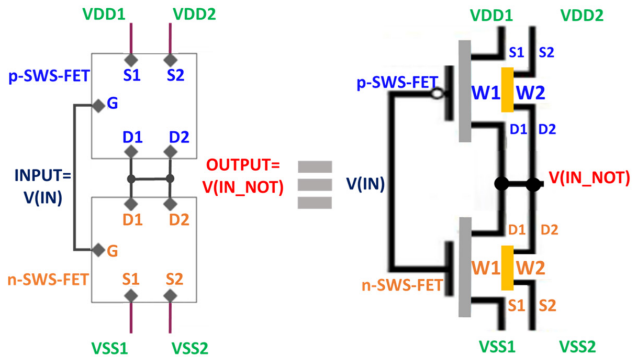

Fig. 5: SWS-FET-based quaternary inverter circuit

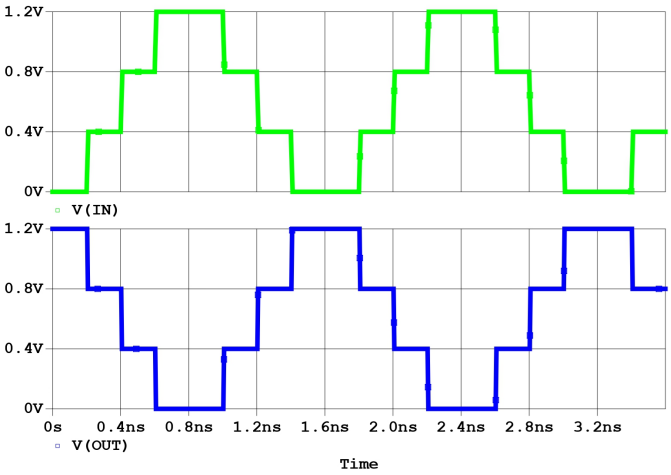

Fig. 6: Transient response of the SWS-FET quaternary inverter

CNTFET-based QMCs have also been proposed, leveraging the tunable threshold voltage of carbon nanotubes, which can be adjusted by varying nanotube diameter.[32] This property makes CNTFETs naturally suited to multi-threshold logic gates, and several designs for quaternary circuits such as latches, flip-flops, and arithmetic units have been reported.[15,33,34] However, CNTFET magnitude comparators still involve intricate circuit arrangements and require careful optimization to account for process variations.[34]

Overall, current QMC implementations face tradeoffs between design complexity, device count, power

consumption, and operating speed. Although CMOS and CNTFET technologies have demonstrated functional quaternary comparators, they typically incur significant overhead when handling multiple logic levels. To overcome these limitations, this work leverages the intrinsic multistate switching of SWS-FETs to achieve a more compact and efficient solution. A summary of representative CMOS and CNTFET QMC implementations is provided in Table 2.

Proposed QMC Architecture

This section details the architectural design of the proposed QMC, which leverages SWS-FETs. The design focuses on directly implementing quaternary comparison logic to achieve high efficiency and compactness.

Functional Requirements

The QMC compares two single-digit quaternary inputs, A and B, where both inputs ∈ {0, 1, 2, 3}. It generates three mutually exclusive outputs: Greater Than (GT), Equal (EQ), and Less Than (LT).[10,11] Each output is asserted to quaternary logic level "3" when its condition is satisfied and remains at "0" otherwise,[35] consistent with MVL design principles, the functional definitions of the outputs and their roles in arithmetic units are as follows:

- GT: The GT output is "3" if A > B; otherwise, it is "0".
- EQ: The EQ output is "3" if A = B; otherwise, it is "0".
- LT: The LT output is "3" if A < B; otherwise, it is "0".

The design requirements for the proposed QMC emphasize direct quaternary implementation. This avoids intermediate binary conversions, ensuring stable and well-defined output logic levels compatible with SWS-FET characteristics.[21,26] Furthermore, the architecture aims for minimal transistor usage and inherent compatibility for cascading to enable multi-digit quaternary comparison, thereby contributing to overall system efficiency and scalability.[36,37]

CMOS-Based Multi-Flag QMC Design

In adapting a conventional binary circuit for MVL operation, each pair of binary inputs is treated as one quaternary digit through a simple binary-to-quaternary mapping. The two bits, designated as the Most Significant Bit (MSB) and the Least Significant Bit (LSB), together define the four logic states of the quaternary domain. The MSB corresponds to the higher positional weight, while the LSB represents the lower one.

From the 16-row truth table established for this design, summarized in Table 3, the minimal sum-of-products (SOP) expressions for the comparison outputs can be derived. The logical formulations of the greater-than (GT_logic), equality (EQ_logic), and less-than (LT_logic) functions are expressed as follows:

$$GT\_logic = OR\ (AND(NB1,A1),\ AND(NB1,NB0,A0),\ AND\ (NB0,A1,A0)) \quad (1)$$

$$EQ\_logic = NOR(XOR(B1,A1),\ XOR(B0,A0)) \quad (2)$$

$$LT\_logic = NOR(GT\_logic,\ EQ\_logic) \quad (3)$$

where NB1 and NB0 denote the inverted input signals of B1 and B0, respectively, such that NB1 = NOT(B1) and NB0 = NOT(B0). The operators AND, OR, XOR, and NOR denote standard Boolean logic operations.

Figure 7 illustrates the CMOS logic realization of GT_logic, EQ_logic, and LT_logic based on Equations (1)–(3). Table 4 reports the detailed transistor-count breakdown of the binary-coded QMC gates and confirms a 58-transistor core implementation using

Table 2: Summary of Representative CMOS and CNTFET-Based QMC Designs.

Technology	Key Approach	Advantages	Limitations
CMOS	Uses multiple supplies and level shifters	Mature and widely available	High power, large area, and high transistor count
CNTFET	Diameter-based threshold control	Supports multi-threshold logic at low voltage	Complex layout and process variation issues

Table 3: Truth Table of the QMC.

	B=0 (00)	B=1 (01)	B=2 (10)	B=3 (11)
A=0 (00)	GT=0, LT=0, EQ=3	GT=0, LT=3, EQ=0	GT=0, LT=3, EQ=0	GT=0, LT=3, EQ=0
A=1 (01)	GT=3, LT=0, EQ=0	GT=0, LT=0, EQ=3	GT=0, LT=3, EQ=0	GT=0, LT=3, EQ=0
A=2 (10)	GT=3, LT=0, EQ=0	GT=3, LT=0, EQ=0	GT=0, LT=0, EQ=3	GT=0, LT=3, EQ=0
A=3 (11)	GT=3, LT=0, EQ=0	GT=3, LT=0, EQ=0	GT=3, LT=0, EQ=0	GT=0, LT=0, EQ=3

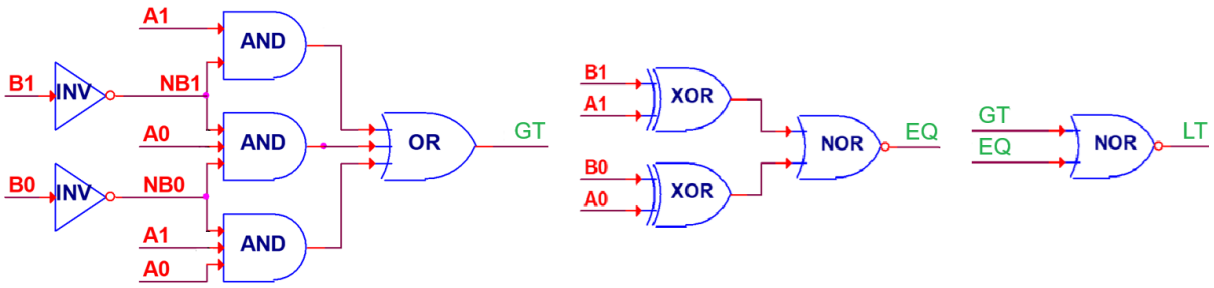

Fig. 7: CMOS binary-coded QMC implementing GT, EQ, and LT outputs

Table 4: Transistor Count for the Binary-Coded CMOS QM.

Gate type	GT OUT	LT OUT	EQ OUT XOR-TG
Inverter (two inputs)	2*2=4		--
AND (two inputs NAND + two inputs Inverter)	1*(4+2)=6		--
AND (three inputs NAND + two inputs Inverter)	2*(6+2)=16		--
OR (three inputs NOR + two inputs Inverter)	1*(6+2)=8		--
NOR (two inputs)		1*2=4	1*2=4
XOR using NAND	--	--	--
XOR using Transmission Gate TG	--	--	2*8=16
Total Transistor count (TC)	34	4	20

transmission-gate XORs. To ensure interoperability with conventional binary systems, conversion interfaces are required. The quaternary-to-binary (Q-to-B) stage can be implemented as a 1-hot encoder (≈12 transistors) or as a 2-bit analog-to-digital converter (ADC, ≈40 transistors), while the binary-to-quaternary (B-to-Q) stage can be realized using a 1-hot decoder (≈28 transistors) or a 2-bit digital-to-analog converter (DAC, ≈12 transistors). By adopting the optimized configuration combining the 1-hot Q-to-B encoder and the 2-bit DAC B-to-Q converter, the total transistor count becomes 58 + 12 + 12=82, achieving a functionally complete yet area-efficient binary-encoded QMC architecture.

SWS-FET-Based Multi-Flag QMC Design

The proposed QMC based on SWS-FET technology comprises three dedicated logic blocks that generate the comparator flags: Greater (GT), Less (LT), and Equal (EQ). The multi-flag QMC provides these three outputs independently, each driving quaternary logic level “3” when its condition is satisfied and “0” otherwise.

Each flag block is realized solely with SWS-FET cells: pSWS devices form the pull-up network (PUN), while nSWS devices form the pull-down network (PDN). The output node is directly connected to the reference rails through conditional pass paths. The rail mapping follows the adopted quaternary voltage levels (0 → 0.0 V, 1 → 0.4 V, 2 → 0.8 V, 3 → 1.2 V). A compact rail-select header at the top of each schematic chooses the active rail pair (e.g., VDD1 and VSS1) for the required flag level. If an interface with reduced swing is needed, a two-stage limiter can bound any flag output to 0–0.4 V without altering the internal pass network.

Complementary inputs are employed to minimize logic depth. The inverted signals N_A and N_B are generated by compact SWS-FET inverters, such that levels map as 0 → 3 and 1 → 2 across the four rails. These complementary lines are routed as primary inputs to the PUN/PDN structures, reducing series stack depth and balancing conduction choices.

Figure 8 shows the schematic diagrams of the 1-digit (2-bit) multi-flag QMC for GT, EQ, and LT networks. In each case (flag), the PUN lists the pSWS series devices that connect the output to VDD, while the PDN lists the nSWS series that connect the output to VSS1 when the flag is de-asserted. The three networks are topologically balanced with identical fan-in depth, ensuring uniform propagation delay across GT, EQ, and LT. Because the outputs are rail-driven through SWS pass paths, no static short-circuit current flows in steady state, and the total device count is lower than in an equivalent CMOS implementation. The active pull-up and pull-down conduction paths for all input combinations (A, B) are explicitly listed in Tables 5-7 for the GT, EQ, and LT flags, respectively.

Figure 9 shows a CMOS-based implementation in which the LT flag is derived from the GT and EQ outputs using

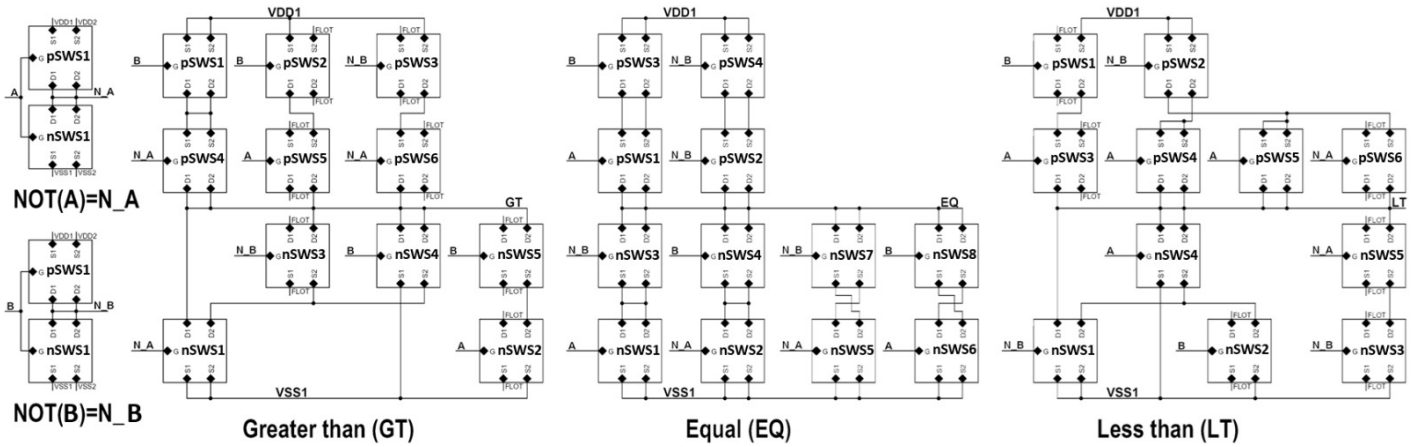

Fig. 8: SWS-FET-based one-digit (2-bit) multi-flag QMC.

Table 5: GT Conduction Paths of the SWS-FET-Based QMC.

A \ B	0	1	2	3
0	PDN: nSWS1-W1	PDN: nSWS1-W1	PDN: nSWS1-W1 & nSWS4-W2	PDN: nSWS1-W1 & nSWS4-W1
1	PUN: pSWS5-W2 & pSWS1-W1	PDN: nSWS1-W2 & nSWS3-W2	PDN: nSWS1-W2 & nSWS4-W2	PDN: nSWS4-W1
2	PUN: pSWS4-W2 & pSWS1-W1	PUN: pSWS4-W2 & pSWS1-W2	PDN: nSWS2-W2 & nSWS5-W2	PDN: nSWS4-W1
3	PUN: pSWS4-W1 & pSWS1-W1	PUN: pSWS4-W1 & pSWS1-W2	PUN: pSWS6-W1 & pSWS3-W2	PDN: nSWS4-W1

Table 6: EQ Conduction Paths of the SWS-FET-Based QMC.

A\B	0	1	2	3
0	PUN: pSWS1-W1 & pSWS3-W1	PDN: nSWS5-W1 & nSWS7-W2	PDN: nSWS2-W1 & nSWS4-W2	PDN: nSWS2-W1 & nSWS4-W1
1	PDN: nSWS5-W2 & nSWS7-W1	PUN: pSWS1-W2 & pSWS3-W2	PDN: nSWS2-W2 & nSWS4-W2	PDN: nSWS2-W2 & nSWS4-W1
2	PDN: nSWS1-W2 & nSWS3-W1	PDN: nSWS1-W2 & nSWS3-W2	PUN: pSWS2-W2 & pSWS4-W2	PDN: nSWS6-W2 & nSWS8-W1
3	PDN: nSWS1-W1 & nSWS3-W1	PDN: nSWS1-W1 & nSWS3-W2	PDN: nSWS6-W1 & nSWS8-W2	PUN: pSWS2-W1 & pSWS4-W1

Table 7: LT Conduction Paths of the SWS-FET-Based QMC.

A \ B	0	1	2	3
0	PDN: nSWS1-W1	PUN: pSWS1-W2 + pSWS3-W1	PUN: pSWS2-W2 + pSWS4-W1	PUN: pSWS2-W1 + pSWS5-W1
1	PDN: nSWS1-W1	PDN: nSWS3-W2 + nSWS5-W2	PUN: pSWS2-W2 + pSWS4-W2	PUN: pSWS2-W1 + pSWS5-W2
2	PDN: nSWS1-W1	PDN: nSWS1-W2 + nSWS4-W2	PDN: nSWS2-W2 + nSWS4-W2	PUN: pSWS2-W1 + pSWS6-W2
3	PDN: nSWS4-W1	PDN: nSWS4-W1	PDN: nSWS4-W1	PDN: nSWS4-W1

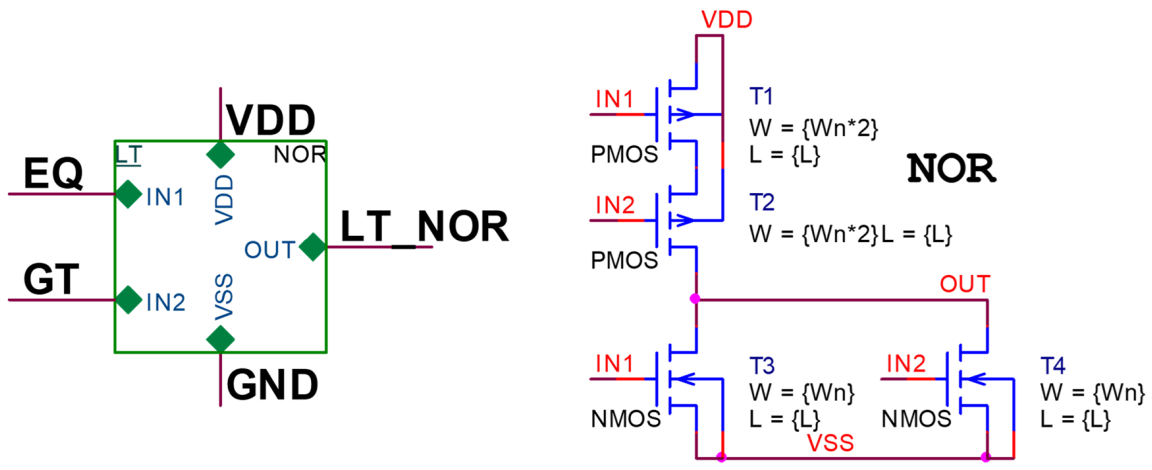

Fig. 9: CMOS NOR-based LT generation for a one-digit (2-bit) QMC.

a two-input NOR gate, according to LT = NOR(GT, EQ). In contrast to the direct SWS-FET PUN-PDN realization shown in Figure 8, this CMOS approach simplifies the LT stage by reusing the GT and EQ signals at the expense of an additional logic operation. Table 8 summarizes the transistor count of the proposed one-digit (2-bit) QMC for the different GT, EQ, and LT realizations, including both the SWS-FET-based implementation and the alternative CMOS NOR-based LT generation.

Multi-Digit QMC Extension using Multi-Flag QMC

The one-digit QMC serves as the fundamental building block for multi-digit comparison. To enable comparisons between multi-digit operands, multiple one-digit QMC units are cascaded in a hierarchical multi-flag architecture, as illustrated in Figure 10, where m denotes the total number of comparison stages.

Each QMC compares the corresponding quaternary digits of the operands A = (A[m−1] .... A[0]) and B = (B[m−1] .... B[0]) and generates two binary outputs: GT[i] = 1 when A[i] > B[i], and EQ[i] = 1 when A[i] = B[i]. Here, i denotes the digit index, with i = 0 corresponding to the least significant digit (LSD) and i = m − 1 corresponding to the most significant digit (MSD).

The local comparison flags propagate through the hierarchical logic from lower to higher digit positions. If a difference is detected at any stage, the comparison result is finalized; otherwise, equality continues to propagate, ensuring modularity, uniform timing, and consistent evaluation across all stages.

The logical relationships between consecutive comparison stages are defined using two propagation parameters: the greater-than propagation signal F and the equality propagation signal H, as given by Equations (4) and (5), respectively.

$$F[i] = OR(GT[i], AND(EQ[i], F[i\text{-}1])) \text{ here } i = 1,.., \ m - 1, \text{ and } F[0] = GT[0] \quad (4)$$

$$H[i] = AND(EQ[i],H[i\text{-}1]) \text{ here } i = 1,..,m - 1, \text{ and } H[0] = EQ[0] \quad (5)$$

The final greater-than output GT[m], final equality output EQ[m], and final less-than output LT[m] are obtained as follows:

$$GT[m] = F[m\text{-}1] \quad (6)$$

$$EQ[m] = H[m\text{-}1] \quad (7)$$

$$LT[m] = NOR(GT[m],EQ[m]) \quad (8)$$

Binary operations are implemented using NAND and inverter gates to reduce transistor count for m > 4, while maintaining full compatibility with the SWS-FET logic framework.

Applying De Morgan theorem to Equation (4) yields the equivalent NAND-based realization (9)

$$F[i] = NAND(NOT(GT[i]),NAND(EQ[i],F[i\text{-}1])) \quad (9)$$

When a three-input NAND gate is available, Eq. (9) can be compactly implemented as (10)

$$F[i]=NAND3(NOT(GT[i]),EQ[i],F[i\text{-}1]) \quad (10)$$

where NAND3 denotes a three-input NAND gate.

These compact forms preserve full Boolean correctness while minimizing logic depth. Figure 11 illustrates

Table 8: Transistor Count Summary for One-Digit (2-bit) QMC Implementations.

FUNCTION	TC	Details / Expression
Inverter SWS	4	2 Quaternary inverter for N_A and N_B
GT SWS	11	SWS-based as 5 nSWS + 6 pSWS
EQ_SWS	12	SWS-based as 8 nSWS + 4 pSWS
LT_SWS	11	SWS-based as 5 nSWS + 6 pSWS
LT_NOR	4	Binary NOR (GT,EQ) (2 NMOS, 2 PMOS)
1 Digit QMC Unit (GT, EQ)	27	4+11+12=27 as Inputs Inverter + GT + EQ
1 Digit QMC Unit (GT, EQ, LT_CMOS)	31	4+11+12+4=31 as Inputs Inverter + GT + EQ + LT
1 Digit QMC Unit (GT, EQ, LT_SWS)	38	4+11+12+11=38 as Inputs Inverter + GT + EQ + LT

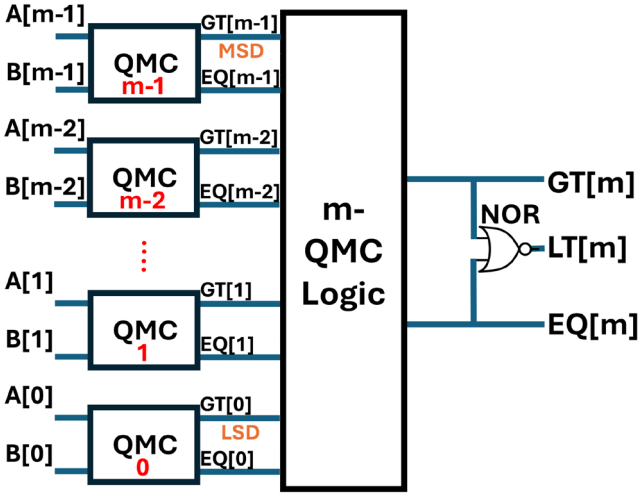

Fig. 10: Hierarchical m-digit QMC architecture

the implemented *m* = 2 and *m* = 4 QMC logic circuits, referred to as Circuit 1 and Circuit 2, respectively. The detailed gate composition and corresponding transistor count (TC) are summarized in Table 9.

The overall hierarchical architecture is formed by interconnecting the *m* = 2 and *m* = 4 logic circuits across successive stages. Each stage contains a specific combination of NAND2, NAND3, and NAND4 gates arranged to maintain balanced fan-in and linear scalability with operand size. The distribution of logic units across the hierarchy is summarized in Table 10.

The total transistor count (TC) for an m-digit QMC is defined by:

$$TC = TC\_QMC\_logic + m \times TC\_QMC\_unit \quad (11)$$

where TC_QMC unit denotes the transistor count of a one-digit QMC unit implementing the GT and EQ functions, which consists of 27 SWS-FET transistors, and m represents the number of quaternary digits. The cumulative transistor counts for multi-digit QMC architectures up to *m* = 512 are reported in Table 11.

Figure 12 illustrates the hierarchical construction of the proposed multi-digit QMC for operand sizes *m* = 8, 16, and 32. Each architecture is formed by cascading the basic *m* = 2 (Circuit 1) and *m* = 4 (Circuit 2) logic units across sequential stages. In each higher configuration, the number of Circuit 1 and Circuit 2 modules doubles in the first stage and decreases geometrically toward the final NOR stage that produces GT(m), EQ(m), and LT(m). This hierarchical scaling ensures balanced propagation delay, reduced interconnect complexity, and linear transistor growth with operand size.

The effective propagation delay of the one-digit QMC (tp0) is determined by the maximum of the propagation delays of the Greater-Than (tp_GT) and Equal signal paths (tp_EQ) as expressed in (12):

$$tp0 = max(tp\_GT, tp\_EQ) \quad (12)$$

Here, tp_GT and tp_EQ are measured from the input transition to the corresponding output transition of the one-digit QMC.

The *m* = 2 logic block (Circuit 1) exhibits a propagation delay denoted as tp_cr1, while the *m* = 4 logic block (Circuit 2) exhibits a propagation delay denoted as tp_cr2. These delays are defined as

$$tp\_cr1 = 2 \times tp\_nand2 \quad (13)$$
$$tp\_cr2 = 2 \times tp\_nand4 \quad (14)$$

where tp_nand2 and tp_nand4 represent the intrinsic propagation delays of the two-input and four-input NAND gates, respectively. These expressions reflect the two-stage critical signal path of each logic network, corresponding to the maximum logic depth defined by the compact NAND-based Boolean implementation.

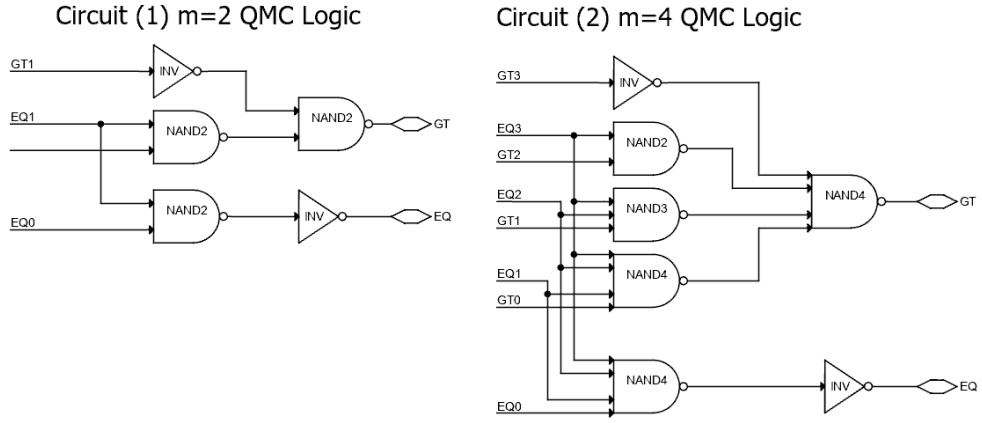

Fig. 11: NAND-based CMOS logic for *m* = 2 and *m* = 4 QMC propagation circuits

Table 9: Gate-Level Composition of *m* = 2 and *m* = 4 QMC Logic Blocks.

m (digits)	GT: INV	GT: NAND2	GT: NAND3	GT: NAND4	EQ: INV	EQ: NAND2	EQ: NAND4	TC
Circuit 1, m=2	1	2	0	0	1	1	0	16
Circuit 2, m=4	1	1	1	2	1	0	1	38

Table 10: Stage Distribution of the Multi-Digit QMC Architecture.

m (digits)	1	2	4	8	16	32	64	128	256	512
Bit n=m*2	2	4	8	16	32	64	128	256	512	1024
Stage 1 m=2 QMC Logic unit Circuit 1	0	1	0	0	0	0	0	0	0	0
Stage 1 m=4 QMC Logic unit Circuit 2	0	0	1	2	4	8	16	32	64	128
Stage 2 m=2 QMC Logic unit Circuit 1	0	0	0	1	0	0	0	0	0	0
Stage 2 m=4 QMC Logic unit Circuit 2	0	0	0	0	1	2	4	8	16	32
Stage 3 m=2 QMC Logic unit Circuit 1	0	0	0	0	0	1	0	0	0	0
Stage 3 m=4 QMC Logic unit Circuit 2	0	0	0	0	0	0	1	2	4	8
Stage 4 m=2 QMC Logic unit Circuit 1	0	0	0	0	0	0	0	1	0	0
Stage 4 m=4 QMC Logic unit Circuit 2	0	0	0	0	0	0	0	0	1	2
Stage 5 m=2 QMC Logic unit Circuit 1	0	0	0	0	0	0	0	0	0	1
Stage 5 m=4 QMC Logic unit Circuit 2	0	0	0	0	0	0	0	0	0	0

Table 11: Total Transistor Count of the Multi-Digit QMC.

m (digits)	1	2	4	8	16	32	64	128	256	512
Bit n=m*2	2	4	8	16	32	64	128	256	512	1,024
TC of SWS-FET transistor	27	54	108	216	432	864	1,728	3,456	6,912	13,824
TC of CMOS transistor	0	16	38	92	190	396	798	1,612	3,230	6,460
TC of LT: NOR "CMOS"	4	4	4	4	4	4	4	4	4	4
Total TC of m-QMC	31	74	150	312	626	1,264	2,530	5,072	10,146	20,288

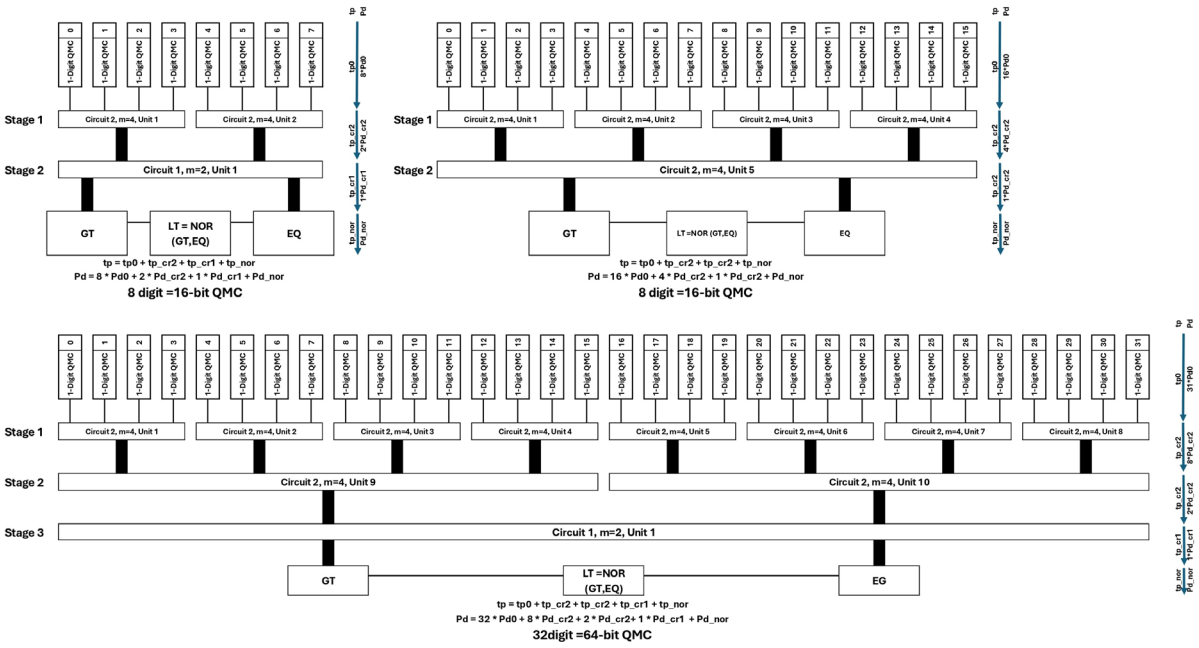

Fig. 12: Hierarchical stage organization for **m** = 8, 16, and 32 QMCs.

For each hierarchical stage s(k), where k denotes the stage index (k = 1, 2, 3, …), the propagation delay depends on the type of logic block employed. Specifically, the stage delay tp_s(k) is equal to tp_cr1 when Circuit 1 is used and tp_cr2 when Circuit 2 is used. This relationship is expressed as

$$tp\_s(k) = \begin{cases} tp\_cr1 \; if \; stage \; k \; uses \; Circuit \; 1 \\ tp\_cr2 if \; stage \; k \; uses \; Circuit \; 2 \end{cases} \quad (15)$$

The total CMOS logic delay (tp_logic) is obtained by summing the propagation delays of all hierarchical stages and is expressed as

$$tp\_logic = \sum_{j=1}^{N\_stage} tp\_s(j) \quad (16)$$

where N_stage denotes the total number of hierarchical stages.

The overall propagation delay of the multi-digit QMC (tp) is then given by

$$tp = tp0 + tp\_logic + tp\_nor \quad (17)$$

where tp_nor represents the propagation delay of the NOR gate used for LT generation.

The average power dissipation (Pd) is determined by summing the dynamic and leakage components of all logic units, and Pd is obtained as

$$Pd = N0^{*} Pd0 + N1^{*} Pd\_cr1 + N2^{*} Pd\_cr2 + Pd\_nor \quad (18)$$

Here, N0, N1, and N2 denote the numbers of one-digit QMC units, Circuit 1 (m = 2), and Circuit 2 (m = 4) logic units, respectively. The terms Pd0, Pd_cr1, and Pd_cr2 represent the average power dissipations of the one-digit QMC, Circuit 1, and Circuit 2 logic units, respectively. The term Pd_nor accounts for the power consumption of the NOR gate used to generate the LT output.

All numerical evaluations of propagation delay and total power are presented in Section 4 – Simulations and Results.

Simulations and Results

All circuit simulations were performed in Cadence Virtuoso using the SWS-FET compact model with EKV-based parameters corresponding to a 180 nm technology node.[11,20,21,23-26] The proposed SWS-FET-based multi-flag QMC was simulated using the parameters summarized in Table 12. A deterministic full-swing quaternary input sequence was applied, in which input A was updated every 200 ps and input B every 800 ps, ensuring complete coverage of all comparison conditions (A > B, A = B, and A < B).

Table 12: Simulation Parameters for QMC Evaluation.

Parameter	Value / Description
Technology node assumption	180 nm EKV-based SWS-FET model
Load capacitance	1 fF per output node
Input excitation frequency	5 GHz (base functional stimulus period)
Voltage levels	0 V, 0.4 V, 0.8 V, 1.2 V (logic levels 0,1,2,3)
Supply voltage (VDD, VDD1)	1.2 V
Ground reference (VSS1)	0 V
Input activity	Full-swing quaternary sequence; A updates every 200 ps, B every 800 ps

Figure 13 presents the transient response of the 1-digit SWS-FET-based QMC. The waveforms illustrate the input signals A and B (blue) and the corresponding outputs: GT (green), EQ (purple), LT (red), and LT_NOR (black). The LT_NOR output is generated using the CMOS NOR binary logic gate according to LT_NOR = NOR(GT, EQ). Each output correctly asserts the quaternary logic level "3" (VDD = 1.2 V) when its relational condition is satisfied and returns to "0" otherwise, demonstrating accurate quaternary functionality, low-latency switching, and full synchronization among all comparator outputs.

Table 13 summarizes the propagation delays and total power consumption for all QMC building blocks. Based on the measured data, the total power dissipation is expressed in μW/MHz, evaluated under a 5 GHz input-switching frequency and a 1 fF load capacitance. The overall propagation delay of each block is normalized with respect to the fan-out-of-4 (FO4) delay of a minimum-sized inverter in the same technology. In this study, the reference FO4 delay of the SWS-FET inverter is 95 ps.

Table 14 lists the end-to-end comparison power and delay including both the unit QMC and the m QMC logic, representing the observable latency of the m digit operation. For m equal to 1, 2, and 4, the values are obtained from simulation. For m >4, the results are estimated using Eqs. (11)–(18).

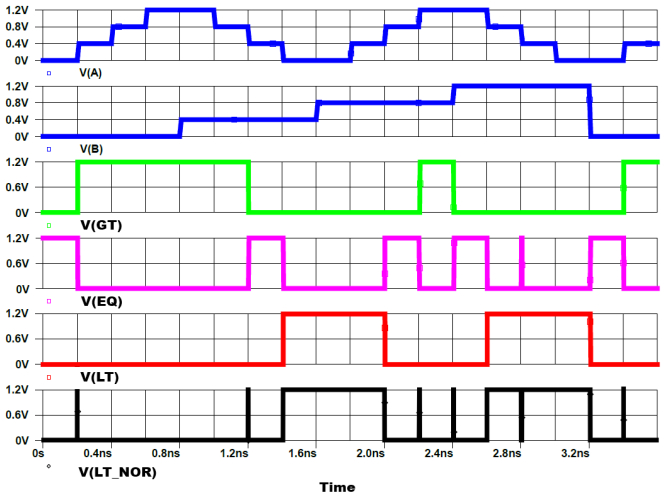

Fig. 13: Transient waveforms of the one-digit SWS-FET-based QMC at 5 GHz.

Table 13: Propagation Delay (tp) and Power Consumption (Pd) of One-Digit SWS-FET QMC.

	INV	NAND2	NOR2	NAND3	NAND4	GT	EQ	Circuit1	Circuit2
tp (ps)	26	30	45	51	65	83	95	60	130
tp (FO4)	0.27	0.32	0.47	0.54	0.68	0.87	1	0.63	1.37
Pd (μW)	6.7	13.4	16.5	21.4	28.1	37.2	42.3	53.6	132.5
Pd (μW/MHz)	1.34	2.68	3.3	4.28	5.62	7.44	8.46	10.72	26.5

Table 14: Total Propagation Delay (tp) and Power Consumption (Pd) of m-Digit SWS-FET QMC.

m (digits)	1	2	4	8	16	32	64	128	256	512
Bit n=m*2	2	4	8	16	32	64	128	256	512	1024
TC	31	74	150	312	626	1,264	2,530	5,072	10,146	20,288
tp (ns)	0.14	0.2	0.27	0.33	0.4	0.46	0.53	0.59	0.66	0.72
tp (FO4)	1.47	2.11	2.84	3.47	4.21	4.84	5.58	6.21	6.95	7.58
Pd (mW)	0.096	0.229	0.467	0.971	1.95	3.94	7.89	15.82	31.64	63.33
Pd (μW/MhZ)	0.019	0.045	0.093	0.194	0.39	0.788	1.58	3.16	6.33	12.67
Result source	Direct simulation			Estimated analytically using Eqs. (11)-(18)						

Discussion

Functional Verification

The transient analysis of the one-digit SWS-FET QMC shown in Figure 13 verifies stable multi-level switching for all relational outputs (GT, EQ, LT, LT_NOR). Each output transitions correctly to logic level 3 (VDD = 1.2 V) when its corresponding condition is satisfied and returns to 0 V otherwise, confirming synchronized operation among all outputs. The clean waveform transitions and absence of level overlap demonstrate the robustness of SWS-FET logic under a 5 GHz excitation with a 1 fF load.

At the device level, the GT, EQ, and LT waveforms reach full quaternary levels, confirming precise control of intermediate conduction states through SWS-FET gating. The LT_NOR output, generated by the NOR combination of GT and EQ, exhibits minor transient glitches due to NOR-stage switching but maintains correct logical behavior.

Quantitatively, Table 13 summarizes the measured propagation delay (tp) and power dissipation (Pd) of all elementary gates and QMC building blocks. The one-digit QMC composite GT and EQ networks demonstrate total delays of approximately 140 ps (1.47 FO4). The total power dissipation equals 96 μW (≈ 0.019 μW/MHz at 5 GHz). The proposed SWS-FET QMC achieves sub-nanosecond switching (tp = 0.14 ns) with only 31 transistors, confirming a substantial reduction in hardware overhead while improving speed and energy efficiency.

Extending the architecture to higher operand sizes, Table 14 reports simulated and estimated performance up to m = 512 digits (1024 bits). The delay increases linearly from 0.14 ns for m = 1 to 0.72 ns for m = 512, while total power scales proportionally with transistor count, reaching about 63 mW at 512 digits. The normalized Pd per MHz remains ≤ 13 μW/MHz, validating the efficiency of the hierarchical logic in maintaining low dynamic activity.

Figure 14 illustrates the relations among transistor count, delay, and power. The transistor count exhibits near-exponential growth due to cascading one-digit QMC units and m-QMC logic stages, averaging ≈ 39 transistors per digit. The propagation delay grows almost linearly, reflecting the predictable ripple-timing behavior of the hierarchical network. Power dissipation remains low for small operand widths and increases moderately for larger configurations, consistent with load-capacitance growth. These observations confirm that the proposed architecture achieves linear delay scalability and controlled power increase, proving its suitability for large-scale multivalued arithmetic systems implemented with SWS-FET technology.

Performance Analysis

The performance of the proposed SWS-FET-based QMC is evaluated using standard circuit-level metrics, including propagation delay (tp), power–delay product (PDP), and the figure of merit (FOM) is defined as

$$FOM = PDP \times TC = (tp \times Pd) \times TC \quad (19)$$

A comparative summary of recently reported 32-bit and 64-bit magnitude comparators is provided in Table 15.

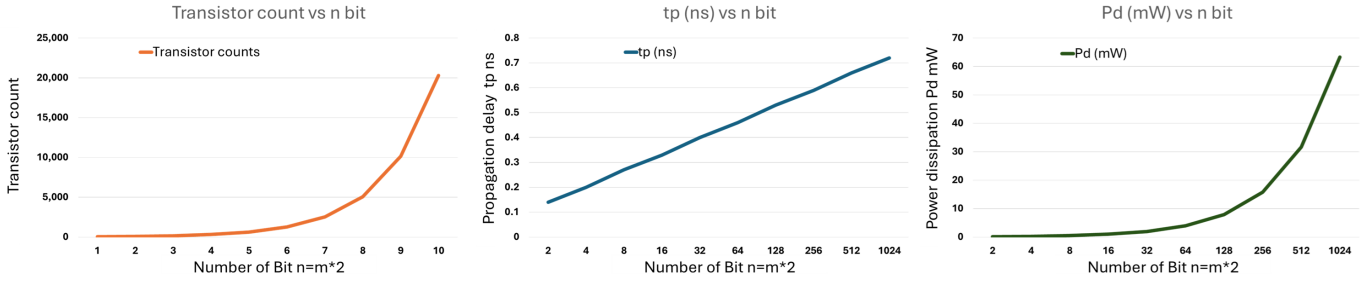

Fig. 14: Scaling of transistor count, delay, and power with operand size.

Table 15: Performance Comparison with Reported Magnitude Comparators.

Comparator, Technology/Power Supply	Bit	TC	Delay tp ns	Delay tp FO4	Pd μW/MHz	PDP fJ/MHz	FOM fJ/MHz
Kim et al.[38], 0.18 μm/1.8 V	32	964	1.12	18.6	12.6	14.11	13602
Tyagi et al.[39], 0.15 μm/1.5 V	64	1586	0.56	9.5	1.03	0.58	919.9
Hafeez et al.[40], 0.18 μm/1.8 V	64	4000	0.86	17.2	7.76	6.67	26680
Chua et al.[41], 0.18 μm/1.8 V	64	1875	0.88	14.7	19	16.72	31350
Proposed SWS-QMC, *m* = 16 digit	32	626	0.4	4.21	0.39	0.16	100.2
Proposed SWS-QMC, *m* = 32 digit	64	1,264	0.46	4.84	0.788	0.36	455

The proposed SWS-FET comparator achieves the lowest FO4-normalized delay among all CMOS-based designs reported in Ref.[38-41] It also exhibits significantly reduced power dissipation and a lower transistor count (1,264 devices for a 64-bit implementation), making it a more area-efficient alternative to conventional architectures.

Overall, the multi-flag SWS-FET QMC delivers simultaneous improvements in speed, power, and scalability. Its fast switching behavior, low-power operation, and compact device footprint demonstrate the advantages of SWS-FET technology as an energy-efficient and area-optimized platform for both binary and MVL comparators. These results confirm its potential for integration into low-power datapaths and arithmetic processing units.

Limitations and Comparison Assumptions

It is important to note that direct quantitative comparisons across different transistor technologies are inherently limited by differences in device physics, technology nodes, supply voltages, compact models, and simulation assumptions. Although FO4-normalized delay and frequency-normalized power metrics are employed to mitigate these disparities, the comparative results should be interpreted as indicative of architectural efficiency and scalability rather than as absolute cross-technology performance benchmarks.

Additionally, the presented results are obtained from simulation-based evaluation using compact SWS-FET models. Effects related to fabrication variability, interconnect parasitics, temperature variation, and layout-dependent constraints are not explicitly considered and may influence real-world implementations.

Conclusion and Future Work

This work introduced and validated an SWS-FET-based QMC that operates directly on four logic levels and provides independent GT, EQ, and LT flags. Device-accurate simulations confirmed clean multi-level switching and correct functionality at 5 GHz for the one-digit unit. The hierarchical extension preserves simple timing behavior: the critical-path delay increases almost linearly with the number of digits, and the normalized power per MHz remains low because only a small fraction of devices switch per cycle. At 64 bits, the proposed QMC achieves 0.46 ns delay at 4.84 FO4 with 1,264 transistors and 0.79 μW/MHz, outperforming contemporary 0.18 μm CMOS comparators in FO4 delay, PDP, and device count. These gains stem from native multi-state SWS-FET operation and a NAND-centric realization that shortens logic depth and reduces effective loading. The results demonstrate that SWS-FETs can deliver practical speed, low power, and compact area for multivalued arithmetic, supporting near-term integration of MVL into low-power datapaths.

Future Work: Technology scaling and system-level integration will focus on migrating the SWS-FET QMC to sub-90 nm nodes (e.g., 65 nm, 40 nm, 28 nm, and below), recharacterizing device and interconnect parasitics,

supply scaling, and variability to achieve lower FO4 delay and energy per operation. Integration into larger arithmetic and datapath subsystems will also be pursued to assess full-chip performance and scalability in practical system-on-chip environments.

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AI Use Disclosure

The authors used ChatGPT 5.1 (OpenAI) for language editing under human supervision. All technical content, results, and circuit designs are solely the responsibility of the authors.

Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this manuscript.

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