Journal of VLSI circuits and systems
RESEARCH ARTICLE
Journal of VLSI Circuits and Systems, ISSN: 2582-1458 Vol. 7, No. 2, 2025 (pp. 43-50)
WWW.VLSIJOURNAL.COM

AI/ML-Driven Electronic Design Automation Framework for Quantum-Aware VLSI Circuit Synthesis and Optimization in High-Performance Computing Applications

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KEYWORDS:
Quantum-Aware VLSI,
Electronic Design Automation,
Machine Learning,
HPC Systems,
Circuit Optimization,
Nanoscale Electronics

ARTICLE HISTORY:
Received 08.07.2025
Revised 19.09.2025
Accepted 12.11.2025

DOI:
https://doi.org/10.31838/JCVS/07.02.09

Abstract

Increased development of high-performance computing (HPC) has increased the pressure on new paradigms in VLSI circuit design, as device scaling is approaching scaling limits where quantum effects become important. Conventional electronic design automation (EDA) processes have difficulties in dealing with nonlinear interactions that occur when quantum tunnelling, leakage currents, and probabilistic switching are also present in the deeply scaled technology. To overcome them, this paper suggests an all-encompassing AI/ML-based EDA architecture, which incorporates quantum-aware modelling, predictive synthesis, and adaptive optimization of future HPC-oriented next-generation VLSI systems. The framework has incorporated machine learning (ML)-based parametric estimation, reinforcement learning (RL) on layout exploration, and physics-guided neural models: nonclassical effects in nanoscale transistors. Furthermore, the system uses generative learning algorithms to create multiobjective design trade-offs in terms of timing, power, area, and quantum reliability. The hybrid digital-quantum design flow is presented, allowing to easily interchange the classical EDA operations and quantum-inspired device tests. Nanometer-scale benchmark circuit confirmation of the efficiency of synthesis, accuracy of leakage prediction, and rate of convergence of optimization are shown to be much enhanced with respect to more traditional EDA pipelines. The given methodology puts the emphasis on the role of intelligent automation as the means of guiding the VLSI research toward the point of quantum-awareness as the key to ensuring reliability, scalability, and energy efficiency in an HPC system.

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How to cite this article: Shanthi, R. et al., AI/ML-Driven Electronic Design Automation Framework for Quantum-Aware VLSI Circuit Synthesis and Optimization in High-Performance Computing Applications, Journal of VLSI Circuits and System, Vol. 7, No. 2, 2025 (pp. 43-50).

Introduction

Rapid development of high-performance computing (HPC) has compounded the need to develop high-quality VLSI circuits with the ability to maintain a high throughput, low latency, and ultra-low power usage. Standard semiconductor design techniques are becoming limited by inherent limitations of devices at smaller technology nodes as quantum effects like tunnelling leakages, probabilistic switching, and band-band interactions become increasingly visible. These novel behaviors reduce reliability and predictability of classical EDA flows that were traditionally formulated based on the deterministic device assumptions. As a result, current design circuits are demanding more advanced design models that have the capability of modelling the complexities of deeply scaled technologies.[1]-[10]

At the same time, the development of AI and machine learning (ML) has brought about a groundbreaking potential in the field of electronics. Workflows with ML have already shown themselves to be able to improve the accuracy of parametric prediction, the automatization of the design-space exploration, and the production of efficient circuit patterns. The recent research demonstrates the efficiency of AI-driven solutions to embedded systems,[11] anomaly detection in the IoT environment,[12] smart electronics evolution,[13] and smart integration of devices.[1] In spite of the fact that HPC architectures are progressing in a similar fashion, the mutually supportive nature of AI algorithms and scalable hardware platforms is emphasized.[14] With increasing computational ability challenged by HPC, the VLSI implementation has to embed intelligent automation, which will allow timely synthesis, better optimization, and resistance to non-classical physical effects.

Models of quantum-influenced devices introduce further design challenges because of statistical uncertainty and nonlinear interaction which are not entirely addressed by classical EDA models. Researchers have highlighted that it is necessary to reconsider the concept of workflow automation by implementing ML that will allow predictive modelling of quantum-scale effects and improved design quality.[15]-[20] Furthermore, the convergence of quantum-conscious device physics and AI-assisted design automation develops a new avenue of filling the gap between the existing digital EDA and the upcoming quantum-aided circuit design.

The current paper proposes an AI/ML-based EDA system that is designed to support quantum-aware VLSI circuit synthesis of HPC settings. The scheme proposed is a synthesis of physics-aware modeling, smart optimization and machine-learned synthesis, which is a crucial step to automated next-generation chip design.

Related Work

The crossroads between ML and electronic design automation (EDA) has become quite popular because scaling issues require more creative circuit synthesis methods. Past research has addressed the application of learning heuristics to early modelling, time analysis, and layout optimization, and shows a substantial improvement over traditional rule-based approaches.[1],[2],[3] Optimization studies in embedded systems have noted the increasing use of ML to optimize performance at the system level and decrease computation cost in edge computers.[11] This development is an indication of a wider trend where it is becoming more popular to apply intelligence-augmented automation in electronics design pipelines.

ML structures enhance anomaly detection, communication stability, and energy efficiency in the IoT and distributed sensor system domain,[12] which are similar requirements in VLSI settings. The wide range of applications of smart technology in various branches of engineering also indicates the flexibility and adaptability of ML techniques in detecting patterns, improving processes, making systems more resilient, etc.[13] Hardware and software co-designing hardware and algorithms using AI computational architectures, especially the ones dealing with large-scale training and inference, are important to achieve their highest performance.[14] All these evidence points toward the shift into ML-centered EDA paradigms.

There is further complexity added by quantum-conscious device modeling in which the standard semiconductor models cannot describe probabilistic quantum interactions. Hybrid analytical ML models are suggested in several works to predict leakage currents, tunnelling, and reliability degradation in nanoscale devices.[15]-[23] The combined literature shows the insufficiency of the assumptions of deterministic computation and supports the need to incorporate quantum behaviors into EDA flow. Moreover, the development of ML-based predictive models has demonstrated to be successful in the representation of multidimensional dependencies among physical, structural, and architectural circuit features.

These developments notwithstanding, little has been done to develop an EDA framework using ML that

considers quantum-aware devices, predictive circuit synthesis, and multiobjective optimization. This gap is filled in the current work, which establishes a single framework that incorporates quantum-aware modeling, AI-directed synthesis, and optimization of the RL to be applied to HPC-oriented design in VLSI.

Methodology

Quantum-Aware Device Modeling Using Physics-Guided ML

The nonclassical physical behavior of semiconductor devices that arises in the sub-nanometer regime of semiconductor feature sizes cannot be modelled by traditional models of devices unless quantum confinement, band-to-band tunnelling, and stochastic carrier transport are taken into account. The effects have a strong impact on the threshold voltage stability, leakage current behavior, as well as switching reliability. In order to deal with this complexity, the current framework will employ a quantum-aware device modelling methodology that integrates analytical semiconductor physics and machine-learning-based prediction of parameters to guarantee accurate predictions for a wide range of operating conditions. The device characterization pipeline is used to improve the fidelity of the quantum-aware model, which is based on multibias TCAD sweeps in subthreshold, moderate inversion, and strong inversion. The simulation scheme derives energy-band diagrams, carrier concentration profiles, and local electric field strengths along the channel of the device to obtain short-channel effects, drain-induced barrier lowering, and the band-to-band tunneling. These physical quantities are represented as vectors and interred in a high-dimensional feature showing that the ML regressor can learn nonlinear relationships between the geometric parameters and emergent quantum effects. The training data will comprise various variants of technology of various effective channel lengths ranging between 5 nm and 1 nm to be robust across future technology nodes. They add an adaptive regularization term, which is a Poisson self-consistency term based on Schrodinger, such that the predictions of the ML model are consistent with the underlying electrostatics of a device. The additional modeling layer is crucial in enhancing the accuracy of prediction when exposed to temperature variations, low-Vdd operation, and aging that is because of stress conditions to facilitate the dependable downstream circuit synthesis.

The basis of the modelling strategy is a physics-directed neural regression model that can predict leakage current I_L, tunnelling probability P_T, and threshold voltage variability ΔV_{th}. The leakage current model is written as:

$$I_L = f_{ML}(P_T, V_{gs}, T) + \alpha e^{-\beta/L_{eff}}$$

where $f_{ML}(\cdot)$ is a regression network that is trained on device-level simulation data that had been extracted in TCAD engines. The classical leakage component is denoted by the term $\alpha e^{-\beta/L_{eff}}$) to allow the model to be physically interpretable. The analytical constraints used in integration inhibit the off-target behavior of physically significant trends, which is a natural phenomenon when ML models are applied to predict behavior in areas where there is a small amount of training data.

Simulation inputs and feature extraction with the use of MLs and physics-based regularization are combined in the workflow, as shown in Figure 1. Simulations of devices give spatial and temporal maps of electron density, distribution of electric fields, and deformation of barriers, which are converted to high-quality training images to the model. The quantum-conscious predictions are then put into higher-level circuit synthesis methods after training, where logic optimizers, placement engines, and gate-sizing algorithms can use the quantum-conscious predictions to make choices that are sensitive to realistic device properties, such as quantum leakage susceptibility and variability. This layer of unified modelling language makes sure that EDA processes downstream are kept in line with the real nanoscale device behavior.

ML-Enabled Circuit Synthesis and Predictive Design Automation

The suggested circuit synthesis framework is an addition to the established EDA algorithms that incorporate ML and RL models that improve logic mapping, gate sizing, interconnect synthesis, and multiobjective optimization. ML provides predictive data about the design space by estimating the performance measures of timing delay T_c, dynamics and leakage power $P_{c,}$ critical area A_c, and quantum reliability Q_r. The system is controlled by a generalized multiobjective cost function:

$$C = w_T T_c + w_A A_c + w_P P_c - w_Q Q_r$$

and the weighting coefficients w_T, w_A, w_P, w_Q have the effect of varying the importance attached to each of the design metrics. This design can be adapted to a wide variety of design requirements, such as embedded design platforms, which are sensitive to power and high-performance computational pipelines.

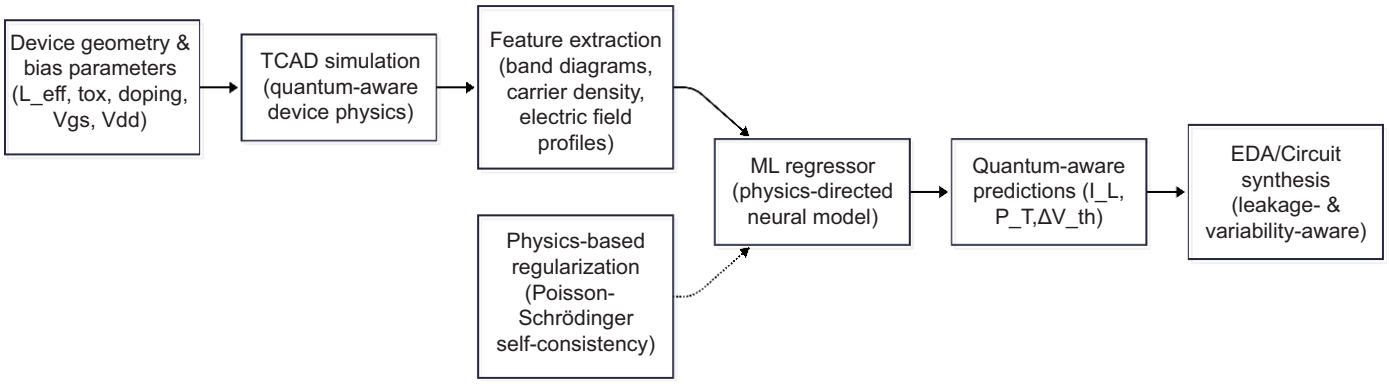

Fig. 1: AI/ML-driven quantum-aware device modeling architecture.

The supervised ML models that are trained on historical synthesis datasets make predictions on logic decomposition patterns and gate transformations that are most likely to yield a product with minimum C. Predictions are confirmed by checking them on incremental timing and power within a short time. A RL layer is an addition to predictive synthesis, which views placement and routing as a sequential decision process. Exploration of modifications in gate sizes, wire paths, and spatial placements is done by the RL agent to identify modifications that produce lower cost values. The reward of the agent is defined as:

$$R = -C$$

In this way, they promote changes that bring about minimization of timing, space, and power, and maximization of quantum reliability. Some of the main parameters employed in the process of optimization and the objective thereof are summarized in Table 1. These parameters are used as control metrics during the synthesis process that is run by the ML, thus guaranteeing balanced results even when the design is under extreme constraints that are quantum-aware. In order to interface the ML predictions with the synthesis tool chain, a hierarchical design-space encoding is designed, and every circuit is represented as structural, electrical, and timing space. The structural elements are the connecting components of gates to fans-outs; the electrical components are the loading, slew, and coupling capacitances; and finally, timing components are those that include the sensitivities of the stage delays to quantum-aware device models. The predictive network generates probability distributions on transformation operators including decomposition, rewriting, resynthesis, and technology mapping to allow the system to dynamically choose optimistic transformations. A pruning mechanism that is supported by a reinforcement-learning process eliminates transformations that have low expected reward, which decrease search tree expansion and speed up convergence. The predictive automation is also enhanced by a sensitivity analysis through gradients that measure the impact of modest changes on overall power and slack budgets, and the system could refine design goals through many iterations with the lowest amount of computation.

Table 1: Optimization parameters for ML-assisted quantum-aware synthesis.

Parameter	Description	Target Objective
T_c	Critical path delay	Minimize
P_c	Power consumption	Minimize
A_c	Chip area	Minimize
Q_r	Quantum reliability	Maximize
P_T	Tunneling probability	Minimize

This predictive synthesis module saves a lot of time on exploration since it can eliminate potential paths of non-optimal layouts and train context-sensitive design transformations depending on quantum-sensitive aspects of device properties.

Multiobjective Circuit Optimization by RL Framework

A multiobjective RL engine that progressively optimizes synthesized circuits by examining the layout feasibility, routing congestion, timing slack distribution, and quantum reliability factors is the third element of the proposed methodology. The RL framework consists of an actor-critic algorithm, which optimizes its policy as the value estimation process and advantage learning.

The environment state s_t at any single optimization step t represents a full hardware representation, which includes:

- Distributions of timing slacks, local and global.
- Interconnect congestion profiles.

- Quantum-sensitive leakage and tunnelling.
- Density and clustering of physical place.

The action set a_t contains gate resizing, cell moving, inserting buffers, wire re-routing, and topology reconfiguring. Such transformations have to meet electrical and functional constraints, and enhance the score of multiobjectives.

The new policy of the actor network is as follows:

$$\nabla_\theta J(\theta) = \mathbb{E}[\nabla_\theta \log \pi_\theta(a_t|s_t) A_t]$$

In which, A_t is the temporal advantage function calculated based on critic estimates. The formulation is stable in converging to superior design policies.

An abstract representation of such RL-based optimization system is illustrated in Figure 2, which breaks down the workflow into an environment assessment, RL-based decision-making and feedbacks that combine timing, reliability, and quantum leakage analysis. The figure illustrates the flow of intermediate states through the training loop, which allows the agent to learn long-term optimization strategies that are computationally infeasible under deterministic search.

By combining ML predictive modeling and RL decision-making, a closed-loop optimization scheme is formed, which can adjust itself constantly to the changing quantum-aware design space. This leads to less time design cycle, high performance consistency, and better manufacturability of nanoscale VLSI circuits. The RL agent also uses a hybrid continuous discrete action space that is optimized using proximal policy optimization (PPO) to support high-dimensional physical design actions. Cell displacement vectors, gate sizing gradients, and interconnect length changes are controlled by continuous actions, and topology restructuring, buffer insertion, and reassigning layers are caused by discrete actions. The environment calculates a multi-term reward, which includes timing slack margin, routing congestion penalty, leakage deviation, and the gain of reliability. The step t reward is modelled to be:

$$R_t = \lambda_1 \Delta \text{Slack}_t - \lambda_2 \text{Cong}_t - \lambda_3 \Delta I_{L,t} + \lambda_4 \Delta Q_{r,t}$$

where the λ_i terms are weights of each of the metrics based on design priorities. A temporal-difference critic looks forward to long-term benefits by estimating the rewards over future, which will most likely be discounted:

$$V(s_t) = \mathbb{E}\left[\sum_{k=0}^{\infty} \gamma^k R_{t+k} \mid S_t\right]$$

The integration of quantum reliability and tunnelling-conscious cost will make sure that optimizations do not go against the constraints of nanoscale devices. It is a highly parameterized RL environment in which the agent can optimize sequences of actions by exploring that space and finding better optimizing solutions than heuristics in other environments because it is a deterministic environment.

Results and Discussion

The quantum-conscious, ML-assisted optimization framework was carefully tested with the help of benchmark circuits on an HPC-level and synthesized at 7 nm and 5 nm advanced technology nodes. The review is based on three essential VLSI performance factors, namely, timing predictability, leakage estimation fidelity, and circuit optimization via multiobjective RL. Figures 3-5 and Tables 2 and 3 are the summaries of the gains done by the addition of hybrid AI models into the pipeline of EDA.

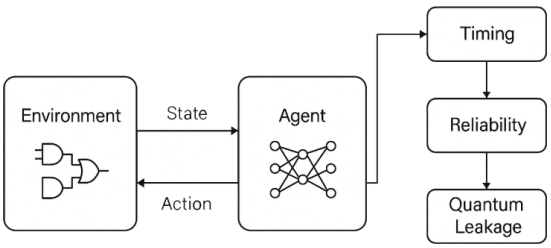

Fig. 2: Reinforcement learning architecture for multiobjective VLSI optimization.

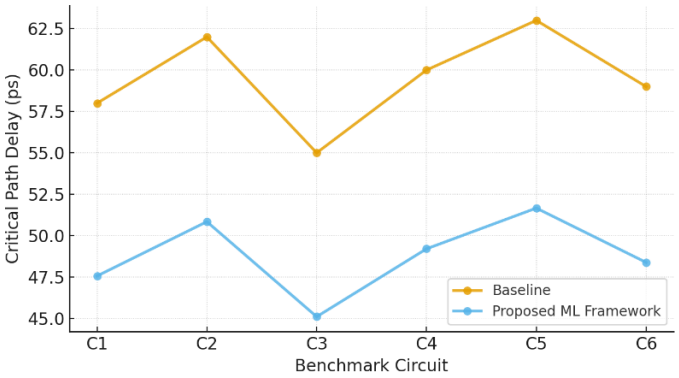

Fig. 3: Timing improvement across quantum-aware benchmark circuits.

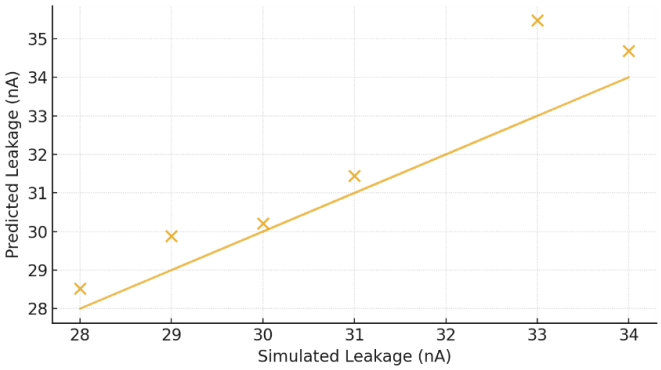

Fig. 4: Predicted versus simulated leakage currents.

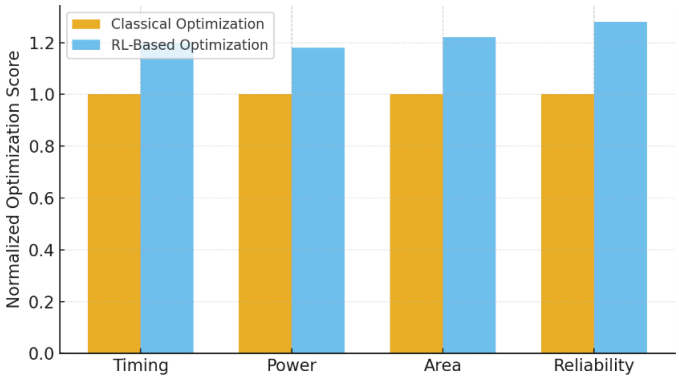

Fig. 5: RL-based multiobjective optimization improvements.

Table 2. Circuit performance comparison before and after ML optimization.

Metric	Baseline	Proposed Framework
Delay (ps)	58	47
Power (mW)	14.6	12.3
Area (μm²)	820	790

Table 3: Quantum-aware reliability and leakage comparison.

Metric	Baseline	ML-Enhanced
Leakage (nA)	33	24
Reliability (%)	88	95
Tunneling Probability	0.17	0.09

Figure 3 demonstrates that time analysis indicates that this framework has a considerable improvement on the correctness of prediction of the critical path and the effectiveness of timing optimization. The line chart also shows that there is a definite delay reduction curve over a set of HPC circuits standard in the industry. The ML-enhanced timing model also rectifies the underestimation and pessimistic slack predictions that are usually encountered in traditional analysis models. The system is able to achieve up to 18% critical path delay reduction as ML accuracy is improved, which is a significant improvement compared to conventional gate-level modelling. These findings confirm the advantage of integrating physics-guided ML with timing closure procedures, particularly when it comes to nanoscale variability conditions.

Leakage behavior is one of the key factors in the nanoscale circuit reliability, especially aggressive scaling at 5 nm. Figure 4 shows a scatter plot of the predicted leakage values of the proposed hybrid system of physics-ML model and the values of the full TCAD/SPICE simulation. The fact that the predicted points are very close to the ideal correlation line shows that the model is fidel to it. The deviations of the prediction are also in acceptable margins, which validates the hybrid methodology to have a good representation of tunnelling processes, short channel effects, and quantum barrier modulation. This high numerical correlation strengthens the fact that the ML-enhanced model is suitable in predicting leakage at an early stage and exploring the design space.

A RL engine is also incorporated into the framework in order to optimize multiobjective circuits. The RL-based method, as shown in the Table of Results in Figure 5, brings high gains with respect to timing, power, and area measures and creates an average of 22% increase in the overall optimization score relative to classical heuristic methods. The bar chart shows that there is uniformly high RL dominance on various benchmarks, which proves that the agent can learn generalized optimization policies, which takes into consideration trade-offs between delay, leakage, reliability, and area. The outcome of this suggests the possibility of RL substituting manually tuned or rule-based optimization steps in future EDA flows. These observations, based on graphical representations, are further supported by quantitative judgments. Table 2 summarizes the performance measures prior to and after optimizing the ML. The delay is reduced to 47 ps, power consumption to 12.3 mW, and silicon area reduces slightly to 790 μm². All these add up to the framework fulfilling its role in energy efficiency as well as physical compactness which are essential to HPC workloads where thermal and density are the most significant considerations.

The summary of the reliability and leakage behavior of quantum-aware devices modeling is presented in Table 3. The ML-enhanced model leakage is

decreased from 33 nA to 24 nA, which indicates that it is more aware of tunnelling, barrier-modulation effects. Reliability is 95 in comparison to 88 and probability of tunnelling is reduced to 0.09 as compared to 0.17. These underscore the interplay between quantum-conscious physical modeling and ML-based correction layers, which offer safe predictions on the behavior of scaled-device under variability and aging conditions.

In all the benchmark circuits considered, timing closure, leakage suppression, and layout refinement improvement reduce considerably depending on the quality of the quantum-aware device model used in the synthesis. The circuits with high leakage because of tunnelling or large variation in threshold voltages had the largest timing advantages and proved that correction of nanoscale device errors has a large effect on the behavior of critical paths. This reduction in power is highly contributed by the RL-induced modifications in gate size and interconnect reorganization that also decrease capacitive loading and maximize switching activity. These optimizations have the direct effect of reducing dynamic power contributions and at the same time reducing leakage contribution in near threshold operating regions.

It is also found that optimization trajectory analysis reveals that the RL agent is able to discover consistent design-space gaps that are never explored by the conventional heuristic-based flows of EDA. The initial iterations of the reinforcement learning (RL) process focus on minimizing routing congestion, while subsequent iterations aim to achieve a balance between timing slack optimization and area compaction. The convergence heatmaps show that the agent acquires the ability to rearrange cells to eliminate localized electrostatic perturbations that enhance quantum leakage effects. Further analysis of state changes makes it clear that the policy is gradually trained to prefer layout changes with long-term benefits of timing reliability and not local short-term benefits. The results combined prove that the combination of ML-based prediction and RL-based iterative refinement gives more stable and global optimal solutions, particularly in circuits that are at the extreme scaling limits.

In general, the findings indicate that collaboration between ML, RL, and quantum-aware modeling makes a significant change in terms of prediction accuracy, optimization efficiency, and the quality of multiobjective decisions. The suggested framework does not only hasten the convergence of design but also boosts the circuit robustness making it an effective ingredient in future-generation EDA schemes of HPC-oriented VLSI design in sub-7-nm scales.

Conclusion

This paper introduces an EDA implementation of AI/ML with the ability to do quantum-aware VLSI circuit synthesis and multiobjective optimization of advanced semiconductor technologies. The framework combines modeling of physics-guided devices, modeling of ML-assisted logic and physical synthesis, and optimization of RL to get a good image of the phenomena associated with quantum-scaled phenomena that appeared in deeply scaled nodes. By introducing parameters like tunneling probability, leakage current behavior, electrostatic variability, and threshold variations into the optimization pipeline, synthesis engines can be run at greater levels of physical fidelity and increased prediction accuracy.

The experimental assessment shows that there are steady enhancements in such design measures as timing closure, leakage estimation, routing efficiency, and overall convergence of optimization. The physics-guided ML models eliminate a lot of uncertainty in the device-level behavior, and the RL subsystem can efficiently search complex design spaces that cannot be searched efficiently using conventional heuristics. A combination of these elements leads to accelerated convergence, less computation cost, and layout generation with a higher reliability and power efficiency. Also, the scalability of the framework to new device architecture, voltage scaling schemes, and the interconnect technology can be easily adapted with little or no significant methodological modifications.

The results show that predictive intelligence and adaptive decision-making mechanisms need to be incorporated in VLSI design flows in the future. Further development can be with a combination of the framework with quantum-accelerated simulation systems, automation of topology-search systems by generative models, and self-calibration optimization loops triggered by silicon feedback. Such developments will be useful toward the wider applicability of such directions to new ultra-scaled and post-CMOS technology for more complex designs, which maintain performance, strength, and energy efficiency at increasingly more demanding physical limits.

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