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VLSI Circuits-Oriented Gate-Length-Dependent DC–RF Compact Modeling of AlInN/AlN/GaN MISHEMTs with SSEC Extraction

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Abstract

This work develops a compact analytical DC-RF model based on VLSI-circuit design that accounts for gate-length scaling impacts in RF circuit designs using AlInN/AlN/GaN MISHEMTs. In order to effectively simulate the drain current density, transconductance, and the gate charge for use in simulating RF and microwaves circuits using technology, a two-dimensional electron gas (2D) sheet-charge-based formulation has been developed to account for flat-band voltage and polarization charge impacts. This model was validated with both TCAD simulations and experimental data for a range of gate lengths (from 0.1 to 0.3 µm), resulting in a maximum drain current density of 2.35 A/mm and an estimated cut of frequency of 125 GHz when the gate length was 0.1 µm. In addition, a refined small-signal equivalent circuit extraction methodology, integrating conventional and gradient-based optimization techniques, is introduced to improve parasitic de-embedding accuracy. Extracted S-parameters enable robust frequency-domain characterization, yielding f_T = 170 GHz and f_{max} = 183 GHz. The proposed compact model demonstrates scalable, bias-consistent DC, and RF prediction, making it well-suited for VLSI RF and microwave circuit design and simulation using GaN MISHEMT technologies.

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Introduction

GaN-based MISHEMTs are used with increasing frequency in VLSI RF and hybrid (mixed signal) circuits because they provide a high breakdown voltage, an extremely high electron mobility, and an even higher power handling capability than other semiconductor devices.[1] Therefore, it is necessary to accurately predict how these devices will behave under DC bias conditions and RF small-signal conditions at different gate length scales to assure reliability in terms of gain, stability, and power consumption efficiency.[2] Galium Nitride (GaN) has been found to be an important wide bandgap semiconductor because of its many good physical properties. High electron mobility, high thermal conductivity, large breakdown field, and high saturation velocity are some of those good properties that contribute to GaN being an appropriate material to build GaN-based devices to use in higher power and frequency applications.[3] The most notable advantage of MOSHEMTs compared to traditional HEMTs is significantly reduced gate leakage and lower gate capacitance from using very high quality dielectric layers including Al_2O_3, Si_3N_4, HfO_2, SiO_2, and La_2O_3.[4-6]

Recently, AlInN/GaN heterostructures have emerged as promising alternatives to conventional GaN/AlGaN systems.[7] AlInN provides near-lattice matching with GaN, high spontaneous-polarization (SP) charge, and reduced

strain, permitting the use of thinner barriers and 2D-EG density in the channel. Devices with optimized Al content (≈83% in AlInN and ≈30% in AlGaN) exhibit enhanced 2D-EG mobility due to minimized alloy disorder scattering and reduced wavefunction penetration.[8-10] Gate length scaling has been extensively explored to achieve millimeter-wave and submillimeter-wave operation, with reported cut-off frequencies (f_T) exceeding 300 GHz for gate lengths down to 30 nm. However, aggressive scaling introduces short-channel effects, requiring careful optimization of the aspect ratio and device geometry. Despite the technological progress, comprehensive models capturing both DC and higher-frequency performance of AlInN and AlGaN-based MOSHEMTs remain limited.[11,12] Accurate SSEC modeling is essential for the circuits of monolithic microwave integrated circuits with amplifiers, mixers, and oscillators.[7] SSEC models enable parameter extraction, device characterization, and the development of large signal, noise models, using only DC and S-parameter measurements. Conventional extraction techniques, however, often suffer from error accumulation during de-embedding, and nonquasistatic effects become increasingly relevant at millimeter and microwave frequencies.[13]

To address these challenges, this work presents an analytical and efficient modeling approach for gate length-dependent DC as well as RF performance of AlInN/AlN/GaN MISHEMTs, along with a robust SSEC parameter extraction methodology. The proposed method combines physics-based TCAD simulations with gradient-based optimization to extract intrinsic and extrinsic parameters from *Y*- and *Z*-parameter analyses. The inclusion of intrinsic gate–drain resistance (R_{gd}) ensures accurate representation of the nonzero real part of Y_{12}, improving the prediction of key RF figures of merit. The extracted parameters are optimized using a least-squares fitting approach, offering improved accuracy and reduced computational time compared to conventional averaging methods.[14-17]

Most current DC/RF compact models have been developed using gate lengths that are either fixed or fitted empirically with parameter values that lose their physical meaning when scaled by gate length. The resulting errors in prediction of transconductance, output conductance, and parasitic capacitance as frequency increases can lead to untrustworthy gains and stability margins in circuit level simulation.

Uncertainty related to these limitations impacts the uncertainty of how circuit design will function, specifically regarding the estimation of cut-off frequency (f_T), the highest possible frequency of oscillations (f_{max}) and metrics that reflect the efficiency of a circuit depending upon bias conditions. Thus, RF circuit designers are generally required to either use excessive margins of safety within their designs and/or perform multiple iterations of postlayout tuning, ultimately resulting in increased design time and reduced predictability of the performance characteristics of VLSI circuits.[18-20]

This study will provide a solution to the above-mentioned difficulties through developing a gate length-dependent DC-RF compact model of the AlInN/AlN/GaN MISHEMTs, using the SSEC method as well as systematic approach for source series and extrinsic capacitance extraction. The new analytical methodology presented here has consistent gate length scalable parameters and does not compromise on the model accuracy at RF frequencies; this provides a good basis for the accurate simulation of gain, stability, and efficiency of the circuits.[21]

The main contribution of the work is as follows:

1. We developed a gate length dependent DC-RF compact model for AlInN/AlN/GaN MISHEMTs that allows for consistent parameter scalability across different gate lengths while improving both the DC and RF modeling accuracy.
2. A SSEC extraction technique to enhance the frequency prediction capability and provide an accurate description of parasitic effects impacting f_T and *f*max.
3. An additional advantage of this formulation is its ability to ensure a robust convergence during circuit-level simulation thus reducing bias-dependent discontinuities typically present in existing compact models.

Overall, we demonstrated a significant improvement in the correlation between their compact model and the measured DC characteristics and S-parameters. Thus, they provide more reliable predictions of gain, stability margin, and efficiency that are important to designers using these devices in VLSI RF circuits.

The rest of the paper is organized as follows: The design analysis was explained first, followed by the mathematical calculation. Later explains the proposed work with small-signal equivalent circuit (SSEC) model parameters extraction and the result analysis. Finally conclusion has been explained.

Design ANALYSIS

The device incorporates an AlInN or AlGaN barrier layer having a thickness ($t_{barrier}$) of 15 nm. Figure 1 illustrates

the multibarrier enhancement mode AlInN/AlN/AlInN/GaN/MISHEMT, and the corresponding band diagram (BD) is present in Figure 2. The advanced structure is engineered to leverage high electron mobility and thermal stability of Gallium Nitride (GaN), in combination with the favorable material properties of Aluminum Nitride (AlN) and Aluminum Indium Nitride (AlInN). The configuration is specifically designed to enhance routine in high-power, -frequency applications. The GaN channel, known for its wide-bandgap, great electron-mobility, and superior thrmal conductivity, helps as the prime electron transport-layer, making it appropriate for power and RF applications. On either side of the AlN spacer layer, AlInN multibarriers are employed to enhance the formation of a 2D-EG at the heterointerfaces, benefiting from AlInN's tunable bandgap and near-lattice-matching characteristics with GaN. The AlN spacer provides effective electrical isolation and contributes to a strong 2D-EG at the AlInN/GaN interface, thereby reducing gate leakage and improving device reliability.[22,23]

A recessed gate structure enables enhancement mode operation, which is critical for energy-efficient power electronics. Moreover, field-plate structures are used to prevent electric field crowding, improve breakdown voltage, decrease gate-to-drain capacitance (Cgd) which improves high voltage operation and stability of the whole device. Metal contact on drain and source is made low resistance to get better injection efficiency of current and therefore overall performance of the device is improved. The device was simulated by conducting

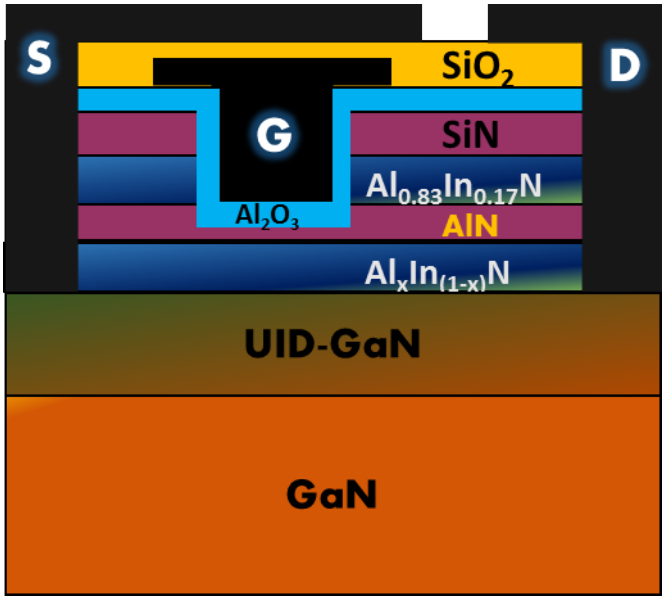

Fig. 1: The schematic outlook structure of AlInN/AlN/AlInN/GaN MISHEMT device.

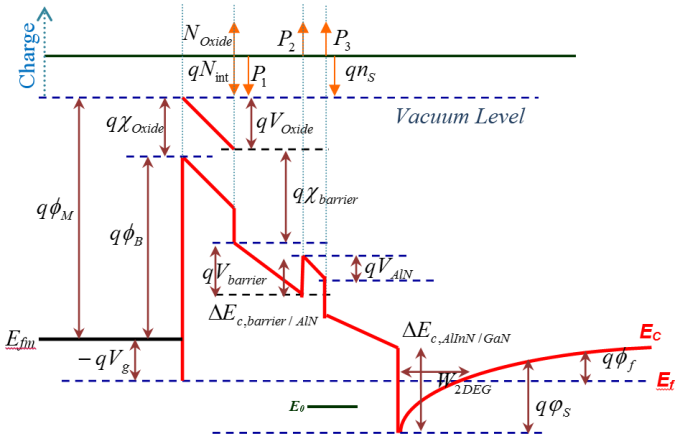

Fig. 2: Band gap diagram of SiO_2/AlInN/GaN/AlInN / MISHEMT and its charge distribution.

a series of detailed device simulations using TCAD simulator in order to determine the device parameters and S-parameter. The simulations employed the drift-diffusion model that utilizes the carrier continuity and Poisson's equations to study carrier transport through channel at 300K [24].

The Newton method was utilized for solving the model equations. A carefully optimized mesh, designed using the Deck-Build editor, ensured precise simulation of critical device regions while improving computational efficiency. The simulations included several physical models like:

CONMOB: concentration-dependent mobility, FLDMOB: electric field-dependent mobility, and CVT as an integrated model accounting for various mobility effects.[25] Additionally, the Fowler-Nordheim model was applied to simulate gate leakage current, while SRH and Auger models addressed recombination and generation phenomena. Trap effects were represented by integrating SRH recombination terms within the continuous equation. Obtained results were analyzed using the TonyPlot tool, and the export feature of Tony Plot was employed for extracting output data. Fixed oxide-charges of 9.71×10^{12} cm^{-2} for HfO_2 at the interface of oxide/semiconductor were considered, while polarization-charges of 2.74×10^{13} cm^{-2} were calculated and incorporated at the AlInN(AlGaN) interface.[26]

Mathematical Calculations

Flat Band Voltage (V_{FB})

Energy band alignment for proposed MISHEMT structure is illustrated in Figure 2. The flat band voltage shows a

paramount role in formative threshold and operational characteristics of the device, as it accounts for WF differences, polarization-induced charges, and potential drops across various hetero structure layers.

The potential equilibrium equation through the metal insulator semiconductor interface is expressed as:[27-29]

$$\phi_M + V_g = V_{Oxide} + \chi_{barrier} + V_{barrier} - \Delta E_{c,barrier/AlN} + V_{AlN} + \Delta E_{c,AlN/GaN} - \varphi_S + \phi_f \quad (1)$$

The work-function (WF) difference between channel and gate is given by

$$\phi_{MC} = \chi_{barrier} - \Delta E_{c,barrier/AlN} + \Delta E_{c,AlN/GaN} + \phi_f \quad (2)$$

From Eqs. (1) and (2), the relationship simplifies to:

$$\phi_{MC} + V_g = V_{Oxide} + V_{barrier} + V_{AlN} - \varphi_S \quad (3)$$

ϕ_{MC} = WF variance between channel ($\phi_{Channel}$) and gate metal (ϕ_M).
ΔE_c = conduction band discontinuity, ϕ_f = potential difference between E_c and E_f.
$V_{barrier}$ = Barrier layer voltage drip
$\chi_{barrier}$ = Electron affinity of AlGaN
V_g = Gate voltage
V_{Oxide} = Oxide voltage drop
φ_S = Surface potential of GaN layer
V_{AlN} = AlN layer voltage drip

The presence of inadvertent charges near the interface, along with polarization-induced charges, leads to potential drops across the oxide, barrier, and spacer layers. Taking into account the individual potential drops at each layer, the potential across the oxide layer can be expressed as

$$V_{Oxide} = P_1 . \frac{N_{Oxide} + N_{int}}{C_{Oxide}} \quad (4)$$

Here, the oxide capacitance per unit area is defined as, $C_{Oxide} = \varepsilon_0 . \varepsilon_{Oxide} / t_{Oxide}$ where ε_{Oxide} represents the oxide permittivity and t_{Oxide}: oxide thickness. The charge densities within the oxide and at the oxide/barrier interface are denoted as N_{Oxide} and N_{int}, respectively.

The corresponding potential drip across the barrier and AlN spacer layer is expressed as

$$V_{barrier} = \frac{\varepsilon_{barrier} t_{Oxide} + q . t_{barrier} \varepsilon_{Oxide}}{\varepsilon_{Oxide} . \varepsilon_{barrier}} P_2 \quad (5)$$

$$V_{AlN} = P_3 . \frac{q . t_{AlN} . \varepsilon_{barrier} . \varepsilon_{Oxide} + \varepsilon_{AlN} . t_{barrier} . \varepsilon_{Oxide} + \varepsilon_{AlN} . \varepsilon_{barrier} . t_{Oxide}}{\varepsilon_{barrier} . \varepsilon_{Oxide} . \varepsilon_{AlN} .} \quad (6)$$

Here, q = electronic charge,
$\varepsilon_{barrier}$ and ε_{AlN} = Permittivity of the AlGaN/AlInN and AlN layers,
P_3, P_2 and P_1 = complete polarization charges
$t_{barrier}$ and t_{AlN} = the thickness of the barrier and AlN layers.

Flat band form is achieved when device is entirely pinched off, affecting the surface potential to come to zero, i.e., when $V_g = V_{FB}$ and is expressed as

$$V_{FB} = P_1 . \frac{N_{Oxide} + N_{int}}{C_{Oxide}} + P_2 \frac{q . t_{barrier} \varepsilon_{Oxide} + \varepsilon_{barrier} t_{Oxide}}{\varepsilon_{Oxide} . \varepsilon_{barrier}} + P_3 \frac{q . t_{AlN} . \varepsilon_{barrier} . \varepsilon_{Oxide} + \varepsilon_{AlN} . t_{barrier} . \varepsilon_{Oxide} + \varepsilon_{AlN} . \varepsilon_{barrier} . t_{Oxide}}{\varepsilon_{Oxide} . \varepsilon_{barrier} . \varepsilon_{AlN} .} - \phi_{MC} \quad (7)$$

The complete polarization charge (P) at each stage is calculated by considering both piezoelectric polarization (P_{PE}) and spontaneous polarization (P_{SP}) of the adjacent layers (within the heterostructure [7] and the resulted polarization charge at an interface is expressed as:

$$P = P(\text{top}) - P(\text{bottom})$$

2D-EG Density Model

2D-EG density is a key determinant of MISHEMT performance, originating from polarization made charges at AlN/GaN interface. The conduction-band forms a triangular quantum well, where most electrons occupy the lowest sub-band near the bottom of the quantum well. As the well area widens toward the top, sub-band space decreases. To derive the 2D-EG density, a self-steady result of Schrodinger and Poisson equations using the WKB calculation is employed [28]. The relationship between E_f variation with (n_s) is expressed as

$$n_s = \sum_{k=0}^{\infty} V_T . \ln \left[\exp \left(\frac{E_f - E_k}{V_T} \right) + 1 \right] \text{DOS} \quad (8)$$

where
$E_k = A_k . n_s^{2/3}$ is k^{th} sub-band energy level
DOS = density-of-states,
V_T = threshold voltage
E_f: Fermi energy level,
k: Boltzmann's constant.

Considering polarization effects, the sheet-charge density can also be expressed via Poisson's equation:

$$n_s = P_3 . \frac{\varepsilon}{q.t}(V_{g0} - E_f) \tag{9}$$

where ε/t = Constant

$$V_{g0} = V_g - V_{FB} - V_p,$$

These nitride-centred designs are substantial for polarization properties and the polarization charge effect is integrated in V_{FB}.

In the *q*-well, only the lower sub-band energy level $E_0 = A_{k0}.n_s^{2/3}$ is concern for calculation and A_0 is the experimentally resolute parameter [29]. By seeing only the lowest sub-band energy term and negating higher order terms, Eq. (8) come to be

$$n_s = DOS.V_T . \ln\left[\exp\left(\frac{E_f - E_0}{V_T}\right) + 1\right]. \tag{10}$$

Equation (10) can also be rewritten as

$$\exp\left(\frac{n_s}{DOS.V_T}\right) = \exp\left(\frac{E_f - E_0}{V_T}\right) + 1 \tag{11}$$

To progress a unified 2D-EG charge density, a clear expression of E_f with V_g is necessary. Now relating Taylor's expansion calculation in Equation (10) and E_f can be estimated as

$$E_f \approx A_0 . n_s^{2/3} + V_T . \ln\left(\frac{n_s}{DOS.V_T}\right) \tag{12}$$

Now, Equation (9) is switched in Equation (12) to exclude *ns* and escalating right side of 2 positions to 1st in practice of E_f/V_{g0}, as

$$E_f = A_0\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3} - \frac{2}{3}A_0\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3}\frac{E_f}{V_{g0}} + \ln\left(\frac{\varepsilon.V_{g0}}{q.t.DOS.V_T}\right)V_T - V_T\frac{E_f}{V_{g0}} \tag{13}$$

And is rewritten as

$$E_f = V_{go}\frac{V_T \ln\left(\frac{\varepsilon.V_{g0}}{q.t.DOS.V_T}\right) + A_0\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3}}{V_{g0} + \frac{2}{3}A_0\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3} + V_T} \tag{14}$$

To accurately model the drain-current density and terminal charges, a unified 2D-EG model applicable across all operating point is essential. For this purpose, by substituting Equation (14) into Equation (9), an analytical aspect for n_s as a task of V_g is derived and expressed as

$$n_s = \frac{P_3.\varepsilon.V_{go}}{q.t}.\frac{V_{go} + V_T\left(1 - \ln\left(\frac{\varepsilon.V_{g0}}{q.t.DOS.V_T}\right)\right) - \frac{A_0}{3}\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3}}{V_{g0} + \frac{2}{3}A_0\left(\frac{\varepsilon.V_{g0}}{q.t}\right)^{2/3} + V_T} \tag{15}$$

Drain Current Model

The drain-current expression is formulated by incorporating the previously derived 2D-EG density model and is expressed as [13]:

$$I_d = \frac{W}{L_g}\int_{V_s}^{V_d} q.\mu_0 . n_s dV_p \tag{16}$$

The primary potential dV_p in Eq. (16) can be derivatived from Eq. (9) and related to Taylor-series calculation:

$$V_g - V_{FB} - V_p = \frac{q.t}{\varepsilon}.n_s + A_0 n_s^{2/3} + V_T . \ln\left(\frac{n_s}{DOS.V_T}\right) \tag{17}$$

V_p is differentiated with Eq. (17) w.r.t ns,

$$-dV_p = \frac{q.t}{\varepsilon}.dn_s + \frac{2}{3}A_0 n_s^{-1/3}.dn_s + \frac{V_T}{n_s}.dn_s \tag{18}$$

The drain-current can be derivative by switching Eq. (18) in Eq. (16) and integrated with source-drain to give:

$$I_d = \frac{q.W.\mu_0}{L_g}\left[\frac{q.t}{2\varepsilon}\left(n_s^2 - n_{s,S}^2\right) + \frac{2}{5}\left(n_s^{5/3} - n_{s,S}^{5/3}\right) + V_T\left(n_s - n_{s,S}\right)\right] \tag{19}$$

Besides, the g_m which outlines the current transport ability of the device to evaluate and microwave behaviour, which can considered by partialdifferentiable of the drain-current in Equation (19) w.r.t V_{gs} and gives $g_m = \partial I_{ds}/\partial V_{gs}$.

Gate Charge Centred Capacitance Design

The intrinsic gate charge is also defined using a unified sheet charge density model to express the *C*ds and *C*gs. Gate-to-channel charges are comprised of both the

oxide layer charge and the inversion layer charge. Total gate charge is found by integrating the 2DEG channel charge density over the area of the gated region:[21]

$$Q_g = -\int_0^{L_g} q.n_s.W\left(V_g, V_p\right)dx \tag{20}$$

The *dx* term of Equation (20) results from the Id in Equation (16) which gives

$$dx = \frac{q.n_s.W\left(V_g, V_p\right)dV_p}{I_d} \tag{21}$$

Now, solving *dx* by switching Equation (18) in Equation (21), and further switching Equation (21) in Equation (20) and integrating, we get

$$Q_g = \frac{\mu_0 (q.W)^2}{I_d}\left[\frac{q.t}{3\varepsilon}\left(n_s^3 - n_{s,S}^3\right) + \frac{1}{4}A_0\left(n_s^{8/3} - n_{s,S}^{8/3}\right) + \frac{V_T}{2}\left(n_s^2 - n_{s,S}^2\right)\right] \tag{22}$$

Now, C_{gd} and C_{gs} are solved from the partial differentiation of Equation (22) with drain and source voltages, respectively, and is expressed as $C_{gs} = (\partial Q_g)/(\partial V_s)$ and $C_{gd} = (\partial Q_g)/(\partial V_d)$. For easiness, Equation (22) is stated with numerator and denominator represented as $N(n_s)$ and $D(n_s)$ correspondingly. With added simplifications, C_{gs} and C_{gd} are expressed as

$$C_{gs/d} = W.L_g.q\left[\frac{\partial N(n_s)}{\partial V_{s/d}}.D(n_s) - N(n_s)\frac{\partial D(n_s)}{\partial V_{s/d}} / \left(D(n_s)\right)^2\right] \tag{23}$$

Cut-Off Frequency (f_T)

The intrinsic-gain cut-off frequency (f_T) illustrates how rapidly the current is being controlled by the gate-voltage, and is one of the most substantial factors for considering the device shown in and microwave frequency ranges. The f_T, calculate from (g_m) and (C_{gs} and C_{gd}), can be expressed as

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})}.$$

Small-Signal Equivalent Circuit Model Parameters Extraction

This section details a comprehensive methodology for extracting all SSEC elements of the proposed structure. The corresponding SSEC model is illustrated in Figure 3. The circuit is conventionally divided into two segments: the extrinsic part—comprising bias-independent parasitic components (C_{pg}, $C_{pd,}$ C_{pgd}, $L_{g,}$ L_s, L_d, R_s, R_g, and R_d) and the intrinsic part, which represents the active device characteristics and exhibits bias dependence (C_{gd}, C_{ds}, C_{gs}, R_{gd}, R_{in}, R_{ds}, g_m, and τ).

The extrinsic (parasitic) components are typically treated as bias-independent because they represent the external interconnections and packaging effects rather than the intrinsic behavior of the device itself. In contrast, the intrinsic elements are bias-dependent. Accurate extraction of extrinsic parameters is crucial, as they directly impact the determination of intrinsic characteristics.[8] For a three-terminal device, the extrinsic network generally includes three parasitic inductances and resistances corresponding to each terminal connection. The inductances L_d, L_g, and L_s originate from the bonding and pad-connections, while the resistances R_d, R_g, and R_s arise from the drain, gate, and source contacts, correspondingly. Additionally, parasitic capacitances C_{pg}, C_{pgd}, and C_{pd} account for the capacitive coupling of the pad connections.

The intrinsic section of the circuit comprises eight key components, each with specific physical significance. These include a characterized by g_m and τ; gate-source capacitance and input channel resistance forming an input *RC* network (R_{in} and C_{gs}); R_{gd} & C_{gd} forming a feedback *RC* network; and R_{ds} and C_{ds} forming an output *RC* network. A critical aspect of equivalent circuit modeling is the accurate extraction of extrinsic elements, as they directly affect the determination of intrinsic parameters. Once these are well-defined, they serve as the foundation for calculating a more physically representative set of intrinsic equivalent circuit parameters.[8]

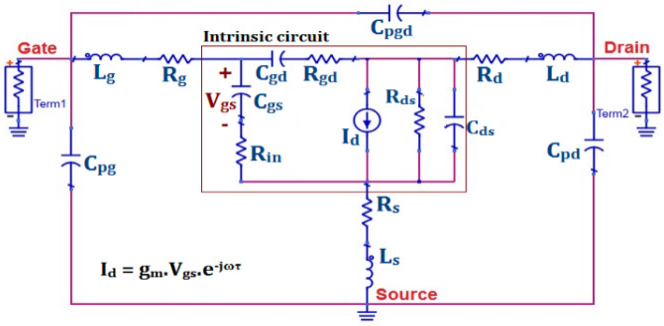

Fig. 3: The SSEC of the AlInN/AlN/GaN MISHEMT, the intrinsic elements indicated in the box.

Extrinsic Parameters

Extrinsic capacitances (C_{pgd}, C_{pg}, C_{pd}) of the device is typically extracted from the cold- routine [20]. When V_{ds} = 0 *V* and V_{gs} is negative to pinch-off voltage, then the channel exhibits negligible conductivity is trivial and the simulated -parameters display capacitive characteristics.[15,19,28] These three pad capacitances, C_{pgd}, C_{pg}, and C_{pd} are extracted from the imaginary components slope of the *Y*-parameters: Y_{11}, Y_{22}, and Y_{12} = Y_{21}, correspondingly as presented in Figure 4(A). The extrinsic parts of inductances and resistances are typically deliberate at zero or trivial negative gate biasing.[8] The extrinsic parts of inductances are L_g, L_d, and L_s can be assessed with *Z*-parameters slope of the imaginary part of ω.Im(ωZ_{ij}) versus ω^2 as presented in Figure 4(B) by linear fitting. The extrinsic resistances R_g, R_d, and R_s can be deliberate from the slope of the real parts of *Z*-parameters *Re*(Z_{ij}) versus ω^2 as shown in Figure 4(C).

The extrinsic parameters can be calculated by imaginary Y-parameters to extract the discrete extrinsic capacitances, imaginary part of Z-parameters for extrinsic inductances, and real part of Z-parameters for extrinsic resistances using Equations (24)-(32)

$$\mathrm{Im}(Y_{21}) = \mathrm{Im}(Y_{12}) = -\omega(C_{pgd}) \quad (24)$$

$$\mathrm{Im}(Y_{11}) = \omega(C_{pgd} + C_{pg}) \quad (25)$$

$$\mathrm{Im}(Y_{22}) = \omega(C_{pd} + C_{pgd}) \quad (26)$$

$$\mathrm{Im}(\omega Z_{11}) = (L_s + L_g)\omega^2 - \left(\frac{1}{C_s} + \frac{1}{C_g}\right) \quad (27)$$

$$\mathrm{Im}(\omega Z_{22}) = (L_s + L_d)\omega^2 - \left(\frac{1}{C_s} + \frac{1}{C_d}\right) \quad (28)$$

$$\mathrm{Im}(\omega Z_{12}) = (L_s)\omega^2 - \left(\frac{1}{C_s}\right) \quad (29)$$

$$\omega^2\mathrm{Re}(Z_{11}) = \omega^2(R_s + R_g) \quad (30)$$

$$\omega^2\mathrm{Re}(Z_{22}) = \omega^2(R_s + R_d) \quad (31)$$

$$\omega^2\mathrm{Re}(Z_{12}) = \omega^2(R_s) \quad (32)$$

Intrinsic Parameters

The intrinsic circuit parameters, as illustrated in Figure 3, are derived after extracting the extrinsic capacitances, inductances, and resistances. The simulated *S*-parameters are transformed into *Y*-parameters following the method outlined in Ref.[29] Subsequently, the remaining intrinsic equivalent circuit parameters are determined through a quasi-analytical approach using the *Y*-parameters and applying equations (33)-(40) within the ADS platform.

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \quad (33)$$

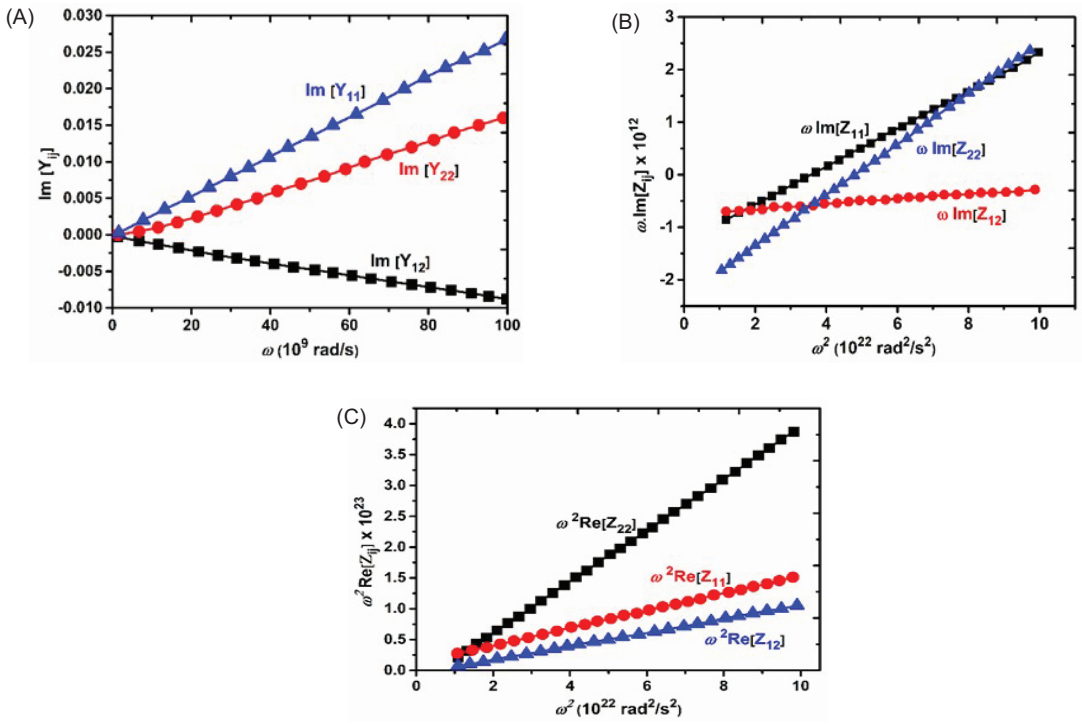

Fig. 4: Extrinsic parameter estimation of (A) Capacitances, (B) Inductances, and (C) Resistances.

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{\left(\mathrm{Re}(Y_{11})\right)^2}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2}\right) \quad (34)$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}) - \omega C_{gd}}{\omega} \quad (35)$$

$$R_i = \frac{\mathrm{Re}(Y_{11})}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2 + \left(\mathrm{Re}(Y_{11})\right)^2} \quad (36)$$

$$R_{gd} = \frac{-\mathrm{Re}(Y_{12})}{\omega C_{gs}.\mathrm{Im}(Y_{12})} \quad (37)$$

$$g_m = \left(\left(\mathrm{Re}(Y_{21})\right)^2 + \left(\omega C_{gd} + \mathrm{Im}(Y_{21})\right)^2\left(\omega^2 R_i^2 C_{gs}^2 + 1\right)\right)^{1/2} \quad (38)$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{21}) - \omega C_{gs} R_{in}\,\mathrm{Re}(Y_{21})}{g_m}\right) \quad (39)$$

$$g_{ds} = \mathrm{Re}(Y_{22}) \quad (40)$$

Results Analysis

The RF and DC performance characteristics of two MISHEMT structures, one with AlInN barrier, and other one with AlGaN barrier with gate lengths (L_g) of 0.1, 0.2, and 0.3 are analyzed and compared. The proposed analytical models are validated against TCAD simulation results. The inclusion of a thin AlN spacer layer at the heterointerface enhances electron transport by mitigating compound disorder scattering. In the nonappearance of an electric field, the complete polarization charge in the material is determined by the combined effects of spontaneous and piezoelectric polarization. Notably, AlN and GaN exhibit considerable differences in polarization behavior owing to the strong necessity of spontaneous polarization on material composition. Group III-nitride materials, particularly AlN, possess high spontaneous polarization. In the case of AlInN, the polarization encouraged charge is higher compared to AlGaN, attributed to the elevated aluminum concentration (83%) in the barrier layer. This enhanced polarization results in stronger internal electric fields and higher edge charge densities.[7] The 2D-EG sheet charge density was evaluated at the AlN/GaN interface for both device structures. Assuming constant barrier and spacer layer thicknesses, the 2D-EG sheet charge densities were calculated using Equation (15) as approximately 1.91×10^{13} cm^{-2} for AlGaN barrier with 30% Al content and 3.41×10^{13} cm^{-2} for AlInN barrier with 83% Al content. The correlation between the modeled and simulated 2D-EG sheet charge densities with gate voltage is presented in Figure 5.

Furthermore, the electron mobilities at 300 K were determined as 1253 cm^2/V·s and 1340 cm^2/V·s, respectively, using a low-field mobility model.[19] The improved electron transport behavior is attributed to the superior properties of -nitride compound semiconductors incorporated in these device architectures. Figure 6A,B illustrates the contrast b/w the analytical model and TCAD simulation results for the $I_d - V_d$ characteristics with gate lengths of 03, 0.2, and 0.1 µm.

The maximum drain current densities calculated using Equation (19) are approximately 0.78, 0.86, and 1.35 A/mm at V_{GS} = 0 V for AlGaN barrier device, respectively. In the case of AlInN device, the corresponding maximum drain current densities at V_{GS} = 0 V are 1.95, 2.12, and 2.34 for gate lengths of 0.1, 0.2, and 0.3 µm, respectively. These results clearly indicate that reducing the gate length enhances the drain current significantly. Furthermore, AlInN device exhibits a higher drain current density, which can be attributed to its increased content and superior material-properties compared to AlGaN device. The drain current values for both devices across various gate lengths are summarized in Table 1, and the analytical model with the simulation is shown in Figure 6A,B.

Figure 7A,B presents a comparison between the analytical model and TCAD simulation outcomes for the $I_d - V_{gs}$ and $g_m - V_{gs}$ characteristics, with gate lengths of 0.1, 0.2,

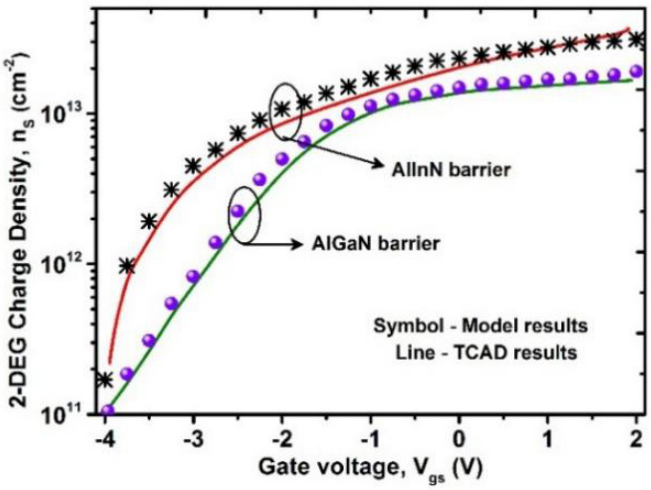

Fig. 5: 2D-EG charge density with gate voltage for AlInN and AlGaN barrier devices.

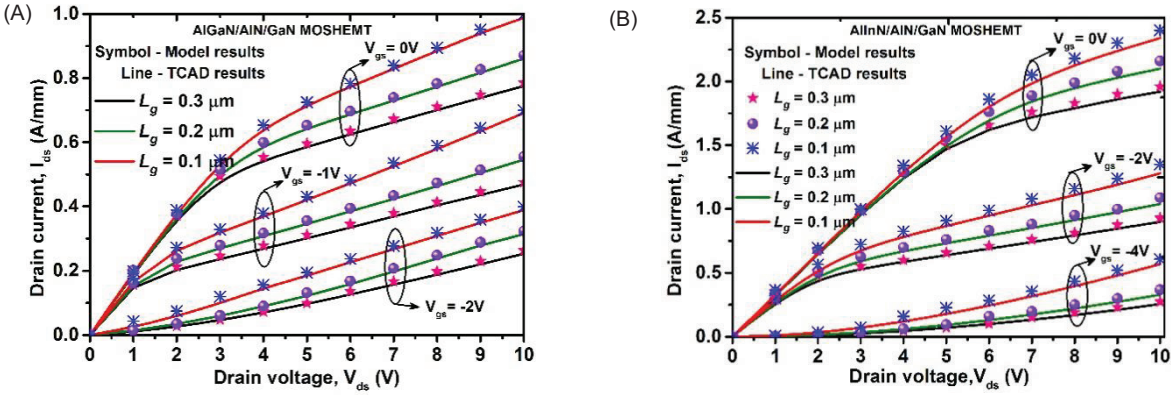

Fig. 6: Analytical model $I_{ds} - V_{ds}$ for gate lengths of 0.1, 0.2, and 0.3 μm. (A) AlN/AlGaN/GaN MOSHEMT (B) AlInN/AlN/GaN MOSHEMT device structure.

Table 1: Comparison of AlGaN/AlN/GaN and AlInN/AlN/GaN MOSHEMT.

Device Structure	I_d (A/mm)	C_{gd} (fF/mm)	g_m (mS/mm)	C_{gs} (fF/mm)	L_g (μm)	f_T (GHZ)
AlGaN/AlN/GaN MISHEMT	0.78	486	310	636	0.3	44
	0.86	404	321	540	0.2	55
	1.35	270	342	370	0.1	86
AlInN/AlN/GaN MISHEMT	1.95	517	467	668	0.3	64
	2.12	433	499	570	0.2	79
	2.34	286	531	395	0.1	125

and 0.3 μm, respectively. From these figures, it is evident that the analytical model closely aligns with the TCAD simulation results. The flat band voltage for the three different gate lengths and device structures is determined from the slope of the $I_d - V_{gs}$ curves. For AlGaN device, V_{FB} lies between −2.5 V and −3.5 V, whereas for AlInN device, it ranges from −4 V to −5 V. Negative VFB shifts result due to a reduction of the VFB, caused by both the variation of gate length and barrier material, and also due to an increase in density when using an spacer layer, and/or a negative gate bias causing electron injection at the interface that results in increased subthreshold current as the gate length decreases.

The determined transconductance (g_m) values obtained for a gate length (L_g) of 0.1 μm are 343 mS/mm for AlGaN device and 531 mS/mm for AlInN device. These results indicate that g_m increases with decreasing L_g, consistent with the behavior predicted by Equation (19). This enhancement in g_m can be recognised to the reduced density of surface traps provided by the Al_2O_3 layer, which increases the electric field beneath the gate, thereby enhancing the 2D-EG sheet-charge density.[4] Additionally, it is observed that the slope of g_m diminishes with increasing V_{gs} beyond its peak, primarily due to the saturation of the 2D-EG sheet charge density, which points to a near-constant current density at higher gate biases.[11] The blend of high 2DEG sheet charge density and carrier mobility is a key factor contributing to the elevated drain current and maximum transconductance.

The gate-channel capacitances, C_{gs} and C_{gd}, calculated using Equation (23), are plotted against the gate voltage for three different gate lengths as depicted in Figure 8A,B. A strong correlation is observed between the analytical model predictions and the simulation outcomes. The results indicate that both C_{gs} and C_{gd} decrease notably as the gate length reduced.[13, 21]

The unity current cut-off frequency (f_T), derived from the capacitances and trans-conductance, is presented in Table 1. The analysis shows that f_T increases consistently from 45 to 86 for AlGaN device and from 64 to 125 for device as L_g is scaled down from 0.3 to 0.1 μm. This enhancement in f_T is attributed to the reduction of C_{gs} and C_{gd} along with an increase in g_m. These observations confirm that f_T improves with decreasing L_g, indicating that AlInN device, with a shorter gate length, is more suitable for and microwave.

Table 2 summarizes experimentally reported data for AlGaN and AlInN-based MOSHEMTs from various studies.[11,26-29]

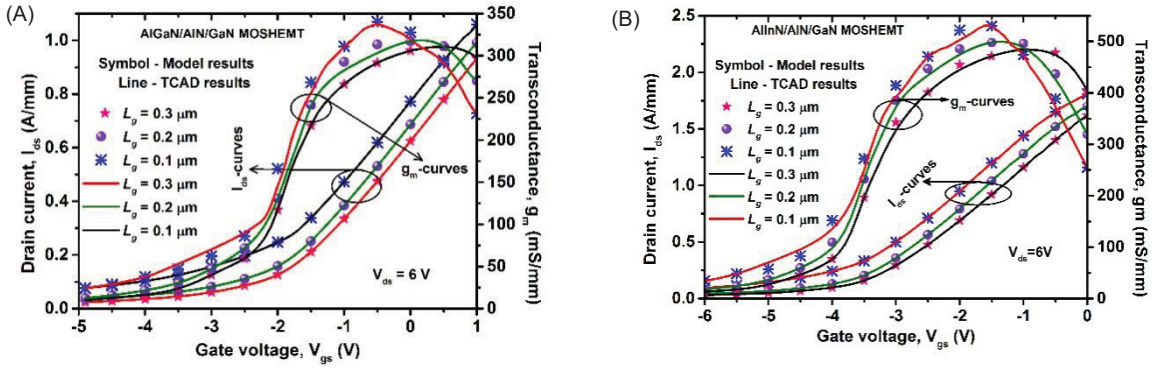

Fig. 7: Analytical model I_{ds} – V_{gs} and g_m – V_{gs} characteristics in association with TCAD simulation results for gate lengths of 0.3, 0.2, and 0.1 μm (A) AlGaN/AlN/GaN MISHEMT (B) AlInN/AlN/GaN MISHEMT.

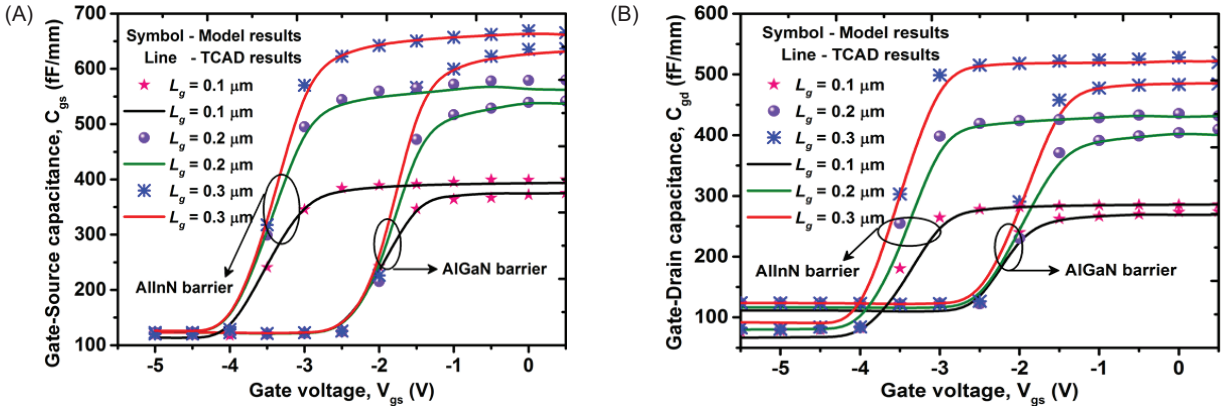

Fig. 8: (A) C_{gs} and (b) C_{gd} capacitance performane with 0.1, 0.2 and 0.3 μm gate lengths.

Table 2: Experimentally determined values of AlGaN (AlInN)-based "MISHEMT"

Device structure	L_g (μm)	I_d (A/mm)	g_m (mS/mm)	f_T (GHz)
AlGaN-based MISHEMT	0.5 [26]	0.488	130	51.3
	0.25 [27]	0.9	240	63
	0.16 [28]	0.54	237.2	65
AlInN-based MISHEMT	0.6 [29]	1.22	328	17
	0.15 [11]	~2.1	~500	~161
	0.1	2.3 [30]	510 [11]	160 [11]

These experimental findings reveal that AlInN-based MISHEMTs demonstrate superior performance at shorter gate lengths compared to their AlGaN counterparts. To validate the proposed analytical model, the results presented in Table 1 were related with the experimental data in Table 2, showing close agreement between the two.

The AlInN/GaN MISHEMT is considered to extract SSEC parameters. Figure 9A,B presents the two-port S-parameter results measured across the frequency range of 500 MHz to 100 GHz. The extrinsic parameters of the device were first derived from slopes of the imaginary components of the *Y* and *Z*-parameters, along with the real part of *Z*-parameters, as presented in Figure 4 and expressed through Equations (24)-(32). Subsequently, the intrinsic parameters were extracted using the previously obtained extrinsic elements in conjunction with the *Y*-parameters derived through the simulations, following Equations (33)-(40). After determining both extrinsic and intrinsic parameters, the model -parameters were simulated using the platform.

To validate the small-signal model extraction methodology, parameters obtained from simulation analysis were examined for validation. The tool's gradient centered optimization method was utilized to minimize the difference between the extracted model and the model. From a modeling perspective, the optimization-based extraction of the model is effective in minimizing errors with respect to the modeled results under one bias condition. Robustness is established through verification of nondependence upon an initial estimate (bias) of the optimized results.[24] The process utilizes a least-squares

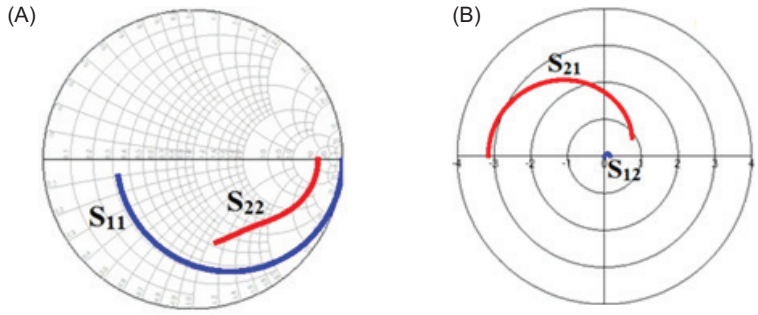

Fig. 9: Device simulation obtained in TCAD tool. (A) S_{11} and S_{22} AC frequency (B) S_{12} and S_{21} AC frequency.

fitting approach[16] to minimize the deviation among the SSEC model and the simulated *S*-parameters. To enhance the fitting accuracy, a maximum repeating optimization setting was applied in ADS. Optimization objectives were specified to minimize both phase and magnitude deviations of the *S*-parameters, with defined parameter constraints for each circuit element. Upon execution, the optimization process achieved a close match among the model and the simulated *S*-parameters, as depicted in Figure 10. The extracted intrinsic and extrinsic parameters for the AlInN/GaN MISHEMT device under cold-conditions are summarized in Table 3.

From the extracted components, it is witnessed that R_d is significantly larger than R_s and L_d is considerably larger than L_g. This is attributed to the proposed structure, where the distance (L_{gd} = 0.6 µm) is greater than the gate-to-source space (L_{gs} = 0.3 µm), with a gate length of 0.1 µm. The increased gate-to-drain spacing enlarges the area of the contact, resulting in a higher R_d compared to R_s. Moreover, this larger distance increases the materialization length, leading to a higher L_d.[5,11,30] The *S*-parameter error percentage between the model and the simulated device is S_{11} = 3.53%, S_{21} = 3.45%, S_{12} = 2.87%, and S_{22} = 3.941%. Additionally, to strengthen the validity of the small-signal model, the SSEC (Figure 3)

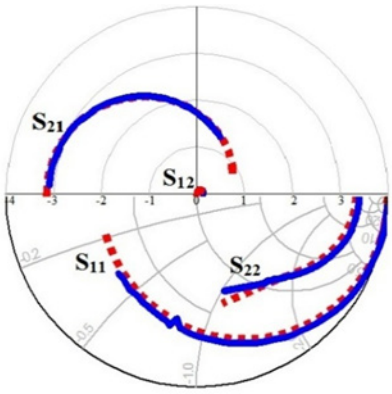

Fig. 10: *S*-parameter (line) and TCAD (dashed line) simulations results for AlInN/GaN MISHEMT.

Table 3: Optimized Model of the Intrinsic and Extrinsic Elements

Extrinsic elements	Optimized value	Intrinsic elements	Optimized value
$R_g(\Omega)$	18.68	$C_{gs}(fF)$	98.15
$R_d(\Omega)$	13.75	$C_{gd}(fF)$	34.5
$R_s(\Omega)$	02.75	$C_{ds}(fF)$	30.26
$L_g(\Omega)$	39.61	$g_m(mS)$	395.60
$L_d(\Omega)$	78.21	$\tau(ps)$	1.05
$L_s(\Omega)$	3.531	$R_{in}(\Omega)$	4.6
$C_{pg}(fF)$	52.411	$R_{gd}(\Omega)$	73.29
$C_{pd}(fF)$	40.121	$R_{ds}(\Omega)$	118.3
$C_{pgd}(fF)$	2.861		

simulated using the extracted factor values under different operating conditions. This approach helps to distinguish bias-dependent from bias-independent parameters, enabling accurate modeling under varying biasing. Hence, it is recommended to deliberate at least two biases to ensure robust parameter extraction.[21] The intrinsic factors are attained from the admittance parameters once de-embedding extrinsic contributions under diverse bias conditions. It is worth mentioning that these parameters may also be extracted through bias-reliant *S*-parameters calculated for several voltages, which is particularly useful for large-signal model design.[17] Table 4 encapsulates the extracted parameter figures for various biases.

The small signal model reproduces the S-parameter behavior to varying degrees of accuracy at different levels of dc biasing, as shown in Figure 11. Therefore, it is assumed that those parameters determined at and less than Vp are sufficient to establish the *s*-parameter description of this device. The parameters have been determined at three additional operating conditions to validate the model further: V_{gs} = 0 V, V_{ds} = 5 V; (b) V_{gs} = –2 V, V_{ds} = 20 V; and (c) V_{gs} = –4 V, V_{ds} = 10 V. These parameter values demonstrate a continuous relationship among the operating points, and therefore are appropriate for

providing a uniform value for use in optimization-based extraction methodologies. Also, the extracted -parameter values show good agreement with previously published values for similar devices.[21,24,27]

Table 4: Extracted Intrinsic parts of SSEC at diverse biases.

	V_{gs} = −2.0 V V_{ds} = 20 V	V_{gs} = 0.0 V V_{ds} = 5 V	V_{gs} = −4.0 V V_{ds} = 10 V
$C_{gs}(fF)$	137.21	113.80	118.30
$C_{gd}(fF)$	28.41	42.90	37.80
$C_{ds}(fF)$	26.631	29.80	28.241
$g_m(mS)$	301.71	219.21	337.21
$\tau(ps)$	1.252	1.031	1.041
$R_{in}(\Omega)$	11.50	13.012	6.91
$R_{gd}(\Omega)$	121.80	84.72	89.51
$R_{ds}(\Omega)$	107.60	128.32	131.11

The extracted *S*-parameters from small-signal model simulation were utilized to determine various *FoM* of the device. Among these, the cut-off frequency (f_T) and f_{max} are the critical indicators of microwave frequency performance. The (f_T) is derived from −20 dB/decade slope of the h_{21}, while the maximum oscillation frequency is estimated using the −20 dB/decade slope of the maximum available gain (MAG).

The maximum available gain (MAG), unilateral power gain (U) current gain (h_{21}) of the optimized model SSEC with cold-FET conditions are plotted in Figure 12 against frequency based on equations (41)-(43).

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)} \tag{41}$$

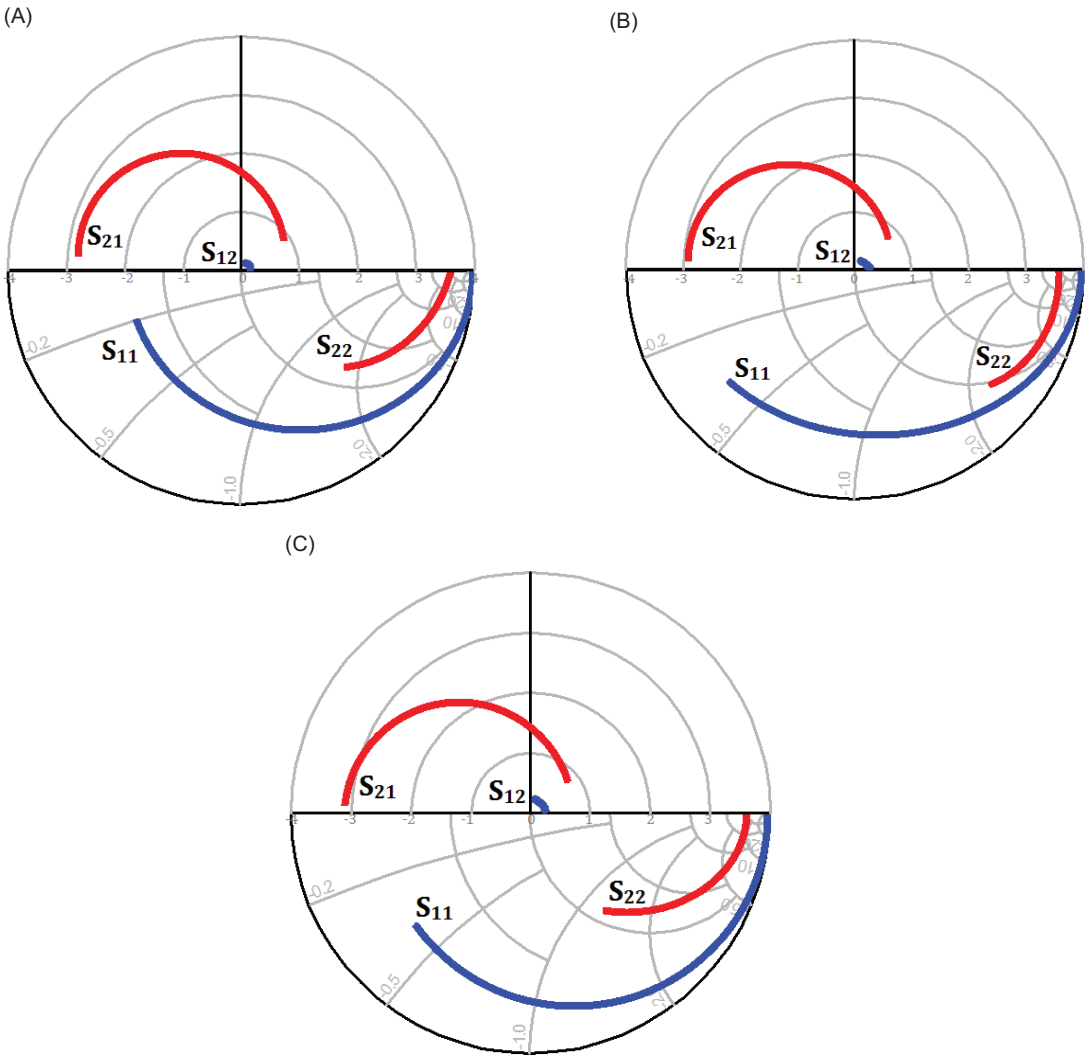

Fig. 11: *S*-parameter attained with diverse biases. (A) V_{ds} = 5V and V_{gs} = 0 V (B) V_{ds} = 20V and V_{gs} = 2 V (C) V_{ds} = 10 V, and V_{gs} = −4 V.

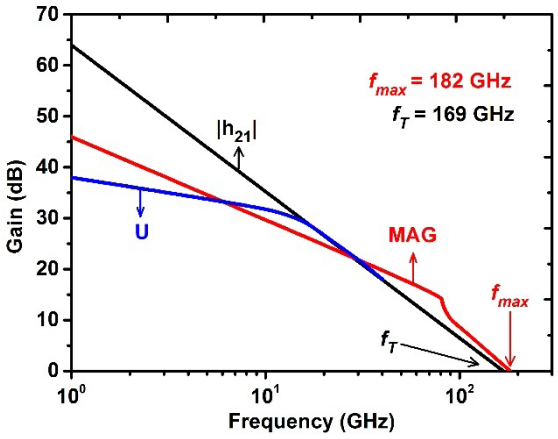

Fig. 12: SSEC device microwave traits optimized cold-state via Equation (41)-(43).

Table 5: *FoM* of Microwave Characteristics in Association with Swain et al.[3] and Jena et al.[5]

	Proposed work	Ref[3]	Ref[5]
f_T(GHz)	170	162	160
f_{max}(GHz)	183	172	
H_{21}(dB)	64.0	46	
MAG	46.0	28	
U	38.0	23	

$$MAG = 10\log\left|\frac{S_{21}}{S_{12}}\right| \quad (42)$$

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad (43)$$

The approximate parameters (based on the plot) used to determine the 170 MHz small-signal current cut-off frequency for the proposed microwave device; and, the maximum oscillation frequency of the device of 183 MHz were compared to values obtained from previously published experiments.[3,5] Although,[3] utilized a single finger gate that was 100 microns long, and[5] utilized a two-finger gate that was also 100 microns long, there is good correlation as indicated in Table 5.

Conclusion

An analytical model to evaluate the 2DEG sheet charge density was developed based upon the polarization characteristics and the flat band voltage of , and . This model, in turn, was used to develop models for drain current density, transconductance, capacitances, and high-frequency cutoff (current gain) frequency as a function of gate length. These models have been validated using both and experimental data from several authors over a wide range of gate lengths. Furthermore, the results indicated that the best performance at high frequencies can be achieved by employing a barrier material of high Al content and decreasing the gate length.

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