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Design and Analysis of 4-bit Reconfigurable Johnson Counter using 18nm finFET

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Abstract

The counter is used widely as an important component in measurement systems. Hybrid logic has one prominent advantage in the construction of counter circuits because it requires a minimal number of transistors and demands low power. This work is a reconfigurable 4-bit Johnson counter. The counter is used for counting, when the mode is set to one. In this configuration, the flip-flops are initialized after four clock cycles, provided that the reset (RST) signal is low. If RST is high, then the counter performs its normal counting operation. When the mode is off, the counter is changed by resetting the last bit of the count vector to its initial value. The flip-flop is the basic component of the proposed counter. To realize a low-power, high-speed and low-complexity counter, we implemented a mixed logic flip-flop. This flip-flop is implemented using 18 transistors, comprising 9 PMOS and 9 NMOS. It is built only on complementary logic and pass-gate transistors, resulting in higher operating speed, less power consumption, and fewer transistors, which ultimately enhance the power-delay-complexity trade-off. The obtained results were achieved using Cadence Virtuoso at the finFET technology node 18 nm. Experiments were conducted in different process corners, with supply voltages ranging from 0.7 to 1.0 V, and temperatures varying from −25 to 75 °C. Based on the results, the proposed counter shows tremendous stability.

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Introduction

Analog-to-digital converters (ADCs), phase-locked loops (PLLs), frequency dividers, synthesizers, and other analog-to-digital interconversion structures use a counter as a basic functional block. Recent advances in technology have created an increasing need for high-speed counters over a wide range of numbers while having a constant counting frequency regardless of their bit width. A constant problem is the propagation delay involved when a carry propagates from less significant to more significant bits; this increases with increasing counter width. Simple asynchronous counters, also known as ripple counters, only require a few logic gates to realize. But still, in the propagation of ripple, all the flip-flops (F/F) have different clock signals, and the transient effect makes the output incorrect, and adds to the delay time. The ripple effect increases with the increase in counter size, which is of serious concern in applications that require a deterministically accurate counter value.[1]

A synchronous digital counter can be used to produce a consistent, reliable binary result. In a ripple-carry synchronous counter, the carry-out of one adder stage is used as the carry-in of the next adder stage; the series of carry signals is called a ripple-carry chain, because the carry is propagated from one stage to the next in sequence. The rate of the carry propagation is the maximum limiting factor to the speed of a synchronous counter. Several researchers have introduced many techniques to speed up the adders and use those techniques to build quick counters.[2] To speed up a conventional binary counter, methods such as carry-look-ahead circuitry have been put in place as a substitute for the ripple-carry chain. Further, a hierarchy-based Manchester carry chain was used to support carry propagation.[3] A state-lookahead architecture has also been exploited to suppress the ripple effect by using D-type flip-flops to reduce the possibility of carrying ripple. For a counter using a combination of addition and a state

register, the minimum delay of an adder is not a constant, and this does not allow for a uniform clock period. Previous efforts to speed up the flip-flop itself, and for realizing high-speed, synchronous counters that run off a single-phase real clock have been reported.[4,5] When rapid concurrent counting is needed rather than a simple binary sequence, a counter can be synthesized by combining state generation with the existence of a consistent clock period. The Johnson counter was chosen for this configuration because it provides a great combination of speed, low power consumption and can also be programmed. The shrinking size and controllability of conventional semiconductors of the type of metal oxide semiconductors (MOS transistors) have intensified the short-channel effects (SCEs) evident in substantial low-threshold-voltage roll-off, decreased subthreshold swing, and high leakage currents. Consequently, the FinFET has become one of the predominant solutions to reduce SCEs[6,7]. FinFET technology has brought further development to a wide variety of devices and has proven to be useful in overcoming such challenges. While bulk transistors of dense silicon are restricted to channel sizes equal to or larger than 45 nm, FinFETS could have terminals equal to or smaller than 7 nm with minimal loss in conductivity[8,9].

Traditional planar CMOS circuits have strong short-channel effects at technology nodes in nanometers that give rise to high leakage currents, increased threshold voltage variability and reduced electrostatic control. The impairments have a significant effect on the performance of sequential digital circuits (such as counters and flip-flops) run at reduced supply voltages. FinFET devices have better electrostatic control through multi-gate channel modulation that suppresses leakage currents and gives a better sub-threshold slope compared to bulk CMOS technology. The inherent three-dimensional gate structure enhances the channel confinement and thereby reduces the Drain Induced Barrier Lowering (DIBL) and improves the switching efficiency. These features make FinFET topology particularly favorable to low-power sequential circuits, which require robust functionality in a wide variety of process and environmental conditions. The experimental data provided in this paper are directly supported by the benefits that FinFET devices can provide. The reduced leakage property is the basis of the lower power consumption at a range of supply voltage 0.7–1.0 V, and the improved electrostatic control is the key to the stability of delay at PVT (process, voltage, temperature) variation. Also, the limited performance dispersion that was observed with the Monte Carlo simulation supports the reduction in variability obtained with FinFET implementation.

Due to the compact dimensions of the modern components, an appropriate memory organisation is needed. FinFETs have superseded the use of the MOS transistor (MOSFETs) in many applications due to size limitations[5,8,25]. An extra gate has been introduced in low-voltage activity monitoring, as it is recognized that FinFET operation depends on both gate potentials. Figure 1 shows the structure of the novel FinFET, whereas Figure 2 shows an SOI FinFET device with three different gates: Gate 1, placed on the side of the fin channel; Gate 2, placed at the upper center; and Gate 3, placed at an alternate extremity. Many gate architectures are used in a FinFET die. The fabrication sequence usually starts with preparation of the SOI substrate and construction of the primary FinFET framework, and ends with the deposition of an intergate dielectric isolation layer. The corresponding demonstrations

This study examines a low-power, low-delay, mixed logic, reconfigurable Johnson counter. At first, a high-speed and low-power flip-flop was designed; the PVT (process variation, voltage variation, and temperature) resilience of the flip-flop was confirmed through an extensive analysis. Simulation results show that when the proposed flip-flop is added to the reconfigurable Johnson counter, it can achieve a significant decrease in delay and power consumption. Evaluations were performed in Cadence

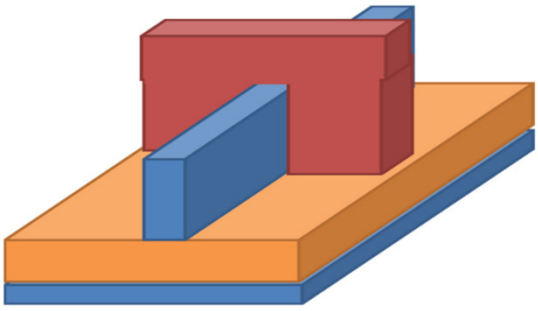

Fig. 1: Diagram of FinFET Device[10].

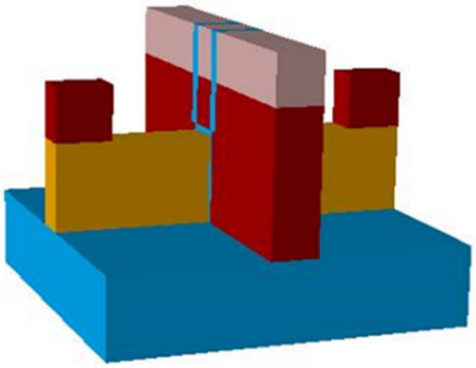

Fig. 2: Diagram of SOI FinFET Device with Independent Gates[10].

Virtuoso under the supply voltage of 0.7 V and clock frequency of 10 MHz at ambient temperature using 18nm FinFET technology. Monte Carlo simulations also support the lower power dissipation and propagation delay of the chosen flip-flop. Although Johnson counters are widely used for sequence generation and low-transition switching applications, conventional designs typically operate in fixed configurations without architectural adaptability. Existing works primarily focus either on counter topology optimization or flip-flop power reduction independently.

The novelty of the proposed work is in the merging of reconfigurability of architectural components, together with device-level optimization where a mixed-logic flip-flop is produced by means of 18 nm FinFET technology. This counter employs a mode-controlled feedback loop that enables the counting behavior of this counter to be adjusted dynamically, without the extra control circuitry or increased hardware overhead.

The principal contributions of the work are as follows:

1. Architecture of a reconfigurable Johnson counter that could be changed to different operating modes by a simple control signal.
2. Addition of an 18-transistor mixed-logic flip-flop, a circuit simplifier and switchcap.
3. Minimization of power utilization by single-bit transition properties of Johnson sequences.
4. PVT and Monte-Carlo analysis validation, which shows strength and reliability.
5. Application of FinFET technology, making it possible to use low voltages in applications with better electrostatic control.

The architecture proposed is highly configurable, energy-efficient and delay-sensitive. It is similar in benefits to traditional Johnson counters but with less hardware complexity.

Section 2 provides a lengthy review of Johnson counters and flip-flop configurations. Section 3 outlines the combination of the functional capabilities of the proposed counter and flip-flip. Section 4 shows a comparative analysis between the results of the simulation and existing configurations. Section 5 highlights the conclusions.

Literature Review

The next subsection is a detailed description of studies from the past that contain concepts that are relevant to the recommended counter. Figure 3 shows the traditional synchronised binary counter, which is made up of a series of T flip-flops, which have the XOR gate within them. Note that the simplest logical operations needed to change a single bit in the number of the counter are XOR operations. The set of AND gates examine each of the lowest bits in a certain order, beginning with the least significant bit (LSB). If all of the lower bits are set to 1, then a carry signal is sent. The AND gates are linked in series to form a long pathway called a ripple-carrying chain.[3,11,12]

The ripple carry chain passes the carry signal from the least significant bit (LSB) to the most significant bit (MSB), one after the other moving forward. For this reason, the standard binary counter has a significant propagation delay, which is proportional to the size of the counter. Reverse carry propagation, according to the description in Ajane et al. (2011),[3,24] is an essential concept for the efficient implementation of high-speed synchronous counters. Owing to the inherent characteristics of the binary numeral system, the counter sequentially gives a higher-order bit a high state before the corresponding lower-order bit is set. As shown in Figure 4, unlike a traditional binary counter, the counter uses a different AND chain for each bit and has its chain input to the reverse. Thota and Mal (2016)[4] suggested a constant-delay digital counter using prescaling, as shown in Figure 5.

In recent counter studies involving low power, much of the research aimed at minimizing unnecessary switching transitions through architectural methods, including clock gating, low-transition sequencing, and activity-aware state generation. Generation of low-transition sequences is also applied, especially in test-pattern generation and energy-conscious sequential logic, because it generates minimal bit switching between successive vectors and lowers the dynamic power. These techniques encourage

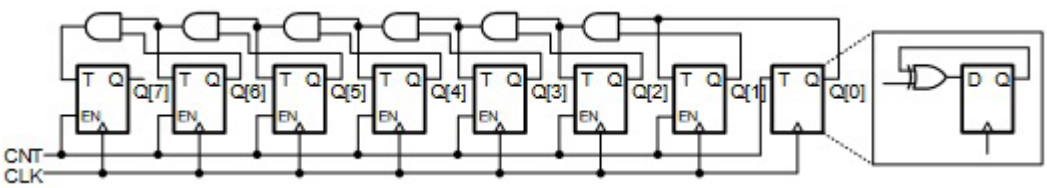

Fig. 3: Traditional 8-bit Synchronous Counter.[3]

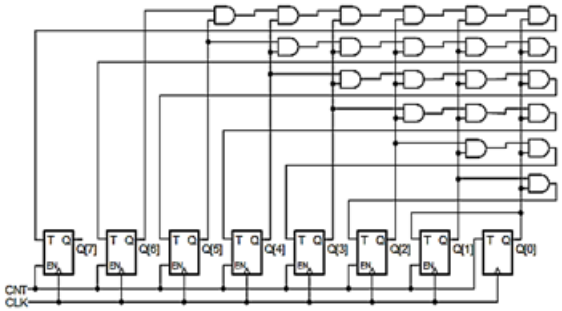

Fig. 4: Backward Propagation Carry Based 8-bit Synchronous Counter.[3]

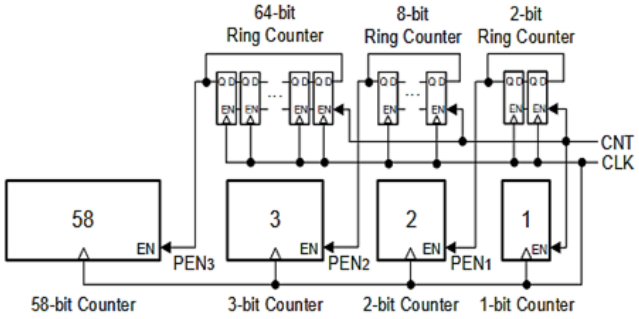

Fig. 5: Prescaled-enabled Signals-based 64-bit Counter.[4]

the usage of Johnson-style sequences as they possess a single-bit transition behavior and are suitable for low switching activity.[13,14]

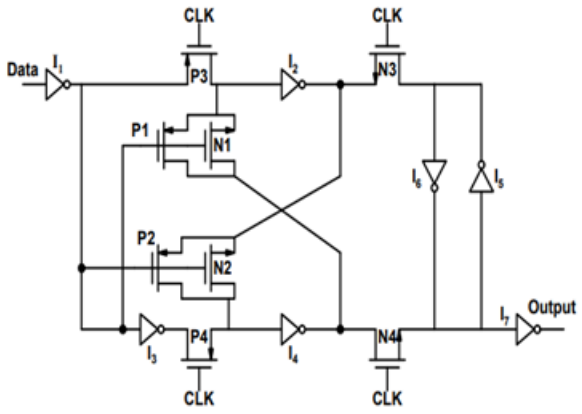

Fig. 6: Implementation of CMOS-based TG Flip-Flop [16].

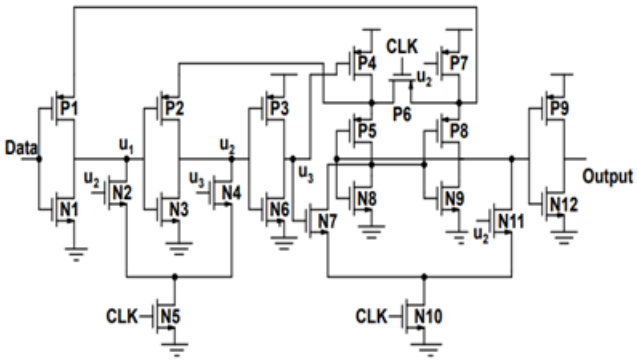

Fig. 7: Implementation of CMOS-based AC Flip-Flop [17].

The structures of traditional flip-flops are very similar to the traditional Set-Reset flip-flop (SRFF). Conversely, the increasing popularity and recognition of the Transmission Gate flip-flop (TGFF) as a suitable alternative is illustrated in Figure 6. The main problem related to this arrangement is a high clock load. The clock signals CLK (CLOCK) and CLK - (CLOCK BAR) are used by each flip-flop logic block, and their simultaneous use increases the number of transistors and the load at the clock input. Moreover, the extra circuitry required for the generation of CLK and CLK' interferes with the overall architectural scheme and thus causes a strong increase in the dynamic distortions even with relatively low switching frequencies of data. Presently, minimization of production cost and silicon real estate is the focus of the VLSI sector. Digital-centric industries require economically viable and small electronic devices; therefore, it is imperative to reduce the silicon footprint in central processing units (CPUs). The True Single-Phase Clocking (TSPC) based flip-flop design is therefore used to reduce the burden of the clock load. Irrespective of the input stimulus, when the clock requirement increases, power consumption increases proportionally. TGFF is subjected to a lot of clock-overload because it relies on one clock to drive twelve transistors. Other flip-flop topologies, such as the adaptive coupled flip-flop (ACFF) shown in Figure 7, the conceptually compressed flip-flop (TCFF) shown in Figure 8, and the logical structuring reduction flip-flop (LRFF) shown in Figure 9, have higher power dissipation due to clock overloading. The ACFF design uses differential latching instead of the normal SRFF scheme to support TSPC functionality. Here, the transmission gate is replaced by the pass-transistors used as a part of a two-level restorer (LR) network; LR circuits use a parallel configuration with an NMOS and a PMOS device. As a result, the clock pulse only turns on 4 out of the 22 transistors, and the decrease in ACFF slave count becomes very apparent. Data conflicts may breed problems in establishing reliable connections, and the switching activity is intensified. By adding an auxiliary multiplexer to the SRFF master, the clock burden is effectively relieved, and we have a True Single-phase Clock Flip-Flop (TCFF) system. Using a simplified approach, only one clock input is needed to limit energy consumption; therefore, the number of transistors in the TCFF is lower than in the SRFF. LRFF is a better version of TCFF, using complementary-pass-transistor logic (CPL) topology. CPL architecture consists of a pass transistor that transmits the clock pulse in the gate terminal with either terminal 2 or 3 as the signalling drain. The CPL

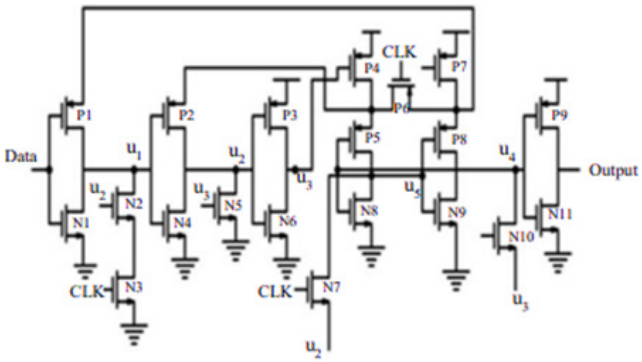

Fig. 8: Implementation of CMOS-based TC Flip-Flop[18].

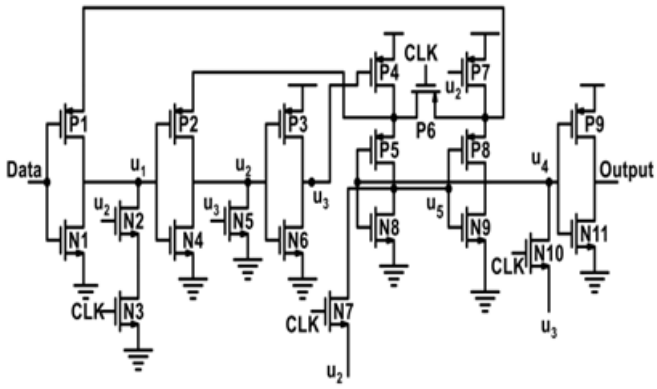

Fig. 9: CMOS-based implementation of LRFF[19].

(Complementary Pass Logic) design ends up providing the slave side with two charging channels, each with two pass terminals, making it easy to carry out the charging of terminals 4 and 5 to a high logical state represented by a value "1." The paper introduces a comprehensive analysis of the development of a flip-flop called as "conditioned clock technique-based level-converting flip-flop with a conditional clock technique" (CC - LCFF).

New developments in flip-flops focus on minimising the clock loading, the number of clock-controlled devices and also the use of hybrid/mixed-logic designs to enhance energy efficiency whilst preserving strong timing. FinFET-based flip flop design space exploration has revealed that sizing approaches and the topology selection play an important role in power and delay at nanoscale nodes. Low-power operation through a low count of transistors and better delay characteristics have also been reported to be accomplished by hybrid logic flip-flops based on modern nodes. Very low-power flip-flops based on a small number of clock transistors have also been suggested, and the significance of clock-load minimization in energy-efficient sequential design is solidified. Also, single-phase clocking scan flip-flop methods have been studied in reality to minimize overhead clock and maintain functionality.

Rajesh Krishna et al.[15] proposed a new master-slave flip-flop with 15 transistors and a single-phase clock using both fundamental and adaptive coupled approaches. The proposed circuit is an improvement over the existing logic, structured architectures with 45 nm CMOS technology. Comparative analysis shows that this flip-flop consumes significantly less power than other variants. Monte Carlo simulations show a decrease in the total area due to a reduction in the number of PMOS devices. The design remains efficient up to clock frequencies of 1 GHz.

In the case of nanoscale digital circuits, FinFET technology is commonly used because of enhanced electrostatic design, decreased short-channel behavior, and enhanced leakage models in comparison to planar CMOS. Recent investigations on low-power FinFET-based methods focus on the reduction of leakage properties and energy efficiency in scaled design processes, and it is in support of the applicability of FinFETs in low-voltage sequential circuits. Scalability and variability issues are also referred to as wider FinFET literature that can directly affect how sequential circuits can be stable to changes in both process and environment. More recent works on FinFET-based arithmetic circuits also indicate that topology design can be used to achieve better speed/energy behavior as well as overcome variability issues in scaled nodes.

Existing works have optimized (i) counter architectures in terms of speed or switching activity reductions, or (ii) flip-flop topologies in terms of low power and reduced clock load. Nevertheless, relatively little work co-optimizes a reconfigurable Johnson counter architecture and a mixed-logic flip-flop on FinFET technology, and also demonstrates its robustness on PVT and Monte-Carlo analysis. The explained gap drives the suggested design, in which the architectural reconfigurability is coupled with the low number of transistor-count mixed-logic, the power-delay trade-off and is stable to the supply-voltage and process variations.

Proposed Structure of Johnson Counter

The next subsection shows a demonstration of one reconfigurable setup for a 4-bit Johnson counter. Since the test is a direct relationship between the power consumption and the rate of transitions between adjacent values of the test vector, the Johnson counter can provide vectors with minimal transition activity between consecutive vectors or between neighbouring bits within the same vector. The Johnson series is a series of modifications of a single input (or sometimes

called a Single Input Change, SIC pattern). In each step of this series, every clock pulse produces a vector that differs from the previous alphabet string by one bit. Johnson's sequences are a sequence of alternating "0" and "1" values, which reduces the power usage. A simple Johnson counter, however, cannot be used for data shifting and loading operations. We make changes in the Johnson counter depending upon the evaluated pattern-generating technique. The reconfigurable Johnson counter can be seen in Figure 10. Whenever the mode is set to one, the counter performs the counting operation. In this configuration, the initial configuration of all the flip-flops is completed after L clock cycles, provided that the reset (RST) signal is asserted to zero. Whenever the RST signal is asserted to one, the counter carries out its normal counting operation. When the mode is disabled, the counter changes by replacing the last bit of the counted vector with its original value. Every Johnson vector's neighboring bit is alternately zero and one, conserving the adaptable Johnson counter's single-hop attribute in the sequence that it produces. The experimental configuration of the 4-bit counter proposed in this paper is shown in Figure 11. The subsections discuss in detail the design of all the submodules of the counter.

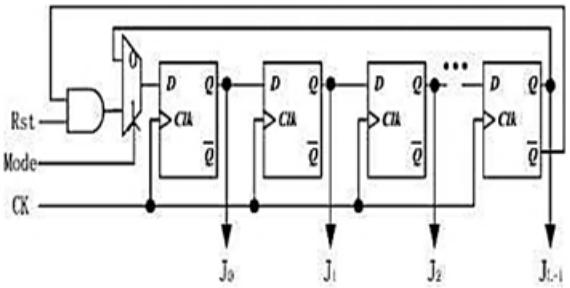

Fig. 10: Architecture of Reconfigurable Johnson Counter.

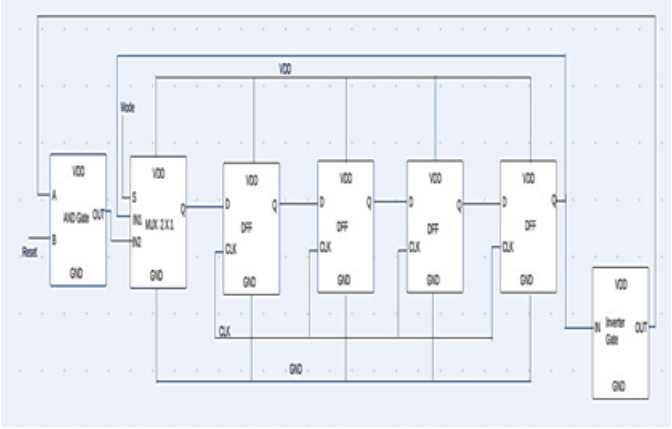

Fig. 11: 4-bit Architecture of Proposed Reconfigurable Counter.

Design of Proposed Low Power Mixed Logic Flip-flop

The limitations of prior low-power flip-flop approaches have prompted calls for more advanced solutions. This methodology adds other circuit topology simplification techniques to increase the design of ACFF circuits. The hybrid logical architecture is incorporated into the proposed design. At the initial stage, a complementary metal oxide semiconductor (CMOS) style SR (Set - Reset) latch is used, while a pass transistor logic (PTL) is used for SRAM-based latching at the secondary stage. This hybrid approach is therefore used to reduce the overall circuit intricacy. The proposed circuit design consists of 18 transistors (Figure 12). The transistor architecture implies the following transistor-level techniques: The pull-down circuitry uses NFETs for both control and regulation using a single signal often referred to as "u2". Figure 5 shows that there are two different channels that could use this signal to help discharge. It is critical to realize that the NM6 transistor, which works as the main latch, holds the input stage in an active state. This condition triggers the NM14 device, which controls the slave latching circuit. Therefore, the slave latch can be used for releasing the primary latch. Thus, it avoids the need for duplicating each of the n-MOS devices that are activated by the clock signal, which makes the design easier. This approach potentially reduces power consumption and design constraints, as well as reducing the capacitance load associated with the clocking signal. In most cases, by minimizing leakage, a reduced number of transistors needed to make a fully static design saves on energy. The total number of transistors in the proposal is 18, including 9 PFETs and 9 NFETs. The configured flip-flop circuitry uses exclusively complementary logic and pass logic transistors. It succeeds in achieving an increase in delay values while at the same time minimizing the overall circuit complexity. The proposed circuit design comprises 18 transistors (Figure 12). The MOS transistor architecture proposes the following transistor-level techniques: The pull-down circuitry uses NFET transistors for the control and regulation through a single signal, generally denoted as "u2." There is a problem

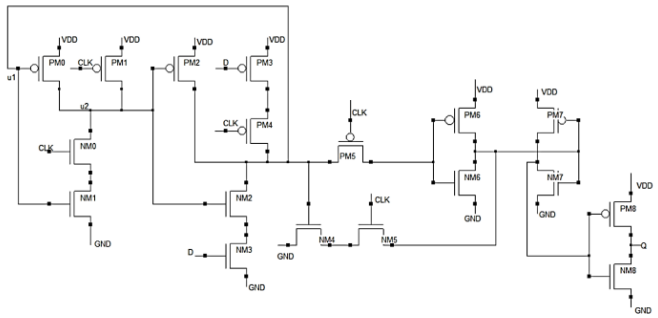

Fig. 12: Proposed Low-Power Mixed-Signal Flip-Flop

in realizing that the NM6 transistor, as the main latch, keeps the input stage in an active state. This condition activates the NM7 device, which controls the slave latching circuit. As such, the slave latch can be activated to release the primary latch. Thus, it eliminates the requirement of duplicating each n-FET device activated by the clock signal, and makes the circuit design simpler.

In general, the decrease in the number of transistors needed to make an entirely static configuration is for the sake of energy conservation, by reducing the amount of leakage currents. The total number of transistors in the proposal is 18 PFETs and 9 NFETs. The structure of the flip-flop (FF) circuit proposed in this work uses only complementary logic and pass logic transistors. This arrangement has achieved both objectives: increasing operating speed and reducing circuit complexity. Figures 13 to 16 show the operational behavior of the proposed FF circuit, showing various inputs such as data input, clock input, and so on. In the figures, the red cross symbols represent the inactive transistors, while the blue lines represent the discharge paths. The complexity of the circuit is measured by the number of transistors and the clock loading. The suggested flip-flop includes only 18 transistors, which simplifies the hardware of the existing architectures but still attains performance gains.

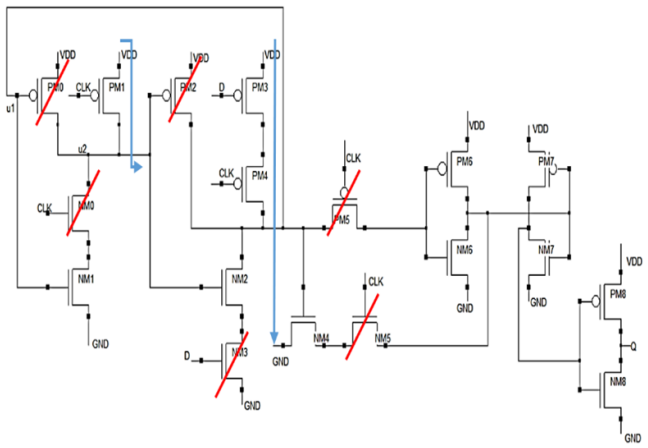

Fig. 13: Circuit Operation of Proposed FF When CLK = 0; D = 0.

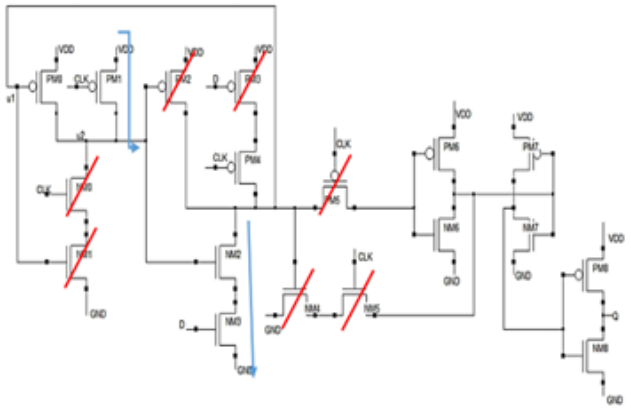

Fig. 14: Circuit Operation of Proposed FF When CLK = 0; D = 1.

Design of 2×1 MUX

Figure 17 shows the setup of a fully functional 2×1 multiplexer (MUX) used in this investigation. The devices PM1 and NM1 are integrated to implement a MUX that uses GDI technology. The main drawback of the hybrid MUX is that they do not have enough capacity to take high voltage signals. To increase the range of output voltages that can be obtained, NM2 has been connected in parallel with the M3 device.

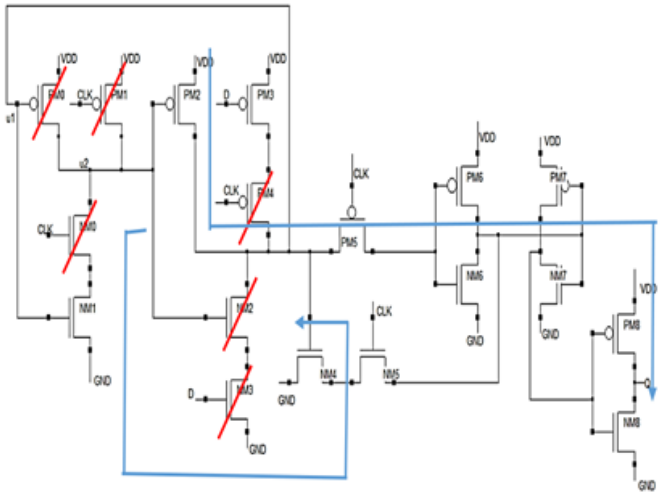

Fig. 15: Circuit Operation of Proposed FF When CLK = 1; D = 0.

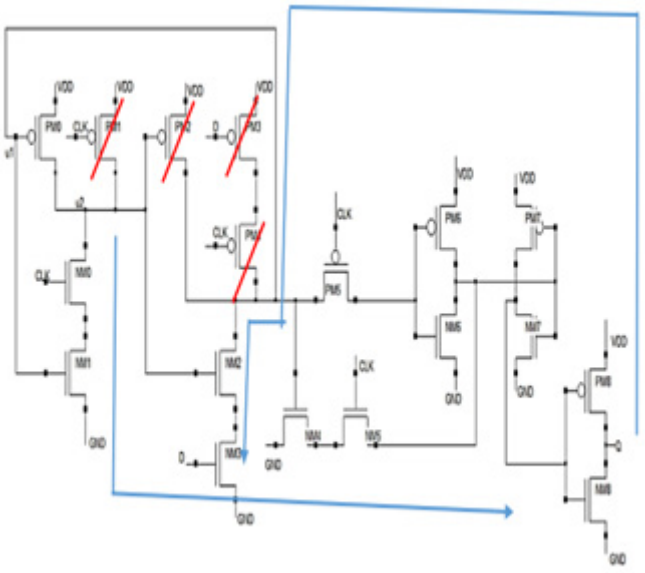

Fig. 16: Circuit Operation of Proposed FF When CLK = 1; D = 0.

Design of an AND Gate

The operational characteristics of the AND gate are described in Figure 18. The AND gate has been implemented on GDI (Gate Diffusion Input) logic. The inputs, which are configured on both PFET and NFET, are interconnected at the AND gate, which gives the input represented as A. The source of PFET and NFET are connection to the ground and input B, respectively. The drain terminals of both the transistors are combined to form the output node.

Simulation Results

All simulations were conducted in Cadence Virtuoso at the same operating conditions for reproducible results. The dimensions of the devices, supply voltage, temperature span, and process corners were kept constant across all the analyzed flip-flop architectures. The same stimulus signals and loading conditions were used to perform transient analyses for fair comparison between proposed and existing designs. The proposed

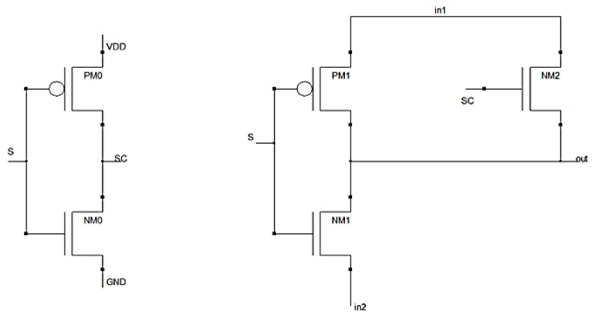

Fig. 17: Mixed logic based 2x1 MUX

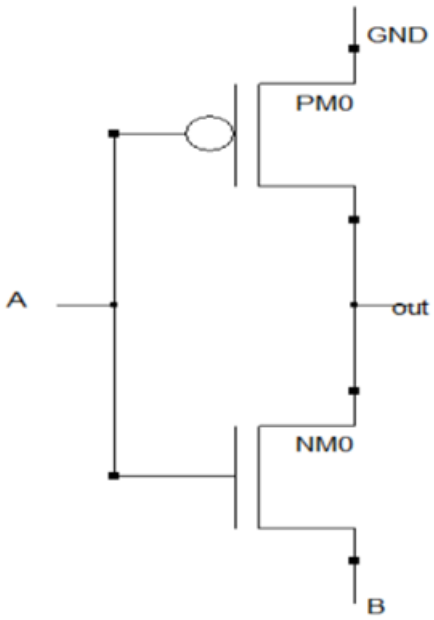

Fig. 18: Schematic 2-Input AND Gate.

counter and its constituent components were evaluated to compare their performance with other 18 nm devices. Extensive investigations were carried out to evaluate the power consumption, propagation delay, process variation sensitivity, physical area, and reliability of the proposed counter. This work simulates the currently available flip-flop topologies, as well as the proposed flip-flop and counter architecture, in FinFET 18 nm technology. A supply running at 0.7 V is able to lower the ambient temperature to around 27°C. A summary of the computational metrics used is provided in Table 1.

The characteristics that are relevant to the manufacturer of integrated semiconductor devices tend to have statistical distributions. The abbreviation PVT refers to the three main variables: Process, Voltage, and Temperature. These characteristics, commonly referred to as corner points, exercise a direct influence on the operation of each of the individual logic cells. PVT corner points are used as a reference for determining the best operational conditions for a silicon die. Such states are sometimes referred to as “square corners.”

Within the scope of process corner nomenclature, the traditional lexicon uses two-letter identifiers. The first letter of the designation indicates an N-channel field effect transistor (FET) corner, and the second letter of the designation indicates a P-channel FET corner. Corner types may be grouped into three main categories: fast-fast (FF), typical-typical (TT), and slow-slow (SS). Both device families show similar sensitivity to the effects of these corners, often resulting in a detrimental effect on circuit logic performance. The operational conditions of a device are determined by the applied voltage (commonly expressed as the die voltage “V”) and the operating temperature (T), primarily. Temperature can vary from −25 to 75°C. Alterations in PVT parameters have a significant impact on the behavior of the flip-flop cells, as well as on their power consumption, response latency, and efficiency.

Table 1. Parameters setup for simulation.

Parameter	Value
Technology	18 nm
Device	finFET
Supply Voltage(V)	0.7V
Analysis done	Transient analysis
Transistor Dimensions (W/L ratio)	NFET:1/1 PFET:2/1
Temperature (°C)	27

A detailed investigation of the PVT variations has been carried out for both the proposed flip-flop designs and those in the literature to provide accurate comparative analyses. The investigation analyzed the differences inherent in the TT, SS, and FF process corners. The research took advantage of a wide range of representative cells that could be compared. Conducting an assessment of process corners can greatly help by indicating and characterizing the parametric variations as much as possible. In this lack, the focus is limited to the design and simulation of current and proposed flip-flops to verify the intentional functionality of the proposed flip-flop with regard to its power consumption and speed. The entire work was done in Cadence Virtuoso in the node of the 18 nm finFET technology. Existing flip-flop architectures were simulated with the proposed design, and performance parameters such as power and delay were calculated. Subsequent PVT analyses were conducted to provide information on the performance of the devices over a range of process, voltage, and temperature conditions. The PVT analysis shows that the design has robustness against process, voltage, and temperature variation. The transient simulation waveforms of the proposed flip flop are given in Figure 19.

The transitional simulation results of the suggested mixed logic 2×1 multiplexer are shown in Figure 20. The methodology uses input signals in1, in2, and the line of selection S, as shown in Figure 20. The computed resultant signal y has a full swing characteristic. When the selection line S is set to a logical high, then the output y is determined by the input in 2 and vice versa.

The waveforms of the reconfigurable Johnson counter are shown in Figure 21. Whenever the mode has been set to one, the counter executes the counting operation.

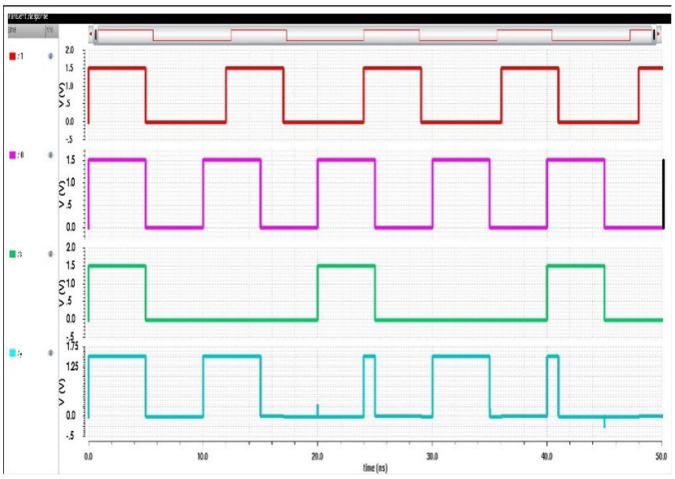

Fig. 19: Transient Simulation Waveform of Proposed FF.

In this configuration, after executing the CLK signal and setting the RST signal to zero, the counter starts the operation of initialization of all flip-flops. Whenever the RST signal has been set to one, the counter performs its normal counting function. When the mode(s) is(are) off, a counter is incremented or decremented by taking the last bit of the vector being counted and writing it into the first position. Each neighboring bit of each Johnson vector alternates with 0 and 1, that is, keeping the single hop characteristic of the adaptable Johnson counter into the sequence which it produces.

Analysis of Proposed FF

Efficient power utilization is especially important in low-power applications, since it allows multiple processes to be executed at the same time, which work synergistically for optimal performance, improving the effectiveness of

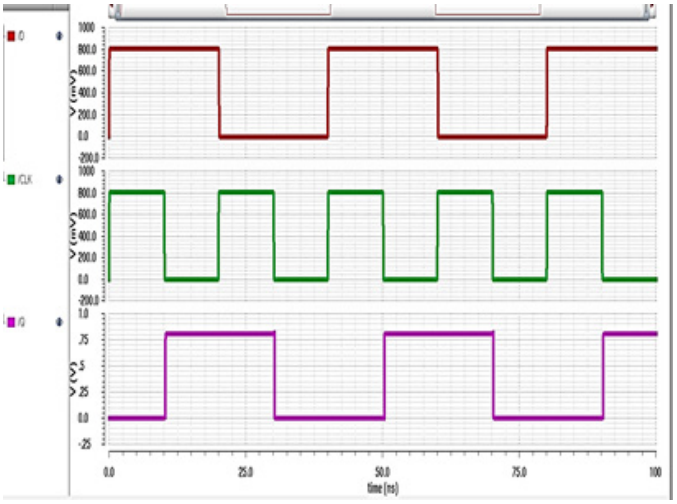

Fig. 20: Transient Simulation Waveform of Mixed Logic 2×1 MUX.

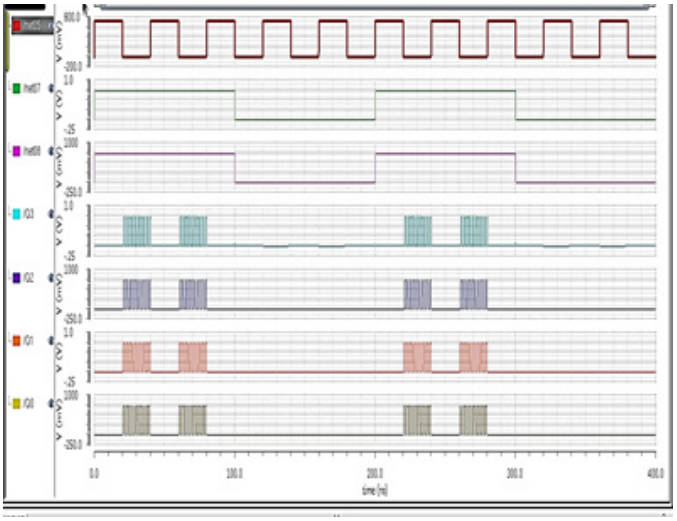

Fig. 21: Transient Simulation Waveforms of Proposed 4-bit Reconfigurable Counter.

the specific process and system throughput. The next few sections will analyze the power consumption features of the proposed architecture compared to the currently deployed flip-flops, and those that are often recommended to be used at the level of the entire system. The robustness that has been observed in the corners of TT, SS, and FF processes can be ascribed to the better channel control and the lower variability nature of FinFET devices. FinFET structures are less susceptible to process-induced fluctuations in parameters, hence, the observed constant power and delay characteristics of the proposed flip-flop and counter architectures. Figure 22 shows the average power consumption in the different operating stages.

The proposed configuration for the flip-flop circuitry consists of exclusively complementary logic and pass-logic transistors thereby reducing power consumption in terms of smaller number of PFET transistors and implementation of mixed logic and also minimizing the circuit complexity. According to Table 2, the proposed flip-flop consumes at least 45% less power than previous implementations for all process corners. Figure 22 shows this result and is also shown in Figure 23 that the suggested flip-flop power consumption is less than other devices in a wide range of supply voltage between 0.7 and 1.0 V. Table 3 also shows that the proposed flip-flop of feed-forward sense is achieved to minimize the power (15% reduction) with respect to the previous designs independent of supply voltage.

The proposed flip-flop had less power consumption compared to conventional design over the whole temperature range from −25 to 75 °C (Figure 24). The proposed flip-flop had at least 35% power consumption reduction with temperature variations regardless of the values (Table 4). The suggested arrangement of the flip-flop circuitry consisted of only complementary logic and pass-logic transistors. This arrangement was successful in reducing power consumption, by reducing the number of PFET transistors, using mixed logic, and reducing circuit complexity.

According to the results of the PVT evaluation, the data show that the proposed flip-flop cell has the ability to achieve the expected power consumption requirements. A comparatively low statistical variance in Monte Carlo simulations also confirms the appropriateness of FinFET technology in designing nanoscale sequential circuits. The multigate design eliminates random variability effects, so that consistent circuit operation is possible even when there are variations in the device parameters. A Monte Carlo simulation was used to statistically

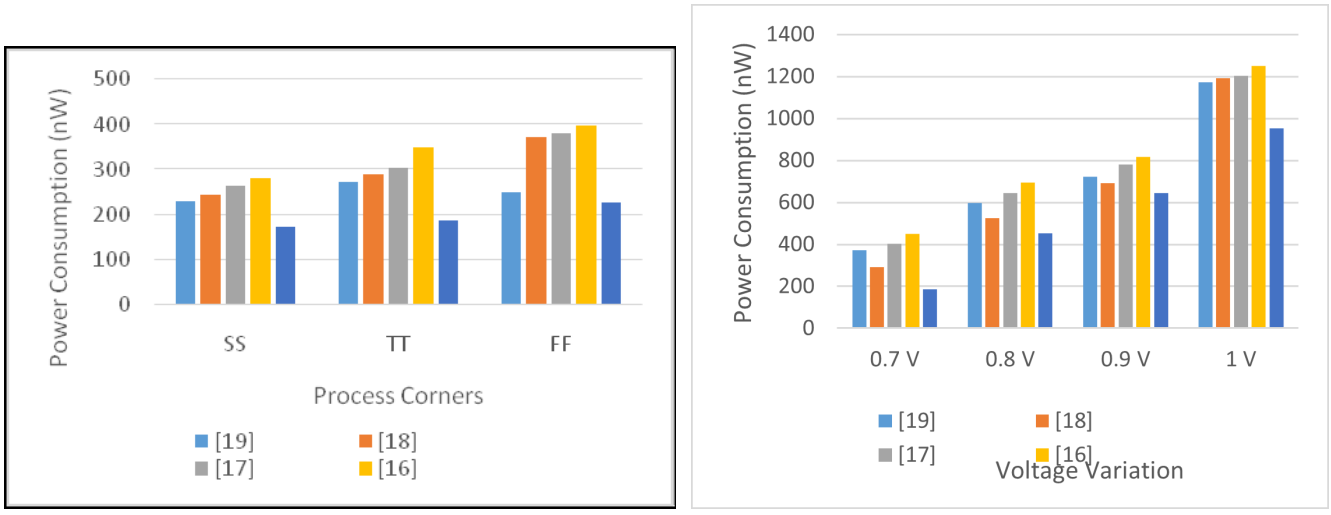

Fig. 22: Power Consumption of the Proposed Flip-Flop (FF) Compared to Current FFs under Different Process Variations.

Table 2. Performance analysis of power consumption of the proposed flip-flop (FF) w.r.t current FFs for various process variations.

Power Consumption (nW) in various process corners	[20]	[21]	[22]	[23]	Proposed FF
SS	230.21	245.12	263.21	281.72	172.28
TT	271.61	290.91	303.92	349.18	186.7
FF	249.11	371.36	381.21	398.12	228.23

evaluate the proposed flip-flop. The computational model consisted of 200 samples and had a standard deviation(s) of 3. Results of a Monte Carlo study which investigated power utilization during the operation of the flip-flops is shown in Figure 25. The power consumption of the suggested flip-flop cell is varied by about 10% during the working period.

This study aims to reduce the latency between the input and output signals in the modern flip-flop circuit by removing the PFETs in the slave circuit, resulting in reduced overall circuit latency. The projected delay and efficacy meet the specifications laid down for VLSI technology. The proposed circuitry enhances input to output delay performance and logical strategies to reduce the number of devices. The goal of the PVT investigation is the assessment of the flip-flop, as demonstrated, and the investigation of its resilience to different physical conditions. Figure 26 shows the comparison of the proposed and conventional flip-flops for each corner, hence taking into consideration the variation of the process delay. This study assesses the input-to-output delay over a temperature range of −25 to 75 °C. A corresponding variation in delay with temperature is given in Figure 27. The proposed flip-flop configuration uses only complementary logic and pass transistor logic, and thus brings about power reduction due to reduced PFET

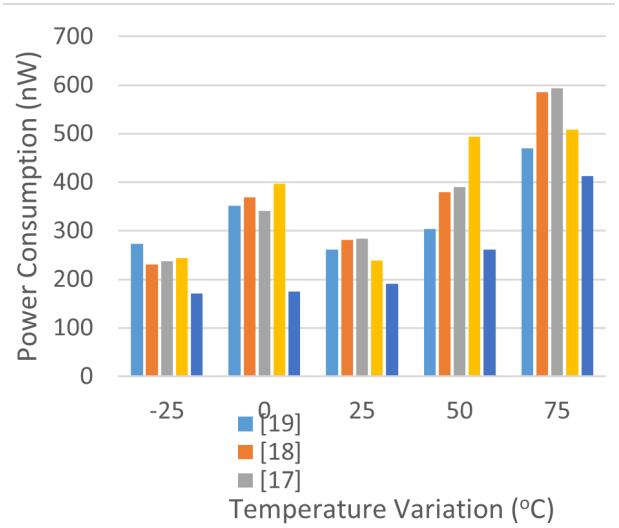

Fig. 23: Power Consumption of the Proposed Flip-Flop (FF) Compared to Current FFs under Different Supply Voltage Variations.

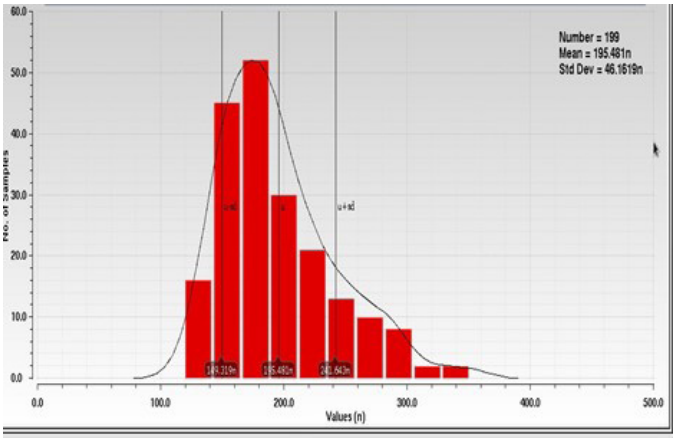

Fig. 24: Power Consumption of the Proposed Flip-Flop (FF) Compared to Current FFs under Different Temperature Variations.

Table 3. Performance analysis of Power consumption of the proposed flip-flop (FF) w.r.t current FFs for various supply voltages.

Power Consumption (nW) at various supply voltages	[20]	[21]	[22]	[23]	Proposed FF
0.7 V	371.61	290.91	403.92	449.18	186.73
0.8 V	598.12	524.16	645.81	694.1	453.1
0.9 V	721.29	691.11	781.36	816.1	644.1
1 V	1171.61	1190.91	1203.92	1249.18	954.3

Table 4. Performance analysis of power consumption of the proposed flip-flop (FF) w.r.t current FFs for various temperature variations.

Power Consumption (nW) at various temperatures (°C)	[20]	[21]	[22]	[23]	Proposed FF
−25	273.4	231.16	237	244.6	170.47
0	351.9	369.2	341.3	396.9	174.54
25	261.61	280.91	283.92	239.18	190.45
50	304.1	379.33	389.8	494	261.05
75	469.5	585.3	593.2	509	413.39

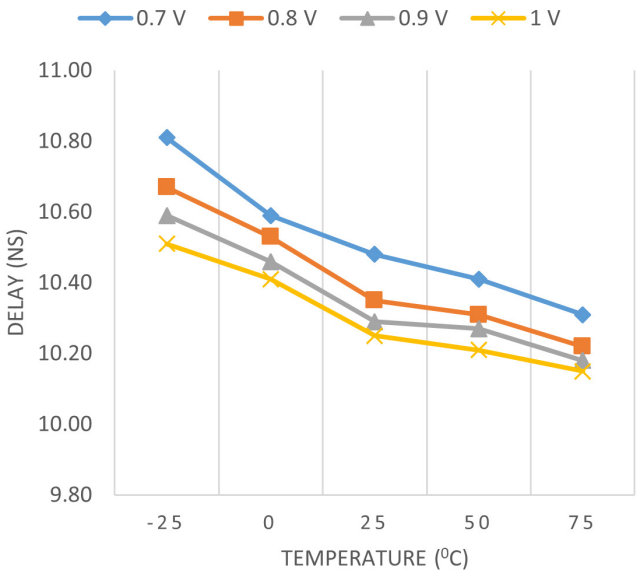

Fig. 25: Monte Carlo Computation of Power Utilization in Recommended FF.

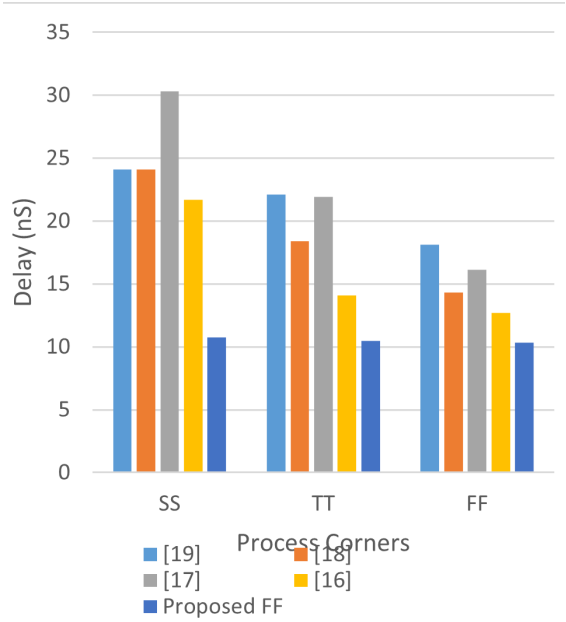

Fig. 26: Power Consumption of the Proposed Flip-Flop (FF) Compared to Current FFs under Different Process Variations.

number and mixed logic and simultaneously reduces circuit complexity. Table 5 shows that the proposed flip-flip works at least 20% faster than the existing alternatives for all process corners.

A Monte Carlo computer model was used to statically evaluate the proposed flip-flop. The computational experiment was developed with 200 samples, whose standard deviations were all three. Figure 28 shows the results of the Monte Carlo analysis to investigate the propagation delay during the operation of the flip-flops.

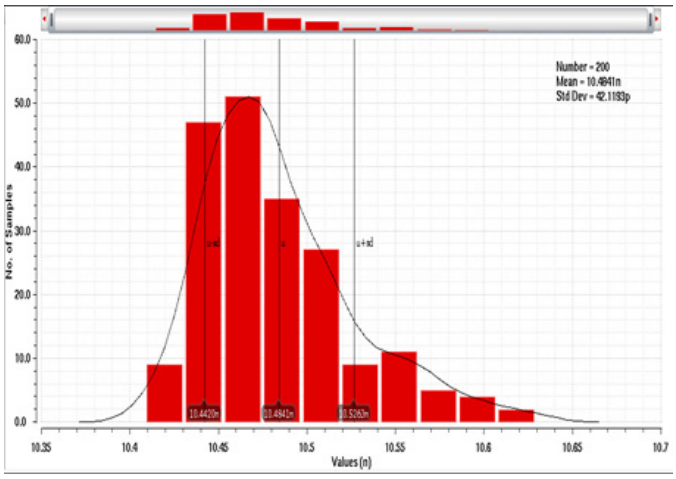

Fig. 27: Delay of Recommended FF w.r.t Temperatures and Supply Voltages.

Table 5. Performance analysis of the delay of the proposed flip-flop (FF) w.r.t current FFs for various process variations.

Delay (ns) in various process corners	[20]	[21]	[22]	[23]	Proposed FF
SS	24.12	24.1	30.3	21.7	10.77
TT	22.1	18.4	21.9	14.1	10.48
FF	18.1	14.3	16.11	12.7	10.34

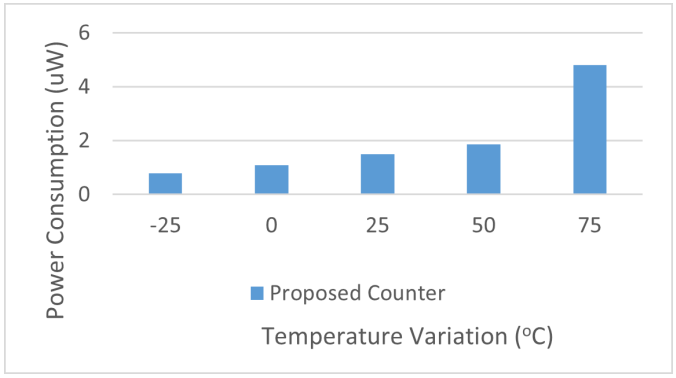

Fig. 28: Monte Carlo Computation of Power Utilization in Recommended FF.

The delay time of the candidate flip-flop cell changes by about 10% during its operation.

Power consumption and operating speed in digital circuits have a trade-off between them. Faster clock frequency decreases the propagation delay because the switching activity is faster, but increases the dynamic power consumption more. This trade-off is reduced by the suggested flip-flop design that can achieve a delay improvement with a small power overhead by minimizing switching capacitance and the number of transistors. Thus, the performance analysis is viewed through

the prism of the power delay trade-off as opposed to the single parameter optimization.

As shown in Table 6, increasing clock frequency from 0.05 to 0.2 GHz reduces propagation delay from 10.48 to 9.56 ns, while power consumption increases from 186.7 to 269.73 nW due to increased switching activity. This behavior confirms the expected power-speed trade-off in synchronous digital circuits. As shown in Tables 3, 5, and 6, the results show an increase in the clock rate from 0.05 to 0.2 GHz, which causes the delay to decrease from 10.48 to 9.56 ns while the power consumption increases from 186.7 to 269.73 nW. On the other hand, by decreasing the supply voltage, one reduces power consumption at the cost of increased delay. The design shown in Table 6 provides a reasonable compromise between power consumption and delay; however, the evaluation of the trade-off shows that it is possible to optimize it even further by adjusting the clock rate and the source voltage.

Analysis of Proposed Reconfigurable Counter

From Section 4.1, a section analyses the flip - flops (FFs), there is a superior performance of the proposed FF in terms of power consumption and propagation delay.

Table 6. Performance analysis of delay and power consumption of the proposed flip-flop (FF) for various clock frequency variations.

Clock Frequency (GHz)	Power Consumption (nW)	Delay (ns)
0.05	186.7	10.48
0.1	232.82	9.83
0.2	269.73	9.56

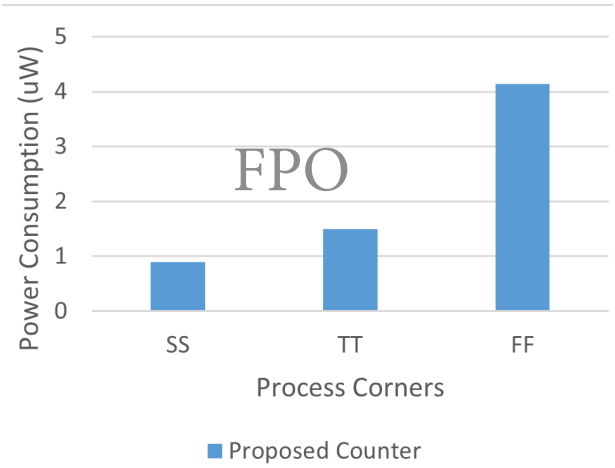

Fig. 29:

Consequently, the proposed FF was incorporated in the 4-bit reconfigurable counter. Furthermore, a process, voltage and temperature (PVT) analysis of the 4-bit reconfigurable counter was performed in order to assess the operational stability of the counter.

Figures 29 to 33 showed that the proposed 4-bit reconfigurable counter met the PVT specifications. It used less power in terms of lower power consumption and had slower operation at the SS corner, in comparison with its operation at the FF corner. Furthermore, the higher the temperature the higher the power consumption and the lower the delay. Also, the comparison of proposed counter with respect to existing counter architectures is shown in Table 7.

According to Table 7, the earlier literature focused primarily on either counter speed improvement or flip-flop optimization in isolation. By contrast, the suggested design merged with the reconfigurability of architectural

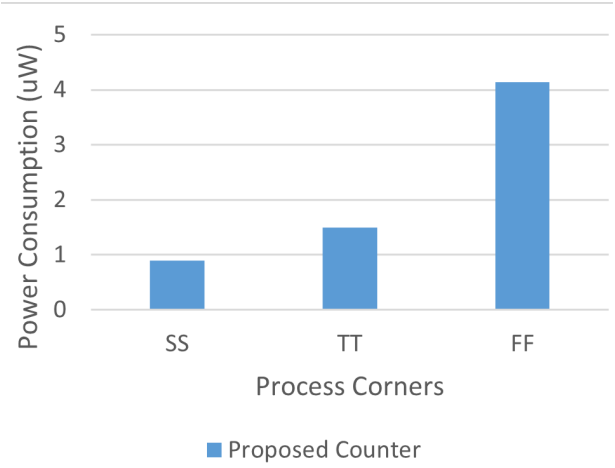

Fig. 30: Power Consumption of the Proposed 4-Bit Counter under Different Supply Voltage Variations

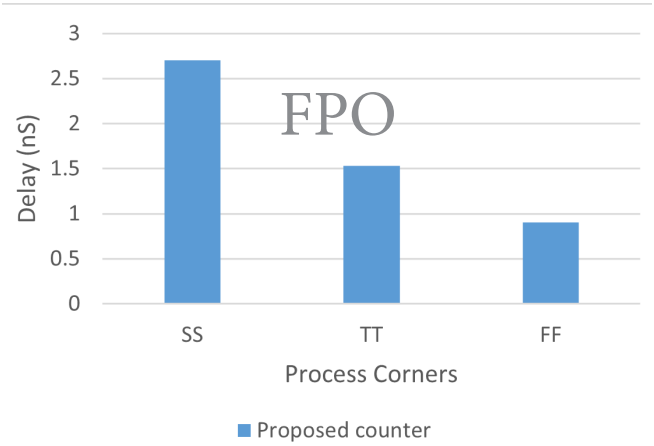

Fig. 31: Power Consumption of the Proposed 4-bit Counter under Different Temperature Variations.

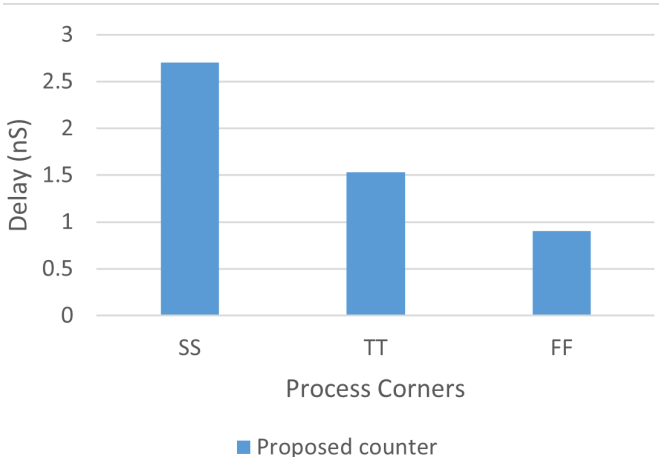

Fig. 32: Power Consumption of the Proposed 4-bit Counter under Different Process Variations.

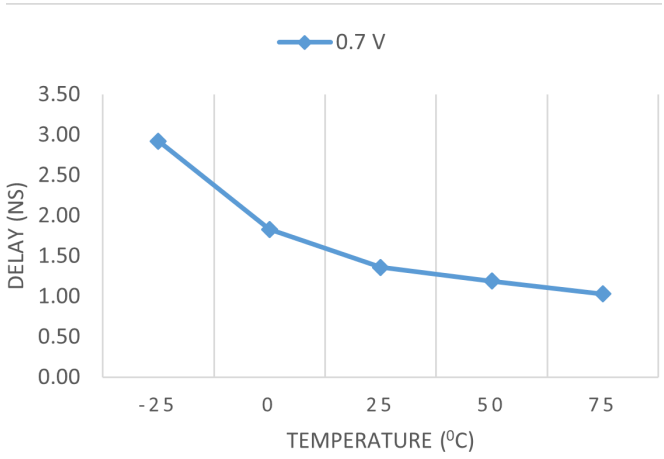

Fig. 33: Delay of Recommended 4-bit Counter w.r.t Temperatures and Supply Voltages.

Table 7. Comparison of existing counter architectures.

Work	Counter Type	Reconfigurable	Power Improvement	Delay Improvement	Area Complexity
[1]	LFSR Counter	No	Moderate	Moderate	High
[4]	High-Speed Counter	No	Limited	High	High
[15]	FF Optimization	No	Improved	Improved	Medium
Proposed Work	**Reconfigurable Johnson Counter**	**Yes**	**45% reduction**	**20% faster**	**Low (18T FF)**

design with the optimization at the transistor level. The switching capacitance was minimized by using a mixed-logic flip-flop, reducing the number of transistors and allowing better delay performance. Also, the addition of mode-based operation provided functional flexibility that was not present in traditional implementations of Johnson counters.

Conclusion

This paper provides the design and analysis of a 4-bit reconfigurable Johnson counter designed in Cadence Virtuoso with the use of 18 nm FinFET technology. To operate at low power consumption and high speed, a mixed-logic flip-flop using complementary logic and pass-transistor technology is offered that has less hardware complexity. The proposed flip-flop has only eighteen transistors, thus reducing the complexity of the circuit without compromising the reliability of the functionality.

The simulation outcomes show that the proposed design shows a large power reduction compared to the current flip-flop designs with variation in process, voltage, and temperature. There is also an improvement in propagation delay, which leads to an improved power-to-delay trade-off, as opposed to the independent optimization of performance measures. Monte-Carlo and PVT analysis is a confirmation that it operates well and is robust in real operating conditions. The choice of FinFET technology is an important factor in the realization of lower leakage power and high variability tolerance, which is proven by PVT and Monte-Carlo analysis.

The designed flip-flop can be used to provide energy-efficient counting with similar performance under varying operating conditions when incorporated into the reconfigurable Johnson counter. The findings confirm that FinFET technology, together with mixed-logic architecture, offers a viable method in designing low-power and scalable sequential circuits that are applicable in nanoscale VLSI applications. The main novelty of the work is the integration of reconfigurable Johnson counter architecture with mixed-logic FinFET-based flip-flop design to improve energy efficiency, delay performance, and functional flexibility simultaneously.

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