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Research Article

Design Of Clocked Jk Flip Flop Using Air Hole Structured Photonic Crystal

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ABSTRACT

In this paper an advanced air-hole type photonic crystal is used to design a clocked JK flip flop. A uniform GaAs photonic crystal that has the refractive index of 2.95 with air hole structure is utilized. Photonic crystal is created with multi-mode interference (MMI) for three input ports which represent three inputs Clock, J and K. The given structure is resulted with 8.657 contrast ratio and the power output is 6.24dB. The response time of the structure is less than 0.27 ps. The overall design and the results are discussed through the experimental implementation and the numerically simulation to confirm its operation and feasibility. The response time of the structure is very less. The simplicity of the crystal, contrast ratio, power output and quick response time makes more suitable to be a part of optical integrated circuits.

Keywords: Contrast ratio (CR), Photonic Crystal (PhC), air hole structure.

Introduction

In the ongoing decade, Analysts are focusing more on the advancement of optical-based rationale plans to improve the rapid exercises in media transmission frameworks and systems in the coming decade. Because of the rapid nature of light, the telecom division as well as electronic calculating frameworks, which may not meet the interest of quick registering because of their constrained abilities, require replacement with optical methods.

Because of the recognition of terahertz optical signs, data handling at terahertz speed is possible with optics. Analysts have investigated optical devices energised by the advancement of non-straight materials and other semiconductor-based advancements toward this methodology. Semiconductor optical intensifier-based systems are at the cutting edge of optical-based intelligent and number-crunching plans.

In any case, aside from the unavoidable unrestricted outflow of commotion, power utilisation and speed remain the major constraints in these plans. Non-linearity devices are influenced by high force utilisation, but they have numerous other applications, and optical devices demonstrated a lot of difficulty in providing exceptionally close channel dividing. To overcome these impediments and as part of testing research, researchers have devoted their time and efforts to the utilisation of reasoning capacities on photonic crystals stage because of its exceptional optical properties. Because of unrivalled advantages like rapid, low force utilisation, and minimization, photonic crystal is such a promising territory that can give a conspicuous space to the acknowledgment of rationale devices. They can control, guide, and point the light as far as possible on a manometer scale. In the plan of rationale devices, numerous ideas such as interference, reverberation, and self-collimation have been presented. Among these, the multi-mode interference (MMI)-based plan has its own and critical spot due to high contrast ratio (CR) and size minimization. [1]

MMI devices are important components of photonic integrated circuits due to their low misfortune, low polarisation reliance, and high optical transfer speed. These structures have a wide range of applications, Including wavelength multiplexers/demultiplexers, optical switches, logical gates, and so on. Because of the massive scattering in photonic crystals, the structure of these MMI devices based on photonic crystal waveguides is much smaller than that of traditional MMI devices.

"Addressing the electronic interconnect barrier through a technology like photonics is essential in keeping Moore's law on track," says Vernon Turner,

senior vice president at IDC. In other words, electronic-based chip I/O is running out of steam, throttling bandwidth and acting as a bottleneck.
In this paper, an essential clocked JK-flip flop is proposed using a two-dimensional photonic crystal-based (2D PhC) MMI waveguide as the ports, along with three input and two yield waveguides. The proposed structure's central MMI location is responsible for the interference of light signals applied through the information ports and provides the integral yields at the predetermined ports.

The recreation results show a good CR at both the yield with a delay and the reaction time in nanoseconds. To construct the postponement, the fundamental structure's information and yield waveguides are stretched out with twist waveguides, which offers a yield with nearly a similar CR but at the expense of size. [2]

Fundamental Clocked Jk Flip-Flop

To begin, flip flops are two stable state devices that are used to store a binary bit of data. There are numerous electronic flip flops available. JK Flip flop is one of the most important devices for storing data.

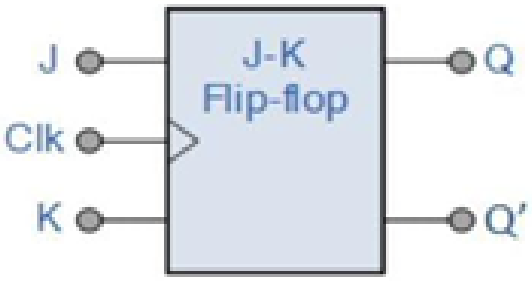


Fig.1: Symbol of clocked JK flipflop

In addition to the clock pulse, there are three inputs J, K. The output is set to logic 1 by 'J,' and the output is reset by 'K.' (sets to logic 0). 'Clock' signal acts as enable signal to control the operation of JK Flip flop. The JK Flip flop has two outputs, which are denoted by the letters 'Q' and Q. Figure-1 depicts the Clocked JK flip flop symbol.
When J is digital 'logic 1' and K is digital 'logic 0', the output of the clocked JK flip flop is digital 'logic 1', and when J is digital 'logic 0' and K is digital 'logic 1' while the clock pulse is enabled, the output of the flip flop is digital 'logic 0'. The output of the clocked JK flip flop is holed during the other input combinations (Past output exists). When all inputs are set to 'digital logic 1' and the clock is enabled, the output is the complement of the previous output; thus, this state is used in a few specific applications such as counters. Figure 2 depicts the truth table of a clocked JK flip flop. [3]

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

Fig.2: Truth table of clocked JK flip flop

In the truth table, Q denotes previous output, and Q' denotes the complement of previous output. In the toggle state, the flip flop output is a complemented version of the previous output.

A flip flop is a type of electronic component that stores a single paired binary digit. Among the various types of flip flops available, the JK-flip flop is an important component used in the design of registers

that can store a collection of two-fold bits, or a double number of n bit sizes. The JK-flip flop is made up of three information sources, J, K, and Clock, as well as two integral yields, Q and Q' When the input Clock is stated, the yield Q follows J and is opposite to K, as shown by the truth table.
Because it is gated by a clock, it is also known as a timed or clocked JK-flip flop. Clock information sources can be edge activated or level activated. Positive going edge or positive level is considered rationale '1', while negative going edge or negative level is considered rationale '0'. The flip flop is activated and the information is handled at the predetermined clock edge or level (for whatever reason it was structured). Clock input is thought to be the positive level activated in the proposed JK-flip flop, which is rationale '1'. [4]

Prpopsed Clocked Jk Flipflop

The structure of an optically based timed JK-flip flop is based on MMI and is made in photonic crystal. The fundamental structure in an MMI-based plan is a waveguide or MMI area, which can support a large number of modes and is linked with access waveguides at the front end and back end to dispatch and recuperate light from that essential MMI waveguide.
These MMI devices are primarily reliant on self-imaging property, wherein the guided modes are activated in the MMI area and play a beneficial role. These energized fields alternately transmute along the proliferation path in the MMI region. The following equation can be used to determine the shortest coupling length of the MMI area.

$$L_c = \frac{\pi}{\beta_0 - \beta_n}$$

Where β0 and βn are the generating constants of the basic and nth request modes, respectively, and are determined from the scattering bends of the super modes in the MMI area. As shown in Figure-3, the proposed timed JK-flip flop structure is made up of a variety of 15*21 poles orchestrated in a square sort grid in air. It has three information ports, J, K, and Clock, as well as two yield ports, Q and Q'. J and K are the real ports for recognising the info bit examples, Clock is for the positive level activated clock input, and Q and Q are the integral yields.
Aside from the edge poles, where it is the grid consistent of significant worth 500 nm, the span r of the significant number of poles is increased to 0.5a. The range re of the edge bars in the MMI waveguide has been reduced to 0.5a in order to improve yield execution. The length of the MMI waveguide, also known as the coupling length Lc, is determined from the waveguide's scattering chart and is set to 8.2a, where Wn represents the waveguide with n number of poles evacuated to make a waveguide. [5]
The photonic band of the band outline is used to resolve the gaps (PBGs) of the photonic crystal cross section on which the waveguide is built. The Plane Wave Expansion (PWE) method is used to determine the band outline as well as the scattering bend. The band outline depicts three potential PBGs, one of which is in TM mode and the other two in TE mode. One of the two TE modes is chosen with the goal of changing the estimation of cross section steady a so that the frequency range can suit C-band.

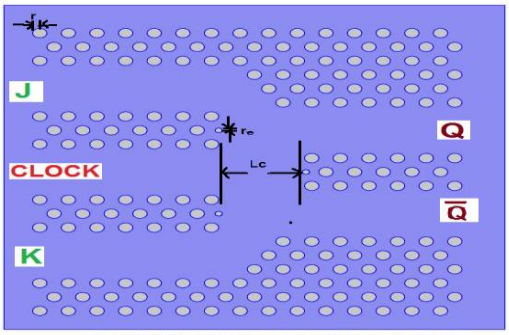


Figure-3: Structure of Clocked J K Flip Flop

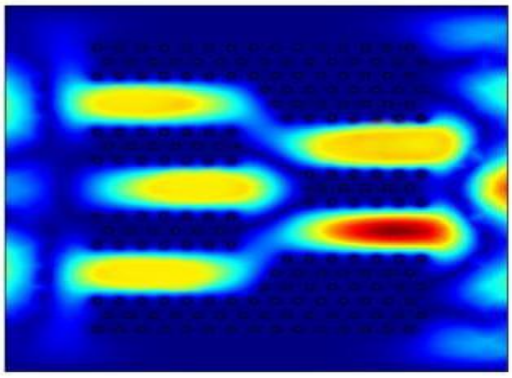
There are four potential guided modes from which the coupling length Lc can be determined: essential mode, first-request mode, second-request mode, and third-request mode. These guided modes are determined by first determining the working point (the point on the y-hub in the scattering outline where the dabbed line converges), which is dependent on the working frequency. The working point a/0 on the scattering graph is 0.367 based on the cross section consistent and working frequency 0 of 1650 nm in the proposed work.
At this working point, the comparing parameters associated with the guided modes are obtained from Figures and recorded in Table 1. The coupling length Lc is determined by the essential mode and the second-request mode (even mode), and it ensures that the three information light signals are properly coupled. At this coupling length, the three information light bars propelled perpendicular to each other at all

of the MMI waveguide's information ports will superimpose on the yield port of the waveguide that is inverse to the info port being energised with a light sign of zero stage. Along these lines, the MMI waveguide's yield port will receive more power. The MMI waveguide's other yield port will be left with a low or insignificant force. [6]

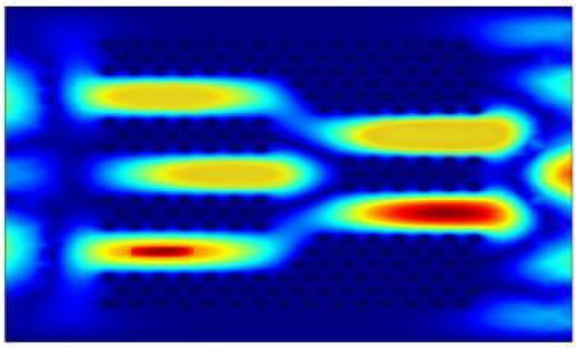
When only one information port is activated, a single image occurs at positive whole number products of beat length (L), which can be approximated to coupling length (Lc) in a photonic crystal-based MMI structure. So, at this coupling length, the yield port of the MMI waveguide will receive a solitary picture with high force while the other yield port will receive a low power. As a result, the coupling length in the proposed structures is kept at 8.2a, which is obtained from the hole between the focal points of both the outrageous edge bars in the MMI waveguide fewer multiple times the range of the edge poles (0.5a). According to the previously mentioned hypothetical viewpoint, the proposed JK-flip flop's Clock contribution is constantly energised with a light emission beginning stage.

When port J is not energised and port K is energised (implies J = 0 and K = 1), the single image of the light bar applied at the Clock input arrives at port Q', which is considered rationale '1', and the other port Q receives zero power, which is considered rationale '0'. When port J is energised and port K is not energised (implies J = 1 and K = 0) with zero stage, the Clock information is superimposed with that contribution at port Q and produces higher power, which is considered logic '1', while leaving a less or insignificant force at port Q', which is considered logic '0'. [7]

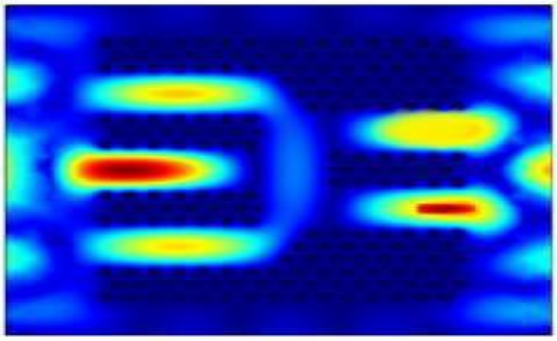
Results



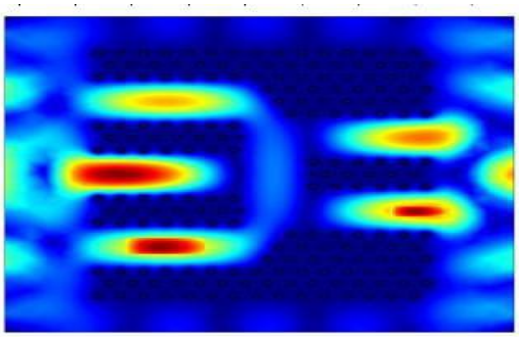
After completion of compute, we will get the output like this by giving the input TEST CASE1 (CLK:0; J:0; K:0), and we get output as (Q=0, Qn+1=1).



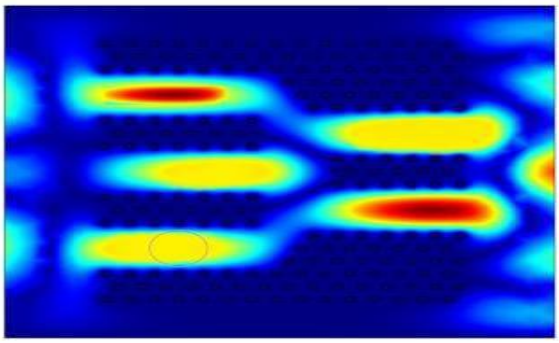
After completion of compute, we will get the output like this by giving the input TEST CASE4 (CLK:0; J:0; K:1), and we get output as (Q=0, Qn+1=1)



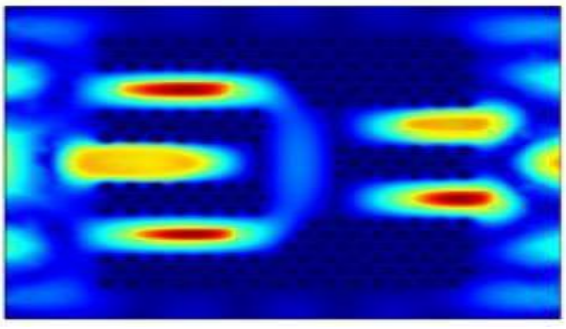
After completion of compute, we will get the output like this by giving the input TEST CASE2 (CLK:0; J:1; K:0), and we get output as (Q=0, Qn+1=1).



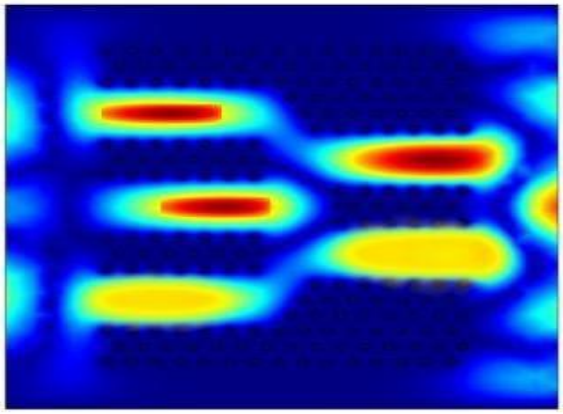
After completion of compute, we will get the output like this by giving the input TEST CASE3 (CLK:0; J:1; K:1), and we get output as (Q=0, Qn+1=1).



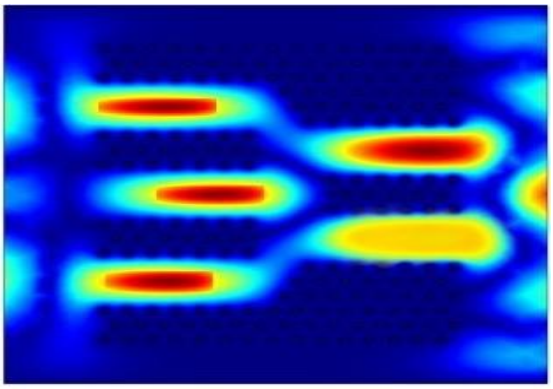
After completion of compute, we will get the output like this by giving the input TEST CASE5 (CLK:1; J:0; K:0), and we get output as (Q=0, Qn+1=1).



After completion of compute we will get the output like this by giving the input TEST CASE7 (CLK:1;J:0;K:), and we get output as(Q=0, Qn+1=1).



After completion of compute we will get the output like this by giving the input TEST CASE2 (CLK:1; J:1; K:0), and we get output as (Q=1, Qn+1=0).



After completion of compute, we will get the output like this by giving the input TEST CASE8 (CLK:1; J:1; K:1), and we get output as (Q=0, Qn+1=1).

Order of the Mode	Propagation Constant (β(2π/a))	Coupling Length Lc (in μm)
Fundamental	0.368	21.2a
First Order	0.326	18.6a
Second Order	0.283	8.2a
Third Order	0.173	2.5a

Table-1: Mode parameters of waveguide at working wavelength

The typical bars as well as the edge bars of the proposed flop structure of the JK-flip are advanced so far that the return transmission (e.g., output power and Pa is the applied information power, for Pout/Pa) may be less than 0.25 or more, to the aim of being considered separately as '0' and rational '1.' The adjustment of the sweeping bars will modify the output transmission and hence the ON-to-OFF CR of the JK-flip flop proposed. By using the associated conditions, the ON-to-OFF CR of the optical logic device can be establish.

$$CR = 10\log\frac{P_1}{P_0}$$

Where P1 is the power level of rationale '1' and P0 is the power level of rationale '0'. A high CR can be acquired by a huge separation in the yield power levels of rationale '1' and rationale '0'. A very low estimation of the force level of rationale '0' contributes more in accomplishing higher CR. The contrast ration details of Clocked JK Flip Flop can be seen in Figure 5. [8]

The range of the ordinary bars is up to 0.5a, such as 120 nm to obtain the pre-determined return transmission at both yields of rational '0' and rational '1.' Due to its incompatibility with specific ports, the variant in the typical polar range changes the rendered transmission at ports Q and $\bar{Q}$, so that the proposed structure stops working as a flip flop and, if J = 0, K = 1 and Clock =1, the reduction in the span of typical pole causes the rendering transmission to be adjusted away from its predefined rating "0".

Finally, both Q and $\bar{Q}$ ports, which do not match each other, can display the transmission. Therefore, when J=1, K=0 and Clock=1, the increase in the range of the common pole causes the yield transmission to be adjusted away from their pre-defined '1' rational qualities and the '0' rational in ports Q and $\bar{Q}$. If J = 1, K=1 and Clock = 1, the flip flop enters the toggle status.

Outputs Of Flipflops at Each Test Case.

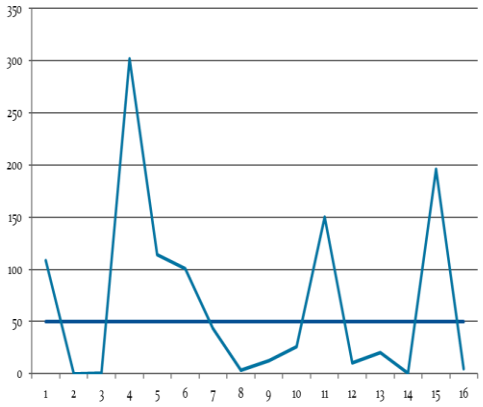


Fig.5: Contrast ratio details of clocked Jk flipflop

While we are designing this flipflop we will get a threshold value at the Y-axis 50. Above the value 50 are logic '1' and below the value 50 are logic '0'. The JK-flip flop stores a few binary data; it can be logic 0 or logic 1 and is referred to as clock pulse which is usually used to count the info-signal sequence.

The device has a very high counting speed. In picoseconds, the JK-flip optical flop gives delay, unlike the electronic JK-flip flop, which leads to nanosecond delay. For rapid workouts in large numbers of applications, such as media transmission systems and frames, optical processing etc, optical sign preparation plans are essentially implied.[9]

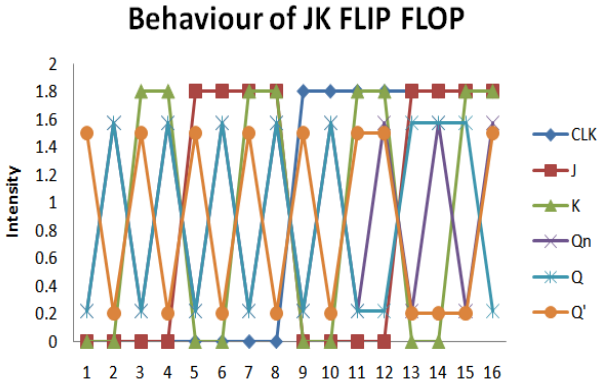


Fig. 6: Intensity of variations of JK flipflop at different input combinations.

The above figure shows the different input combinations of intensity variations for Jk flipflop. Every input and output have different symbolic notations. The output of flipflop at each test case between intensity and behavior of flipflop.

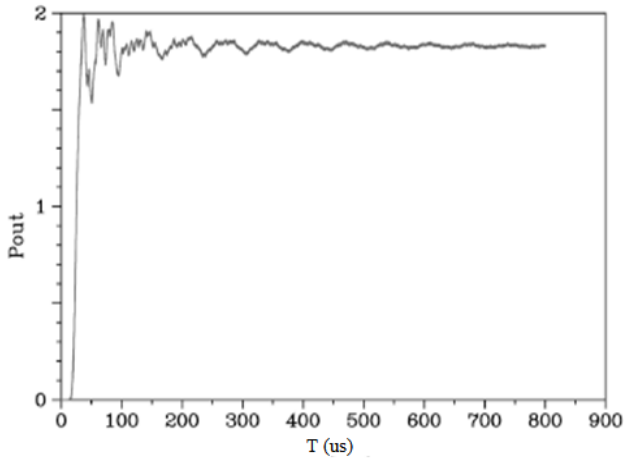


Fig .7: Response time of Flip Flop for change in output

The above figure shows the response time flip flop at each test case. Response time flipflop gives clear information for each and every input or each and every test case.

Table 2: Output Intensity at Q for different input combinations

CLK	J	K	Qn	Qn+1	Output Power at Qn+1
0	0	0	0	0	0.216
0	0	0	1	1	1.571
0	0	1	0	0	0.215
0	0	1	1	1	1.57
0	1	0	0	0	0.217
0	1	0	1	1	1.573
0	1	1	0	0	0.214
0	1	1	1	1	1.572

CLK	J	K	Qn	Qn+1	Output Power at Qn+1
1	0	0	0	0	0.218
1	0	0	1	1	1.572
1	0	1	0	0	0.217
1	0	1	1	0	0.215
1	1	0	0	1	1.572
1	1	0	1	1	1.571
1	1	1	0	1	1.573
1	1	1	1	0	0.214

Table 3: Output Intensity at Q' for different input combinations.

CLK	J	K	Qn	Qn+1	Qn+1'	Output Power at (Qn+1)'
0	0	0	0	0	1	1.498
0	0	0	1	1	0	0.204
0	0	1	0	0	1	1.496
0	0	1	1	1	0	0.203
0	1	0	0	0	1	1.497
0	1	0	1	1	0	0.205
0	1	1	0	0	1	1.498
0	1	1	1	1	0	0.204

CLK	J	K	Qn	Qn+1	Qn+1'	Output Power at (Qn+1)'
1	0	0	0	0	1	1.498
1	0	0	1	1	0	0.204
1	0	1	0	0	1	1.496
1	0	1	1	0	1	0.206
1	1	0	0	1	0	0.205
1	1	0	1	1	0	0.203
1	1	1	0	1	0	0.204
1	1	1	1	0	1	1.497

Contrast Ratio Truth Table

Table 4: CR of Clocked JK Flip Flop at both outputs

Q	Pout	CR		Q'	Pout	CR
0	0.216	8.657		0	0.204	8.568
1	1.571			1	1.498	

Q and Q'.

The contrast ratio (CR) of a display system is defined as the ratio of the luminance of the system's brightest shade (white) to that of the system's darkest shade (black). A high contrast ratio is an important feature of any display. It is comparable to dynamic range.

Static contrast ratio is the luminosity ratio comparing the brightest and darkest shade the system is capable of producing simultaneously at any instant of time, while dynamic contrast ratio is the luminosity ratio comparing the brightest and darkest shade the system is capable of producing over time (while the picture is moving). Moving from a system that displays a static motionless image to a system that displays a dynamic, changing picture slightly complicates the definition of the contrast ratio, due to the need to take into account the extra temporal dimension to the measuring process.

We have a desired formula to calcualte the contrast ratio value by using outputs of logic '1' and logic '0' for both Q and Q'.

$$CR = 10\log\frac{P_1}{P_0}$$

While we are observing the contrast ratio table, In pout, for logic '0' we will get the maximum value from truth table and for logic '1', we will get the minimum value from truth table for both Q and Q'. [10]

Advantages

The PhC-based optical logic gate has numerous advantages

- High operating speed
- High data transfer rate.
- Good contrast ratio.
- Small in size
- PhC-based optical gates are suitable for use in integrated optical circuits can be implemented by CMOS technology.

Applications

The proposed optical logic gates using photonic crystals can be used in many applications

- Used in optical communications
- Used in optoelectronic applications
- Used in instrumentation applications
- Used in bio sensor applications
- Counters, Frequency Dividers.
- Shift Registers, Storage Registers.
- Data storage.
- Data transfer.
- Optical logic gates have expected applications such as binary addition, header recognition, parity checking, addressing, demultiplexing, regenerating, encoders and switching with very high speed.

Conclusion

We proposed in this paper a key structure to use the clocked JK-flip flop on a photonic crystal base of a cross-sectional square type. The proposed structure consists of the MMI Waveguide as a central section in which the information light impedance occurs, and it is connected to the info and the result by direct waveguides. It is reconstructed using a time-area technique of limited distinction which was implemented individually with a CR of 8.657 and 6.24 dB at Q and Q at the yields below 0.27 ps. In this way, it may be concluded that, as a deferral component in frameworks, the proposed JK flip flop of an essential structure can be used as soon as possible.

Future Scope

Autonomous vehicles and factories in common use guided by laser detection and ranging (LiDAR) could become a reality and more efficient with photonics.

Real-time image recognition and AI informed decision making using optically enabled superfast

classical and quantum computers could be the near future.

Deep body soft tissue imaging for precise early disease diagnosis is possible with photonics.

De-carbonization with low impact photovoltaics, precision control of wind generation and ultra-efficient data storage and processing is possible with photonics in near future.

It could build Ultimately secure quantum communication and storage of the world's data. [11]

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