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Research Article

Design Of Clocked Hybrid (D/T) Flipflop Through Air Hole Paradigm Photonic Crystal

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ABSTRACT

In this paper an advanced air-hole type photonic crystal is used to design a clocked Hybrid D/T flip flop which works as both 'D Flip Flop' and 'T Flip Flop' by manipulating the control strobe or enable signal. A uniform Silica photonic crystal that has the refractive index varying from (1.55 to 1.40 for its transparent range 160nm to 3000nm) with air hole structure is utilized. Photonic crystal is created with multi-mode interference (MMI) for three input ports which represent three inputs Clock, D/T and control Strobe or Enable input. The response time of the structure is very less. The simplicity of the crystal, contrast ratio, power output and quick response time makes more suitable to be a part of optical integrated circuits.

Keywords: Contrast ratio (CR), Photonic Crystal (PhC), Air hole structure.

Introduction

In the ongoing decade, The idea of implementing this project Flip-Flops are digital circuits with two stable, self-maintaining states that are used as storage/ memory elements such as Random-Access Memory (RAM), Caches Memory and Read Only Memory (ROM). They are also very useful in the following electronic digital devices design; Sequence Detector, Data Synchronizer, Frequency Divider, Registers (data transfer), Counters and Registers in Central Processing Unit (CPU) for data transfer. They are derived from Sequential Logic Circuits which are the main electronics circuits that make the development of computers possible. The ability of computer systems to operate without the continuous human intervention is solely achieved through sequential logic circuits, the building blocks of Flip Flops.

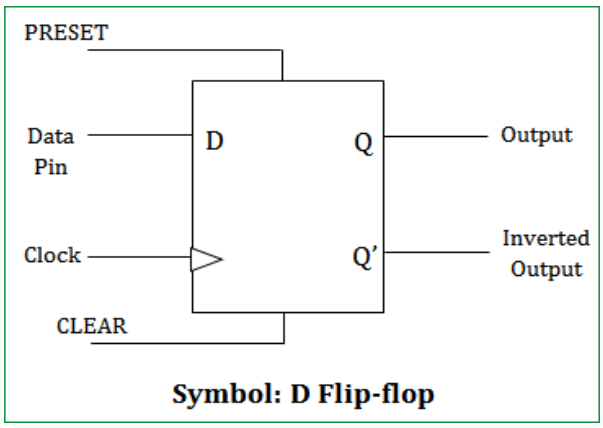
It has been observed that computer performance is primarily affected by the processor and memory. If either one reaches its limits (which may initially be the memory), the performance of the whole system degrades. As semiconductor technology advances, the performance gap between processor - the Central Processing Unit (CPU) and main memory - the Random Access Memory (RAM) has become one of the major issues in computer design. In the past 35 years, an exponential rate of improvement has been witnessed in semiconductor technology. The processor performance increases at a rate of 60% per year while the memory performance increases just 10% per year. This situation causes a 50% growing gap between processor and memory in the performance . If memory fails to keep pace with the processor's constant demands, the processor stalls in a wait state, and valuable processing time is lost. This imbalance has become one major bottleneck in further improving the computer performance. [1]

"Addressing the electronic interconnect barrier through a technology like photonics is essential in keeping Moore's law on track," says Vernon Turner, senior vice president at IDC. In other words, electronic-based chip I/O is running out of steam, throttling bandwidth and acting as a bottleneck.

Speed is the operative word when talking silicon photonics. Technological advances emerging from the world of silicon photonics have sped up dramatically. And, in turn, those advances are poised to deliver significant speed boosts in telecom and Internet applications. Fundamentally, silicon-photonic chip structures can be created using standard fabrication processes. Optical devices, on the other hand, are integrated into the chip alongside electrically driven elements. Given its speed implications, it comes as no surprise that electronics companies such as Fujitsu, IBM, Intel, and NTT are currently investigating silicon photonics as a future

design step toward maintaining Moore's Law as a credible benchmark of electronics progress.
The main object is we are using this project is to design flip flop which can work as D flip flop and T flip flop by manipulating the enable or control strobe this project also aims to give high output power and high contrast ratio with less response time which are also the major contents of the project. [1]

Fundamental Clocked D Flipflop
To begin, flip flops are two stable state devices that are used to store a binary bit of data. There are numerous electronic flip flops available. D Flip flop is one of the most important devices for storing data.



Symbol: D Flip-flop

A D flip-flop is a type of information storage device that has two stable states and a memory function. It is the most fundamental logic unit that makes up a wide range of sequential circuits, as well as an important unit circuit in digital logic circuits. D flip-flops are thus widely used in digital systems and computers. The flip-flop has two stable states, "0" and "1," which can be flipped from one stable state to the other in response to an external signal.

D flip-flops are made up of gate circuits and integrated flip-flops. There are two types of triggers: level triggers and edge triggers. The former can be triggered when CP (clock pulse) =1, whereas the latter is primarily triggered on the leading edge of CP (positive transition 0-->1). D flip-flops are commonly used and can function as a digital signal register, shift register, frequency division, and waveform generator, among other things.[2]

CP	D	Q	Q_{+1}	State
1	0	0	0	RESET
1	0	1	0	
1	1	0	1	SET
1	1	1	1	
0	0	0	0	NO CHANGE
0	0	1	1	
0	1	0	0	NO CHANGE
0	1	1	1	

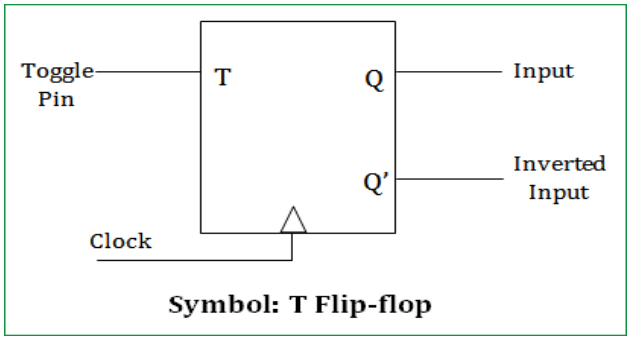
Truth Table of D flip flop

CP	D	Q_{+1}	State
1	0	0	RESET
1	1	1	SET
0	x	Q_n	NO CHANGE

Simplified truth table

When the clock signal is LOW, the input has no effect on the output state. For the inputs to become active, the clock must be set to a high value. As a result, the D flip-flop is a controlled Bi-stable latch, with the clock signal serving as the control signal. This is divided once more into positive edge triggered D flip flops and negative edge triggered D flip flops.
The D(Data) is the D flip-input flop's state. The Q and Q' represent the flip-output flop's states. According to the table, the output's state changes based on the inputs. The important thing to remember is that all of this can happen only in the presence of a clock signal. For the complementary inputs only, this works exactly like an SR flip-flop.

Fundamental Clocked T Flipflop.
To begin, flip flops are two stable state devices that are used to store a binary bit of data. There are numerous electronic flip flops available. D Flip flop is one of the most important devices for storing data.



Symbol: T Flip-flop

The term "Toggle" is defined by the letter "T" in T flip flop. To avoid an intermediate state, we only provide a single input called "Toggle" or "Trigger" in SR Flip Flop. This flip-flop now functions as a toggle switch. The complement of the current state output is used to change the next output state. This process is known as "Toggling"'.

We can create the "T Flip Flop" by modifying the "JK Flip Flop." The "T Flip Flop" has a single input, which is formed by connecting the inputs of the JK flip flop. T is the name given to this single input. In other words, we can make the "T Flip Flop" by converting a "JK Flip Flop." The "T Flip Flop" is also known as the "JK Flip Flop" with a single input.

The "T Flip Flop" is created by feeding the output of the AND gate into the NOR gate of the "SR Flip Flop." The "AND" gates' inputs, the current output state Q, and its complement Q' are returned to each AND gate. The toggle input is used as input for the AND gates.

The Clock (CLK) signal is connected to these gates. The toggle input in the "T Flip Flop" is a pulse train of narrow triggers, which changes the flip flop's output state. [3]

CP	T	Q	Q_{+1}	State
1	0	0	0	NO CHANGE
1	0	1	1	
1	1	0	1	TOGGLES
1	1	1	0	

Truth Table of T flip flop

CP	T	Q_{n+1}	State
1	0	Q_n	NO CHANGE
1	1	$\overline{Q}_n$	TOGGLES

Simplified Truth Table of T flip flop

The T flip flop is a modified version of the JK flip flop. The Q and Q' represent the flip-output flop's states. According to the table, the output's state changes depending on the input. The important thing to remember is that all of this can happen only in the presence of a clock signal. This works differently than the SR and JK flip-flops for complementary inputs. This only has a toggle function.

When you need to reduce the frequency of a clock signal, T flip-flops come in handy: If the T input is held at logic high and the original clock signal is used as the flip-flop clock, the output will change state once per clock period (assuming that the flip-flop is not sensitive to both clock edges). As a result, the frequency of the output clock will be half that of the input clock

When the incoming trigger alternately changes the set and reset inputs, the "T Flip Flop" is toggled. To complete a full cycle of the output waveform, the "T Flip Flop" requires two triggers. The frequency of the "T Flip Flop" output is half that of the input frequency. The "T Flip Flop" circuit functions as a "Frequency Divider Circuit." [2]

Proposed Clocked Hybrid (D/T) Flipflop

An optically based timed (D/T)-flip flop structure is based on MMI and is made of photonic crystal. The fundamental structure in an MMI-based plan is a waveguide or MMI area, which can support a wide range of modes and is linked with access waveguides at the front and back ends to dispatch and recuperate light from that fundamental MMI waveguide.

In transmission side there are three information ports namely D/T where we input of D/T flip flop it is the real port to acknowledge the info bit examples and here Clock is for the positive level activated clock input and the enable is used to switch or change the working either a D Flip flop or T flip flop based on the information provide.

When getting into the output side we have while Q and $\overline{Q}$ are the integral yields as mentioned we have

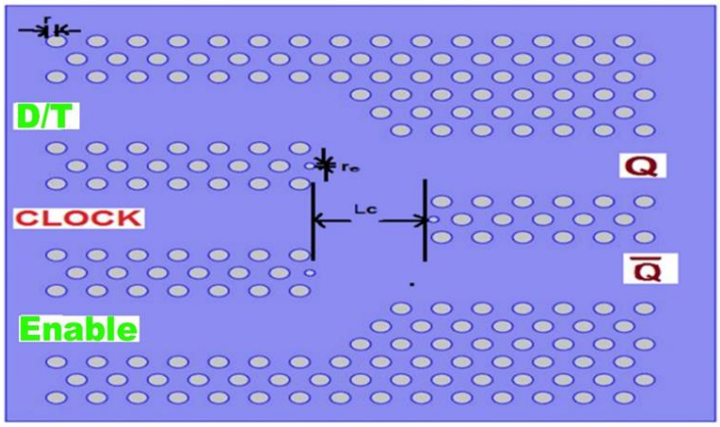
the air hole structures with which are modeled as per requirement and we have supporting materials and back ground material.

The structure of an optically based timed D/T Hybrid -flip flop is based on MMI and is made in photonic crystal. The fundamental structure in an MMI-based plan is a waveguide or MMI area, which can support a large number of modes and is linked with access waveguides at the front end and back end to dispatch and recuperate light from that essential MMI waveguide. [3]

These MMI devices are primarily reliant on self-imaging property, wherein the guided modes are activated in the MMI area and play a beneficial role. These energized fields alternately transmute along the proliferation path in the MMI region. The following equation can be used to determine the shortest coupling length of the MMI area.

$$L_c = \frac{\pi}{\beta_0 - \beta_n}$$

The focal MMI waveguide of the structure is answerable for the interference of the light signals. It has low reaction time in nanoseconds duration (say 10μs). This will initiate sensor cycle.



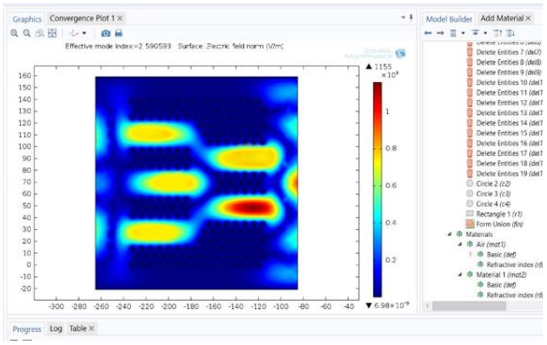
The coupling length Lc can be calculated using one of four potential guided modes: essential mode, first-request mode, second-request mode, and third-request mode. These guided modes are found by first determining the working point (the point on the y-hub in the scattering outline where the dabbed line converges), which is determined by the working frequency. Based on the cross section consistent and working frequency 0 of 1650 nm in the proposed work, the working point a/0 on the scattering graph is 0.367.

At this working point, the comparing parameters associated with the guided modes are obtained from Figures and recorded in Table 1. The coupling length Lc is determined by the essential mode and the second-request mode (even mode), and it ensures that the three information light signals are properly coupled. At this coupling length, the three information light bars propelled perpendicular to each other at all of the MMI waveguide's information ports will superimpose on the yield port of the waveguide that is inverse to the info port being energised with a light sign of zero stage. Along these lines, the MMI waveguide's yield port will receive more power. The MMI waveguide's other yield port will be left with a low or insignificant force.

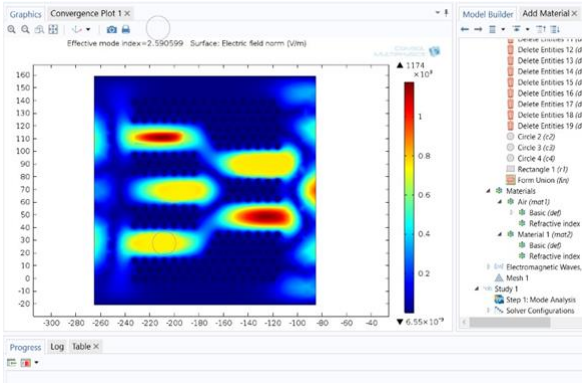
When only one information port is activated, a single image occurs at positive whole number products of beat length (L), which can be approximated to coupling length (Lc) in a photonic crystal-based MMI structure. So, at this coupling length, the yield port of the MMI waveguide will receive a solitary picture with high force while the other yield port will receive a low power. As a result, the coupling length in the proposed structures is kept at 8.2a, which is obtained from the hole between the focal points of both the outrageous edge bars in the MMI waveguide fewer multiple times the range of the edge poles (0.5a). According to the previously mentioned hypothetical viewpoint, the proposed JK-flip flop's Clock contribution is constantly energised with a light emission beginning stage. [4]

RESULTS

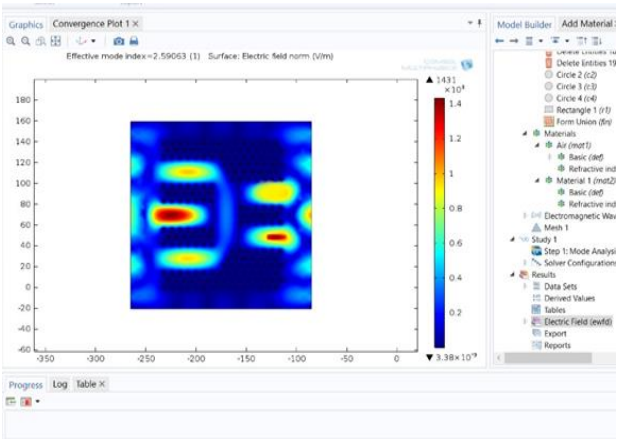
(T FLIPFLOP WHEN EN=0 previous state =0)



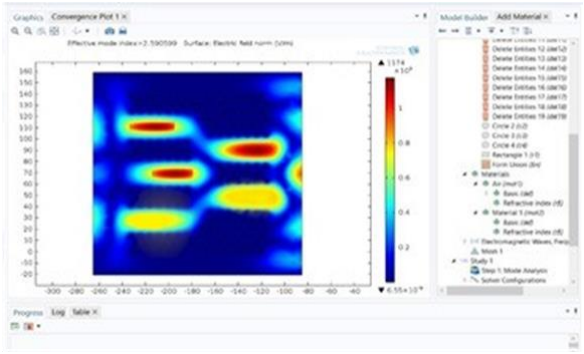
After completion of compute we will get the output like this by giving the input TEST CASE 1 (CLK:0,D/T:0,E:0,Qprev=0), and we get output as (Q=0 Q'=1).



After completion of compute we will get the output like this by giving the input TEST CASE 2 (CLK:0,D/T:1,E:0,Qprev=0), and we get output as (Q=0,Q'=1).

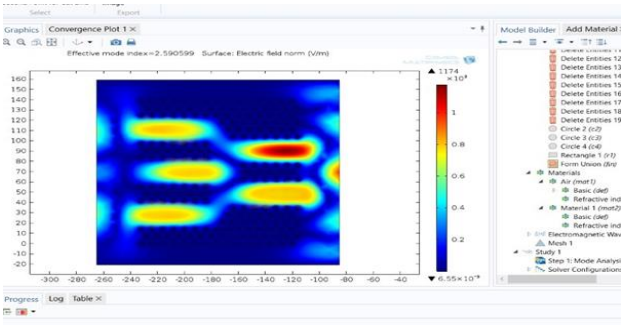


After completion of compute we will get the output like this by giving the input TEST CASE 3 (CLK:1,D/T:0,E:0,Qprev=0), and we get output as (Q=0,Q'=1).

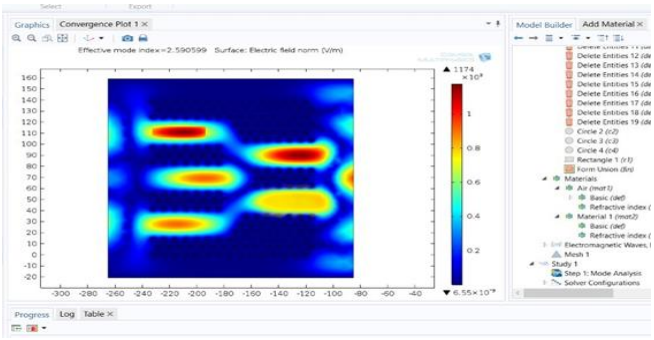


After completion of compute we will get the output like this by giving the input TEST CASE 4 (CLK:1,D/T:1,E:0,Qprev=0), and we get output as(Q=1 Q'=0).

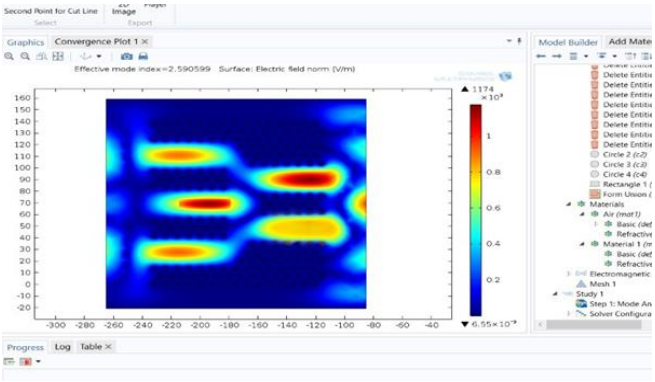
RESULTS
(T FLIPFLOP WHEN EN=0 previous state =1)



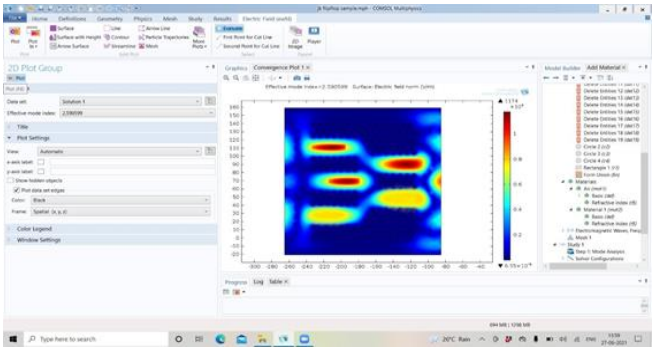
After completion of compute we will get the output like this by giving the input TEST CASE 5 (CLK:0,D/T:0,E:0,Qprev=1), and we get output as(Q=1 Q'=0).



After completion of compute we will get the output like this by giving the input TEST CASE 6 (CLK:0,D/T:1,E:0,Qprev=1), and we get output as(Q=1 Q'=0).

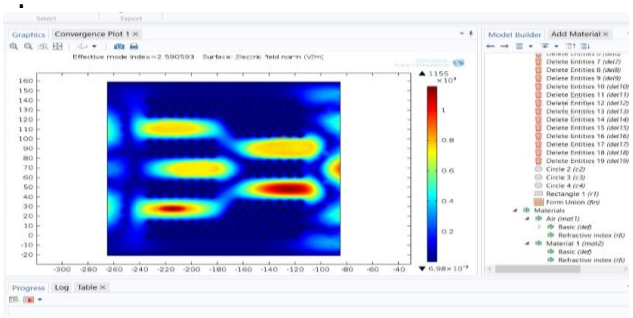


After completion of compute we will get the output like this by giving the input TEST CASE 7 (CLK:1,D/T:0,E:0,Qprev=1), and we get output as(Q=1Q'=0).

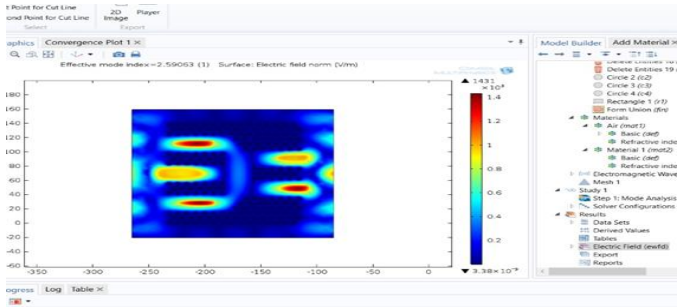


After completion of compute we will get the output like this by giving the input TEST CASE 8 (CLK:1,D/T:1,E:0,Qprev=1), and we get output as(Q=0 Q'=1)

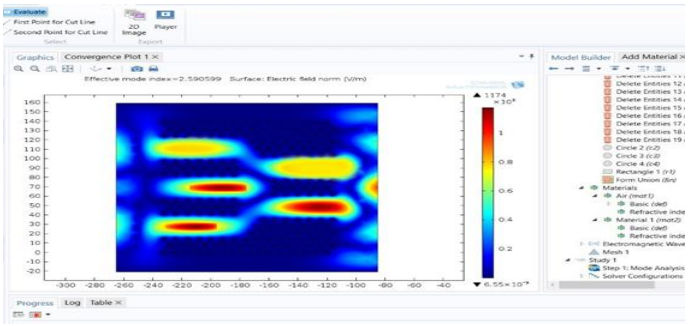
RESULTS
(D FLIPFLOP WHEN EN=1 Previous state =0)



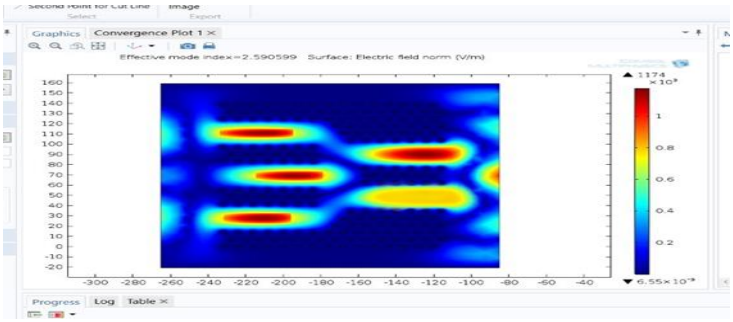
After completion of compute we will get the output like this by giving the input TEST CASE1 (CLK:0,D/T:0,E:1,Qprev=0), and we get output as(Q=0 Q'=1).



After completion of compute we will get the output like this by giving the input TEST CASE 2 (CLK:0,D/T:1,E:1,Qprev=0), and we get output as(Q=0 Q'=1).

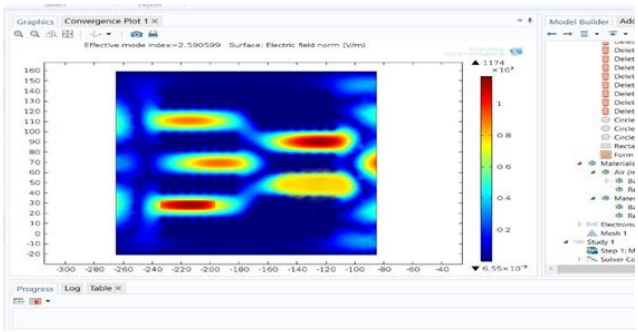


After completion of compute we will get the output like this by giving the input TEST CASE 3 (CLK:1,D/T:0,E:1,Qprev=0), and we get output as(Q=0 Q'=1).

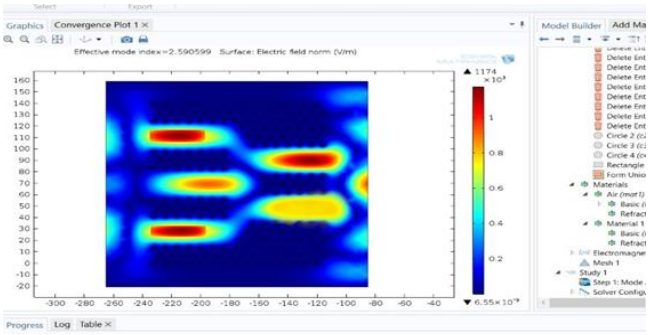


After completion of compute we will get the output like this by giving the input TEST CASE 4 (CLK:1,D/T:1,E:1,Qprev=0), and we get output as(Q=1 Q'=0).

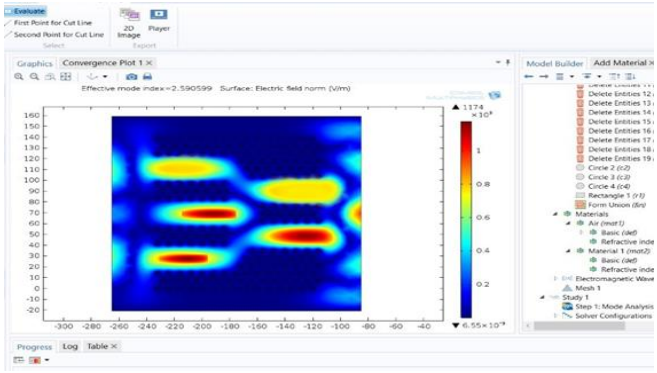
RESULTS
(D FLIPFLOP WHEN EN=1
Previous state =1)



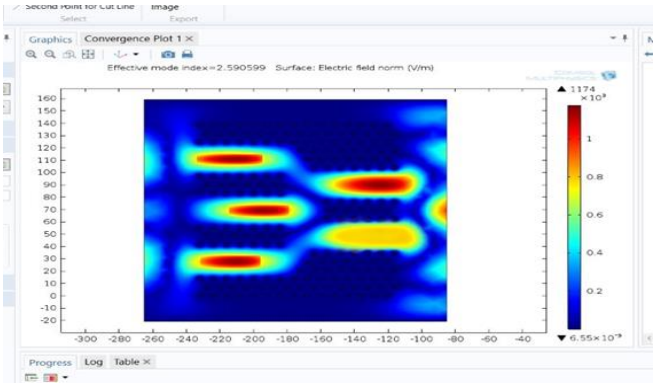
After completion of compute we will get the output like this by giving the input TEST CASE 4 (CLK:0,D/T:0,E:1,Qprev=1), and we get output as(Q=1 Q'=0).



After completion of compute we will get the output like this by giving the input TEST CASE 5 (CLK:0,D/T:1,E:1,Qprev=1), and we get output as(Q=1 Q'=0).



After completion of compute we will get the output like this by giving the input TEST CASE 4 (CLK:1,D/T:0,E:1,Qprev=1), and we get output as(Q=0Q'=1).



After completion of compute we will get the output like this by giving the input TEST CASE 8 (CLK:1,D/T:1,E:1,Qprev=1), and we get output as(Q=1 Q'=0).

Order of the Mode	Propagation Constant (β(2π/a))	Coupling Length Lc (in μm)
Fundamental	0.368	21.2a
First Order	0.326	18.6a
Second Order	0.283	8.2a
Third Order	0.173	2.5a

Table-1: Mode parameters of waveguide at working wavelength

The typical bars as well as the edge bars of the proposed flop structure of the (D/T)-flip are advanced so far that the return transmission (e.g., output power and Pa is the applied information power, for Pout/Pa) may be less than 0.25 or more, to the aim of being considered separately as '0' and rational '1.' [5]

The adjustment of the sweeping bars will modify the output transmission and hence the ON-to-OFF CR of the (D/T)-flip flop proposed. By using the associated conditions, the ON-to-OFF CR of the optical logic device can be establish.

$$CR = 10\log\frac{P_1}{P_0}$$

.

Where P1 is the power level of rationale '1' and P0 is the power level of rationale '0'. A high CR can be acquired by a huge separation in the yield power levels of rationale '1' and rationale '0'. A very low estimation of the force level of rationale '0' contributes more in accomplishing higher CR. The contrast ration details of Clocked (D/T) Flip Flop.

Outputs Of Flipflops At Each Test Case

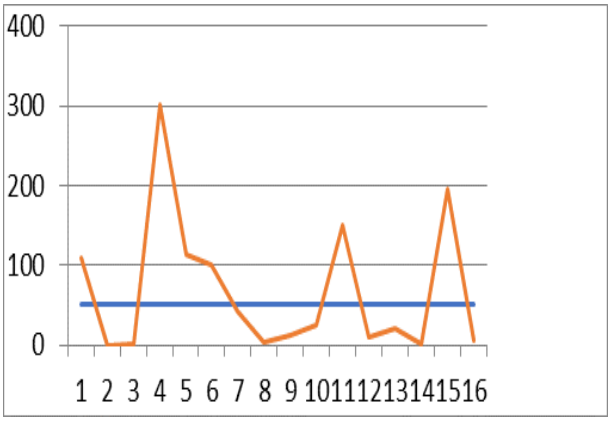


Fig 6: Power of Flip Flop for change in output

We will obtain a threshold value of 50 on the Y-axis while designing this flipflop. Above the value 50, logic `1' is used, and below the value 50, logic `0' is used. The (D/T)-flip flop stores a small amount of binary data; it can be logic 0 or logic 1 and is referred to as a clock pulse, which is typically used to count the information-signal sequence.[6]

The device has an extremely fast counting speed. The (D/T)-flip optical flop causes delay in picoseconds, as opposed to the electronic (D/T)-flip flop, which causes delay in nanoseconds. Optical sign preparation plans are essentially implied for rapid workouts in a wide range of applications, such as media transmission systems and frames, optical processing, and so on.

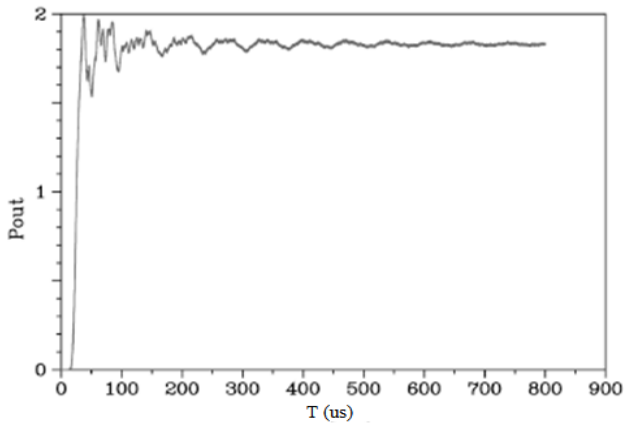


Fig 7: Response time of Flip Flop for change in output

The above figure shows the response time flip flop at each test case. Response time flipflop gives clear information for each and every input or each and every test case. [7]

Truth table for D/T flip-flop works as T flip-flop when En=0

CLK	D/T	EN	Qn (Q PREV=0)	Q'	Output Power at Qn+1
0	0	0	0	1	0.216
0	1	0	0	1	0.215
1	0	0	0	1	0.219
1	1	0	1	0	1.57
0	0	0	1	0	1.571
0	1	0	1	0	1.573
1	0	0	1	0	1.575
1	1	0	0	1	0.219

Truth Table For D/T Flip Flop Working As D Flip Flop When En=1

CLK	D/T	EN	Qn (Q PREV=0 &1)	Q'	Output Power at Qn+1
0	0	1	0	1	0.216
0	1	1	0	1	0.215
1	0	1	0	1	0.219
1	1	1	1	0	1.57
0	0	1	1	0	1.571
0	1	1	1	0	1.573
1	0	1	0	1	1.575
1	1	1	1	0	0.219

Contrast Ratio Truth Table:

Q	Pout	CR		Q'	Pout	CR
0	0.216	8.657		0	0.204	8.568
1	1.571			1	1.498	

Table 2: CR of Clocked (D/T) Flip Flop at both outputs Q and Q'.

The contrast ratio (CR) of a display system is defined as the ratio of the luminance of the system's brightest shade (white) to that of the system's darkest shade (black). A high contrast ratio is an important feature of any display. It is comparable to dynamic range.

Static contrast ratio is the luminosity ratio comparing the brightest and darkest shade the system is capable of producing simultaneously at any instant of time, while dynamic contrast ratio is the luminosity ratio comparing the brightest and darkest shade the system is capable of producing over time (while the picture is moving). Moving from a system that displays a static motionless image to a system that displays a dynamic, changing picture slightly complicates the definition of the contrast ratio, due to the need to take into account the extra temporal dimension to the measuring process.[8]

We have a desired formula to calcualte the contrast ratio value by using outputs of logic '1' and logic '0' for both Q and Q'.

$$\mathbf{CR} = 10\log\frac{P_1}{P_0}$$

While we are observing the contrast ratio table, In pout, for logic '0' we will get the maximum value from truth table and for logic '1', we will get the minimum value from truth table for both Q and Q'.

Advantages

The PhC-based optical logic gate has numerous advantages

- High operating speed
- High data transfer rate.
- Good contrast ratio.
- Small in size
- PhC-based optical gates are suitable for use in integrated optical circuits can be implemented by CMOS technology. [9]

Applications

The proposed optical logic gates using photonic crystals can be used in many applications

- Used in optical communications
- Used in optoelectronic applications
- Used in instrumentation applications
- Used in bio sensor applications
- Counters, Frequency Dividers.
- Shift Registers, Storage Registers.
- Data storage.
- Data transfer.
- Optical logic gates have expected applications such as binary addition, header recognition, parity checking, addressing, demultiplexing, regenerating, encoders and switching with very high speed. [10]

Conclusion

We proposed in this paper a key structure to use the clocked Hybrid D/T-flip flop on a photonic crystal base of a cross-sectional square type. The proposed structure consists of the MMI waveguide as a central section in which the information light impedance occurs, and it is connected to the info and the result by direct waveguides. It is reconstructed using a time-area technique of limited distinction which was implemented individually with a CR of 8.657 and 6.24 dB at Q and Q at the yields below 0.27 ps. In this way, it may be concluded that, as a deferral component in frameworks, the proposed Hybrid D/T-flip flop of an essential structure can be used as soon as possible.

Future Scope

- Autonomous vehicles and factories in common use guided by laser detection and ranging (LiDAR) could become a reality and more efficient with photonics
- Real-time image recognition and AI informed decision making using optically enabled superfast classical and quantum computers could be the near future
- Deep body soft tissue imaging for precise early disease diagnosis is possible with photonics
- De carbonization with low impact photovoltaics, precision control of wind generation and ultra-efficient data storage and processing is possible with photonics in near future
- It could build Ultimately secure quantum communication and storage of the world's data [11].

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