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Research Article

Energy Reduction of D-Flipflop Using 130nm CMOS Technology

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ABSTRACT

At present devices are being used widely. In every device there is use of large number of components. One of the major components in designing a device is a D- flipflop. The features and usage of every component is being increased rapidly. So, here we are going to reduce the size (transistor count), energy (power consumption and power delay) of a D-flipflop.

Keywords: D-flipflop, size, energy, transistor.

1. Introduction

Integrated Circuit is the circuit in which all the Passive and Active components are fabricated onto a single chip. Initially the Integrated Chip could accommodate only a few components. As the days passed, the devices became more complex and required a greater number of circuits which made the devices look bulky. Instead of accommodating more circuits in the system, an Integration technology was developed to increase the number of components that are to be placed on a single chip. This Technology not only helped to reduce the size of the devices but also improved their speed.

Depending upon the number of components (Transistors) to be integrated, they were categorized as SSI, MSI, LSI, VLSI, ULSI & GSI. They all represent the technology that issued that gives the number of transistors in each IC.

Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors or devices into a single chip. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. 2 An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI IC designers add all of these into one chip.

Very large-scale integration (VLSI) is the process of integrating or embedding hundreds of thousands of transistors on a single silicon semiconductor microchip. VLSI technology was conceived in the late 1970s when advanced level computer processor microchips were underdevelopment.

VLSI is a successor to large-scale integration (LSI), medium-scale integration (MSI) and small- scale integration (SSI) technologies. VLSI is one of the most widely used technologies for microchip processors, integrated circuits (IC) and component designing. It was initially designed to support hundreds of thousands of transistor gates on a microchip which, as of 2012, exceeded several billion. All of these transistors are remarkably integrated and embedded within a microchip that has shrunk over time but still has the capacity to hold enormous amounts of transistors. The first 1-megabyte RAM was built on top of VLSI design principles and included more than one million transistors on its microchip dye. VLSI has found several advantages.

- It is easier to make incremental improvements.
- It is easier for the system to explain what it is doing and why.
- It is easier for the human expert to determine what is incorrect or incomplete about the systems knowledge and explain how to fix it.
- It is easier to interactively use a human expert's abilities.

As we have seen that VLSI is a technology by which 10000-1 Million Transistors can be fabricated on a single chip. Now, what is the necessity for fabricating that many of Transistors on a single chip? In olden days during the vacuum tube era, the size of Electronic Devices was huge, required more power, dissipated more amount of heat and were not so reliable. So, there was certainly a need to reduce the size of these devices and their heat dissipation. After the invention of SSD's, the size and the heat produced by devices was undoubtedly reduced drastically, but as the days passed the requirement of additional features in Electronic Devices increased

which again made the devices look bulky and complex. This gave birth to the invention of technology which can fabricate a greater number of components on to a single chip. As the need of additional features in Electronic Devices arisen, the growth of VLSI Technology has improved.

Over the past several years, Silicon CMOS technology has become the dominant fabrication process for relatively high performance and cost-effective VLSI circuits. There evolution nature of this development is understood by the rapid growth in which the number of transistors integrated in circuits on a single chip.

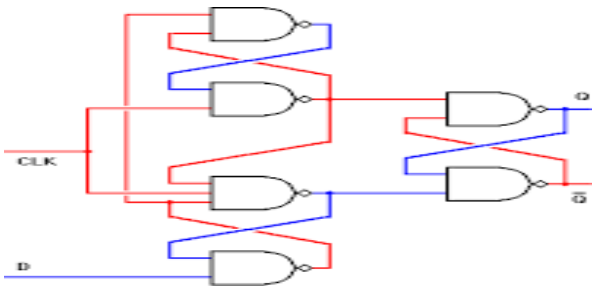
The MOS technology is considered as one of the very important and promising technologies in the VLSI design process. The circuit designs are realized based on pMOS, nMOS, and CMOS and BiCMOS devices. The pMOS devices are based on the p-channel MOS transistors.

Specifically, the pMOS channel is part of a n-type substrate lying between two heavily doped p+ wells beneath the source and drain electrodes. Generally, a pMOS transistor is only constructed in consort with an NMOS transistor. The NMOS technology and design processes provide an excellent background for other technologies. In particular, some familiarity with NMOS allows a relatively easy transition to CMOS technology and design. The techniques employed in NMOS technology for logic design are similar to GaAs technology. Therefore, understanding the basics of NMOS design will help in the layout of GaAs circuits in addition to VLSI technology, the VLSI design processes also provides a new degree of freedom for designers which help for the significant developments. With the rapid advances in technology the size of the ICs is shrinking and the integration density is increasing. VLSI comprises of Front-End Design and Back End design these days. While front end design includes digital design using HDL, design verification through simulation and other verification techniques, the design from gates and design for testability, backend design comprises of CMOS library design and it's characterization. It also covers the physical design and fault simulation.

2. Existing technology

A. CMOS Logic

Flip-flops are the essential structure block of the digital electronics systems utilized within mainframe and most of several kinds of systems. Flip flop are electronic device that provisions position information. The D flip flop output pursue the input which provide the output as input. D signify "DATA" it accumulates the value which is on the data line. Flip-Flop is an electronic circuit which stores the rational condition of individual or extra data input signal are answer to the clock pulse. This D flip flop have set or reset during inverter circuit. There are two kind of flip flop solitary is single edge triggered (SET) and other solitary is double edge triggered (DET). Single edge triggered flip flop is straightforward and simple to propose as works on each increasing or diminishing edge of a clock. The architect of CMOS D flip-flop by 22 transistors is given at this time. The graphic of 5 transistors CMOS D flip-flop. This flip-flop is constructs utilized 22 transistors. This edge triggered flip-flop is diminutive in region because it demonstrates low transistor count merely 22 transistors are utilized and it besides decrease power consumption. In 22T CMOS D Flip Flop, TSPC stands for True Single Phase Clocked logic TSPC circuit method utilized include single phase of the clock and evade skew troubles thus developing the performance of a digital system. These exclusions of skew involve considerable reserves in fragment region and power consumption. Given the graphic of 22T CMOS D Flip Flop. While CLK and input D each are grow then the transistors P1, N3 are OFF and residual transistors P2, N1, N2 are ON. The output turns elevated. Even as in ON clock period suchlike is the worth of input that turn output.



Complementary metal–oxide–semiconductor (CMOS, pronounced "see-moss"), also known as complementary-symmetry metal– oxide–semiconductor (COS-MOS), is a type of metal–oxide– semiconductor field effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions.[1] CMOS technology is used for constructing integrated circuit

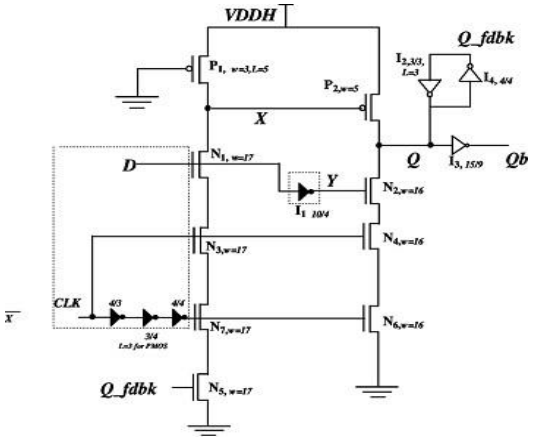
(IC) chips, including microprocessors, microcontrollers, memory chips (including CMOS BIOS), and other digital logic circuits. CMOS technology is also used for analog circuits such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication. Mohamed M. Atalla and Dawon Kahng invented the MOSFET at Bell Labs in 1959, and then demonstrated the PMOS (p-type MOS) and NMOS (n-type MOS) fabrication processes in 1960. These processes were later combined and adapted into the complementary MOS (CMOS) process by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor in 1963. RCA commercialized the technology with the trademark "COS MOS" in the late 1960s, forcing other manufacturers to find another name, leading to "CMOS" becoming the standard name for the technology by the early 1970s. CMOS eventually overtook NMOS as the dominant MOSFET fabrication process for very large-scale integration (VLSI) chips in the 1980s,

while also replacing earlier transistor–transistor logic (TTL) technology. CMOS has since remained the standard fabrication process for MOSFET semiconductor devices in VLSI chips. As of 2011, 99% of IC chips, including most digital, analog and mixed- signal ICs, are fabricated using CMOS technology.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, like NMOS logic or transistor–transistor logic (TTL), which normally have some standing current even when not changing state. These characteristics allow CMOS to integrate a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most widely used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of MOS field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and smaller sizes.

B. Pseudo-nMOS Logic

Using a PMOS transistor simply as a pull-up device for an n-block as shown is called pseudo-NMOS logic. Note, that this type of logic is no longer ratio-less, i.e., the transistor widths must be chosen properly, i.e., The pull-up transistor must be chosen wide enough to conduct a multiple of the n-block's leakage and narrow enough so that the n-block can still pull down the output safely: The advantage of pseudo-NMOS logic are its high speed (especially, in large-fan-in NOR gates) and low transistor count. On the negative side is the static power consumption of the pull-up transistor as well as the reduced output voltage swing and gain, which makes the gate more susceptible to noise. At a second glance, when pseudo-NMOS logic is combined with static CMOS in time critical signal paths only, the overall speed improvement can be substantial at the cost of only a slight increase of static power consumption. Furthermore, when the gate of the pull-up transistor is connected to a appropriate control signal it can be turned off, i.e., pseudo NMOS supports a power-down mode at no extra cost.



The CMOS pull up network is replaced by a single pMOS transistor with its gate grounded. Since the pMOS is not driven by signals, it is always 'on'. The effective gate voltage seen by the pMOS transistor is VDDVDD. Thus, the overvoltage on the p channel gate is always VDD−VTPVDD−VTP. When the nMOS

is turned 'on', a direct path between supply and ground exists and static power will be drawn. However, the dynamic power is reduced due to lower capacitive loading. We design the basic inverter and then scale device sizes based on the logic function being designed. The load device size is calculated from the rise time.

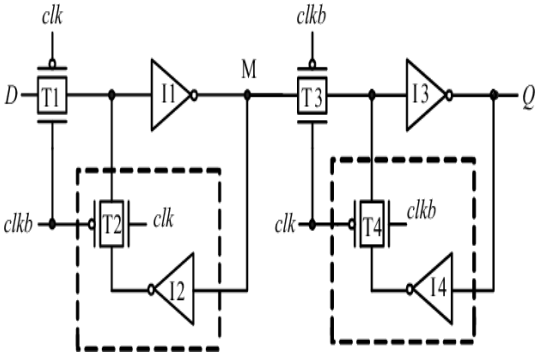
τrise=CKp(VDD−VTP)[2VTpVDD−VTP+lnVDD+VoH−2VTPVD D−VoH]

τrise=CKp(VDD−VTP)[2VTpVDD−VTP+lnVDD+VoH−2VTPVD D−VoH]

Given a value of τrise τrise, operating voltages and technological constant, Kp and hence, the geometry of the p channel transistor can be determined

C. Transmission Gate Logic

A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. Principle diagram of a transmission gate. The control input ST must be able to take to control depending on the supply voltage and switching voltage different logic levels. In principle, a transmission gate is made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p channel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate (inverter), to form the control terminal. Two variants of the "bow tie" symbol commonly used to represent a transmission gate in circuit diagrams Unlike with discrete FETs, the substrate terminal is not connected to the source connection. Instead, the substrate terminals are connected to the respective supply potential in order to ensure that the parasitic substrate diode (between source/drain and substrate) is always reversely biased and so does not affect signal flow. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply potential, and the substrate terminal of the n-channel MOSFET connected to the negative supply potential. Consider a basic transmission gate, having two variables x, y respectively. The nfet is controlled by signal c while pfet is controlled by complement c. The operation of the switch can be understood by analyzing the 2 cases i.e.; i) if c=0 then nfet goes to off, complement c = 1 and pfet also in off state so that transmission gate acts as an open switch. (Both fets are in off state) similarly, ii) if c=1 then both pfet and nfet are onstate. by using single logic two gates are operated. Additionally, we need one not operation for pfet to get complement c value. Resistance 26 characteristic of a transmission gate. VTHN and VTHP denote those positions at which the voltage to be switched has reached a potential, where the threshold voltage of the respective transistor is reached. When the control input is a logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n- channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start conducting at a voltage difference between the gate terminal and one of these conducts. One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the N-channel MOSFET, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the n-channel MOSFET, and this begins to turn off. At the same time, the p- channel MOSFET has a negative gate source voltage (gate-to- drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches. Thereby it is achieved that the transmission gate passes over the entire voltage range. The transition resistance of the transmission gate varies depending upon the voltage to be switched, and corresponds to a superposition of the resistance curves of the two transistor.



3. Proposed technology

CMOS logic (Hybrid Logic) CMOS logic is combination of PMOS and NMOS logic. It works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the CMOS logic is used in low- power VLSI circuits, which implements reversible logic. To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods, yet in all these causes, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of logic circuits, other measures can be introduced for recycling the energy drawn from the figure given below.

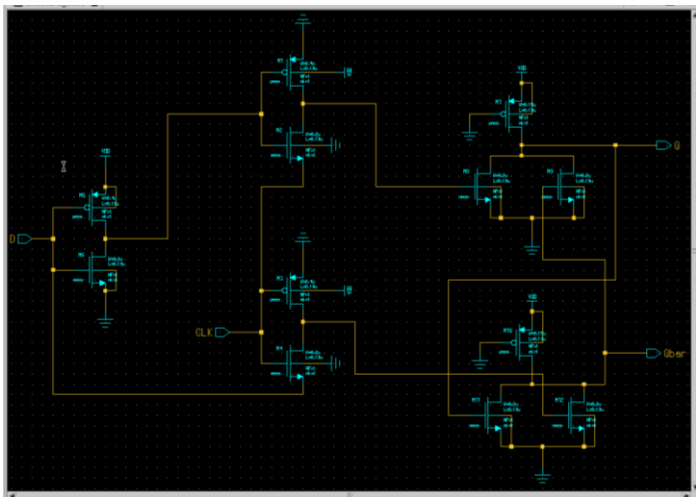


Fig.1 : Proposed flipflop design

This overcomes the problems a raised in existed design that is swaying operation for the inputs A as logic'1' and B as logic'0'. This problem is overcome by using the restitution response loop by the transistors M5 and M10. In the intended design the inputs are given D and CLK as logic '0' then M2 and M3 transistors are in ON state then D Flip Flop gives output Q as logic'0' and Q bar as output logic'1'. But this logic '0' output for Q is in BAD condition. Then the restitution response loop is arranged with the help of M4 and M6 transistors. Then the other Inputs D as logic'0'and CLK as logic'1' then M8 and M9 transistors are in ON condition. Then logic'1' results at Q but this is in swaying situation while the Q results logic'0'. This swaying situation overcomes by restitution loop.

D Flip Flop goes about as the essential square of all adders which are utilized to perform multi bit increases. There are additionally different approaches to plan the D Flip Flop circuit as far as CMOS rationale. With expanding request in speed and power, our principle point is to configuration D Flip Flop circuit so it devours less power and quicker. The vast majority of the power in any circuit is being devoured by the power given to the information way of the circuit which comprises of the transistors. Subsequently by lessening the quantity of transistors we can decrease the power utilization additionally by diminishing the information way, the circuit can be made quicker. The load capacitance is charged by the constant current source while in conventional CMOS constant voltage source is used. Here R is the

resistance PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage is initially zero.

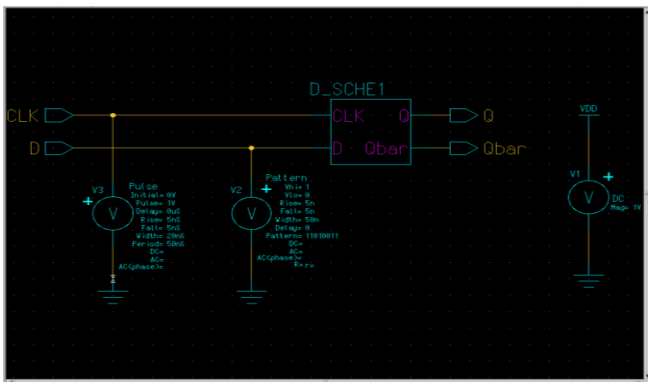


Fig.2 : Simulated schematic of proposed D-flipflop

The schematic diagram for CMOS logic circuit is as shown in the figure. It is having vpc and vpc bar. These two are power supply clocks for tuning the ON &OFF operation of the transistor M3. instead of dc supply we giving sin ac signal. The above figure shows the architecture of proposed system. We proposed new D Flip Flop circuits for different applications which have been appeared in Fig. 4.2. These new D Flip Flops have been utilized switch hybrid logic style, and every one of them is structured by utilizing the proposed CMOS logic style. The notable four- transistor structure is utilized to actualize the proposed cross breed D Flip Flop cells. The D Flip Flop circuit is made with logic style that has no static and short out power dispersal. Hybrid D Flip Flop has not high-power utilization NOT entryways on basic way and comprises of 12 transistors. The benefits of this structure are full-swing yield, low power scattering and extremely rapid, and strength against supply voltage scaling, and transistor estimating. In the event that AB=1, at that point the yield Cout flag equivalents to the info flag. And-or Yet, to level the information sources capacitance, both of the information flags An and B are utilized for execution and are associated with the transistors N9 and P10individually. On the off chance that the info signs are created by the cradle, at that point for all conceivable information mixes, the Q and Qbar yields are not driven by the contributions of the circuit. To do this work, three extra NOT doors are sufficient, in light of the fact that there was at that point the A flag and can be made the cushioned A flag with an additional NOT entryway. So, the capacitance of Q and Q bar hubs wind up littler, and the postponement of the circuit will be made strides. With the progression of innovation and diminished transistor sizes, the conduct and execution of a circuit couldn't be examined without transistor estimating, since a little change in the extent of transistors may significantly change the execution of the circuit. Accordingly, picking the proper strategy for transistor measuring, before acquiring the vital parameters of the circuit, is essential. Instead of DC signal we giving the sin AC signal, this is use to remove unwanted signals that is also useful for reduction power consumption of entire circuit. The figure 4.2 shows VPC and VPC bar these two are useful for power supply clocks, and also useful to ON&OFF the transistor. If we are varying the frequency due to that variation in the VPC and VPC bar. VPC is clockwise direction and VPC bar is anticlockwise direction. In phase clocks amplitude and phase angle, frequency are the parameters if we are varying these parameters due to the corresponding results appear like in the form of Q bar, sum. But the main drawback of the result is voltage degradation drop. But in logic gates above 0 is treated as 1.And above 1 is treated as 0.The main advantage of the using CMOS inverter is reduction of power consumption and delay of existing system

D Flip- flop	Trans-sitar count	Propagation delay (nsec)	Power dissipation(μW)	Power delay product (fJ)
CMOS Logic	22	0.79	0.43	0.339
Pseudo- nMOS logic	20	0.72	0.38	0.273
Transmission gate Logic	18	0.65	0.34	0.221
Hybrid Logic	12	0.61	0.30	0.183

Fig.3 : Comparison of D-flipflop

Waveforms

Fig.4 : Output waveform of existing D-flipflop

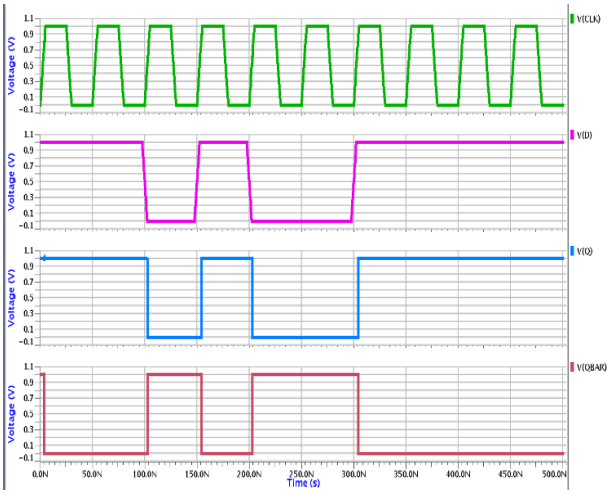


Fig.5 : Output waveform of proposed D-flipflop

References

1. https://ieeexplore.ieee.org/document/8711610
2. N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley,2010.
3. H. Patrovi, R. Byrd, U. Salim, F. Weber, L. Di Gregorio, and D. Draper. Flow-through latch and edge- triggered flip-flop hybrid elements. In Proc. IEEE ISSCC Dig. Tech. Papers. 1996; p. 138–139.
4. F. Klass. Semi dynamic and dynamic flip-flops with embedded logic. In Proc. Symp. VLSI Circuits Dig. Tech. Papers, Honolulu, HI. 1998; p. 108–109.
5. C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Nowaki. Conditional data mapping flip-flops for low-power and high-performance systems. InIEEE Trans. Very Large Scale Integration. (VLSI) Syst. 2006; vol. 14; p.

1379–1383.
6. N. Nedovic, M. Aleksic, and V. G. Oklobdzija. Conditional pre-charge techniques for power efficient dual-edge clocking. In Proceedings. International Symp. Low-Power Electron Design. 2002; p. 56–59.
7. P. Zhao, T. K. Darwish, and M. A. Bayoumi. High performance and low-power conditional discharge flip- flop. InIEEE Trans. Very Large Scale Integration (VLSI) Syst.2004; vol. 12; no.5; p. 477–484.
8. A. Hirata, K. Nakanishi, M. Nozoe, and A. Miyoshi. The cross charge control flip-flop: A low-power and high-speed flip-flop suitable for mobile application SoCs. In Proc. Symp. VLSI Circuits Dig. Tech. Papers. 2005; p. 306–307.
9. KalarikkalAbsel,Lijo Manuel, R.K. Kavitha. Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic. InIEEE Transactions. VLSI Syst. 2013; vol.21; no.9; p.1693-1704
10. Sudheer A, AjithRavindran. Comparative Analysis of Flip-Flops for High-Performance Systems in 0.18µm Technology. In Proc. National Conf. on Recent Trends in Electronics World. Papers. 2014; p. 167-171
11. O. Sarbishei and M. Meymandi-Nejad. A novel overlap-based logic cell: An efficient implementation of flip–flops with embedded logic. InIEEE Trans. Very Large Scale Integration. (VLSI) Syst. 2010; vol. 18; no. 2; p. 222–231.
12. H. Mahmoudi, V. Tirumalasetty, M. Cooke, and K Roy. Ultra low power clocking scheme using energy recovery and clock gating. In IEEE Trans. Very Large Scale Integration. (VLSI) Syst. 2009; vol. 17; no. 1; p. 33–44.