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Research Article

Design A Low Power and High Throughput 130nm Full Adder Utilising Exclusive-OR And Exclusive- NOR Gates

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ABSTRACT

This literature illustrates the high speed and low power Full Adder (FADD) designs. This study relates to the composited structure of FADD design composed in one unit. In this the EXCL-OR/EXCL-NOR designs are used to design the FADD. Mostly concentrates on high speed standard FADD structure by combining the EXCL-OR/EXCL-NOR design in single unit. We implemented two composite structures of FADD through the full swing EXCL-OR/EXCL-NOR designs. And the EXCL-OR/EXCL-NOR design is done through pass transistor logic (PTL) and the same design projected on the composited FADD design. Such that the delay, area of the design, power requirement for the circuit gets optimized. The two composited FADD designs are compared and reduced the constraints of power requirement, area, delay and the power delay product (PDP). The simulated outcomes are verified through 130nnm CMOS mentor graphics tool.

Keywords: Full Adder (FADD), EXCL-OR/EXCL-NOR, Pass transistor logic (PTL), mentor graphics tool.

Introduction

An EXCL-OR – EXCL-NOR gates are designed to create single bit Full Adder(FADD)s of 6 in count with 90-nm CMOS, were developed and the throughput was observed using HSPICE, Cadence tools and found that everything like the power delay product (PDP), energy usage and Fastness were better concert on all aspects. While the size and delay is reduced. The other advantage here is that this mechanism is tolerable to heavy blares. And an invention of single bit FADD is done and it is expanded to 32 bit as well. The design brought development regarding energy and fastness. To design FADD they used pass transistors [PTs], Transmission gates [TGs] and Conventional CMOS is invented and its results were calculated using cadence toolset, also contrasted with 20 FADD past designs and found that it provided fastness among them. So that a hybrid full adder (FADD) design at fundamental level is described and predicted the concert in multistage designs which gave good results in power utilization and tradeoff. A reverse-carry-propagate adder [RCPA] is developed along with few hybrid adders and contrasted with state-of-art summers in HSPICE tool which resulted in low delay and power consumption. To optimize the power they revoked the adder so that the power usage along with output noise with a 20 KHz signal band width and 103.4 μW power loss. An innovative approach is made to get fixed-width adder-tree [AT] pattern with truncated put in with best putout. The other positivity in this is to reduce other obstacles that are available at compound pattern is described from [1]-[9].

An imply based multiplier, IMPLY philosophy with memristors and grapheme barristors are used to design FADD which gave five times extra results by using same weight to figure of process and also gives less PDP, 41% speed and 78% low size when compared to the earlier technologies. In the same, a quantum –dot- cellular automata (QCA) and QCA with Exclusive-Or are proposed which is mainly made of totally used majority gates and with less amount of semi used majority gates, the output is very much enhanced in delay, area and cell count as compared to the previous one. The energy consumption here plays an important role and can easily be achieved. The plasmons were used to design an FADD which is made of SiO_2 film laid on CMOS .The exhibited few input wave as compared with near-field design gave

the same output. Mainly, by taking into account of energy usage and speed in designing carbon nanotube field effect transistor (CNFET), 2 resourceful FADD were used with simple exact algorithm [SEA]. The proposed one gave best PDP and less delay as compared to previous ones. And a fault lenient parallel adder is designed using carry pick add algorithm that can minimize area.

To variant a correct multi-threshold voltage (MTV) along with gate diffusion input (GDI) FADD is demonstrated which provided less size and power leakage compared to the previous works when tested with quality based 45nm CMOS mechanism. In these all literatures [10]-[22] they described different technologies to develop the FADD with less delay, power and area. This is a molecular FADD consisting of molecular fundamental gate along with AND and EX-OR gates is designed under a variant technology with strand- displacement [SD] and visual DNASD [DSD] and then executed using visual DSD and evolved that it is used to develop any kind of DNA integrated circuits [23].

Analysis Of Full Adder (Fadd) Logic Structures

There are various logic structures to design the FADD cells. In exact there are two different structures in FADD those are invariant and variant. Invariant FADDs are stable, flexible and consume less power over the variant. Variant structure is the other option to lay the logic function. But in this the size of the structure is less, voltage level in full swing, fast switching, no invariant consumption of power and non ratioed syllogistics. For example if there are M feed in logic then this have M+2 transistors and 2M transistors in CMOS design. The real usage of this is that the PMOS is the only one transistor in CMOS design. Such that the capacitive load at resultant gets optimized which results with lag at output. In this the main constraints are discussed for FADD design is power dissipation, size, delay, reliability and stability. So to overcome the drawbacks we had composited some structures which are known as Composited Variant – Invariant FADDs. Mainly the FADDs are varied in two types based on output occurred. The first type is full swing contains C-CMOS, CPL, PTL, TGA, TFA, Hybrid, 14T and 16T. The second type is non-full swing consists of 10T, 9T and 8 T. Actually these FADDs are designed containing lesser number of transistors related to Excl-OR/Excl-NOR , low power consumption among the second type. So in this some CMOS based transistor FADD design had done due to the complementary CMOS and Pass transistor logic (PTL) acts very tough even in hard situations and the area consumption of transistor can be modified such that these consumes less amount of power which is the usage of this circuit design.

Design Of Optimized Excl-Or/Excl- Nor Using Transistors

In this paper to design the full adder that is composite full adder we used 2 by 1 multiplexer and 2 input Excl- OR/Excl- NOR circuit. The Excl-OR/Excl-NOR requires high power to run. So this is the main circuit which consumes high amount of power in FADD. So the main focus of this paper is to design the Excl-OR/Excl-NOR with a minimum number of transistors. Such that we used the full swing circuits laid by the Double pass-transistor (DPL) structure and Pass transistor logic (PTL) structure. The implemented DPL is shown in Fig.1 contains eight transistors the drawback of this is it**,** this contains two inverters which drives resultant capacitance which requires more power, more area leads to delay, in addition medium points more capacitance such that the factor power delay product (PDP) is also high. Another logical circuit design Excl-OR/Excl-NOR is the Pass Transistor Logic (PTL) structure shown in Fig.2Contains six transistors, which requires less power, delay, area and such that PDP compared over the DPL structure. This is the best circuit which has one pass transistor gives results with less number of transistors.

Implemented Excl-OR/Excl-NOR Design

So in this by using PTL design we implemented Excl-OR/Excl-NOR circuit and compared this implemented over the non-full swing circuit because for this the Power and lag at the output are very effective. Due to the voltage decrement drawback for single feed in logical data we implemented the full swing structure. In this projected Excl- OR/Excl-NOR structure there are not gates such that there is less lag/delay and good ability to drive the circuit over the Fig.1 and Fig.2. In this Fig.1 have one transistor more than the Fig.2. The design visualized in Fig.1 feed in A and B are not same, due to these are attached to feed in of inverter and other to the nmos, such that delay and power consumption is optimized.

Composited Excl-OR/Excl-NOR Design

So by considering, the Fig.1 we composited those Excl- OR/Excl-NOR circuits and designed the Fig.2. This Fig.2 contains 12 transistors. In this design the feed in are connected as shown in Fig.1. In this we can see the reduced delay and power. The circuit does not contain inverter on its path and resultant capacitance is also negligible. Such that this circuit obtains fast output and low power consumption. While the set back of Excl-OR/Excl-NOR is equal, this minimizes the hitch in another step. Another uses of this circuit are high driving ability, resultant with full swing, tough and reliable, less area and less supply voltage. From this conceptual we can say that the

lag at the output, power consumption is less than then PDP is less. Overall the performance of Fig.2 is better compared over other structures.

Implemented Composited Full Adder (Fadd) Design

We implemented two novel FADD circuits for several appliances shown in Fig.6 and Fig.7. The designed novel FADD have been achieved through composited logic structures, and also these all are implementing utilizing the circuit Fig.5. Fig.6 visualizes the new implemented composited FADD design with 20 transistors, designed with the help of two 2 by 1 multiplexer and Excl- OR/Excl-NOR gates (shown in Fig.5). So the design CFA (Composited Full Adder) have 20 transistors, in this the power consumption is less due to the usage of inverter. The uses of this design are full swing output, less power dissipation and fast switching speed, toughness over the voltage and area. For example if a Excl-NOR b is equal to one then carryout equal to feed in a and b. to unite the feed in Capacitances, a and b are to be utilized for achievement and attached to the N9 and P10 transistors correspondingly. Drawback of this is minimization occurred in resultant driving ability due to chain system like carry adders. Such that we proposed TG logic to avoid the hedging at the resultant. In the design of Fig.2 we utilized minimum number of transistors. So to generate the resultants like sum, Excl-OR/Excl-NOR and the sum resultant will not depends on Excl-OR and Excl-NOR feed in. But these are attached to transmission gate multiplex and then to selection lines of 2 by 1 multiplexer. In this the lag can be optimized only when the Excl-OR/Excl-NOR nodes converts petite. The design Composited FADD (CFA-22T) Fig.4 is generated by enforcing the design of Fig.1 which contains 22 transistors so that the implemented design in which have less power consumption and delay when correlated with CFA-20T, because of minimum capacitance at Excl-OR/Excl-NOR bumps. By summing the cbar, the driving ability of CFA-22T is good over the CFA-20T design.

Simulation Results

In this simulated waveforms we had done on FADD implementation through Excl-OR/Excl-NOR, so that we mainly concentrated to reduce the transistors in Excl- OR/Excl-NOR and also the factors like Power dissipation, Delay and PDP. So in this the Excl-OR/Excl-NOR is implemented through DPL, PTL and Non full swing. In this the simulation results shows that the PTL is suitable to design the FADD. So, we used the PTL style and designed the full adder with 22trqansistors and 20 transistors. In FADD-22T have more power dissipation compared to FADD-20T, while the delay is lesser than the FADD-20T. So at last we concluded that PDP value for FADD-22T is less when compared to FADD-20T. The resultants and their factors are explained in Table1.And the implemented designs Schematics, Symbols, Simulated waveforms are shown below.

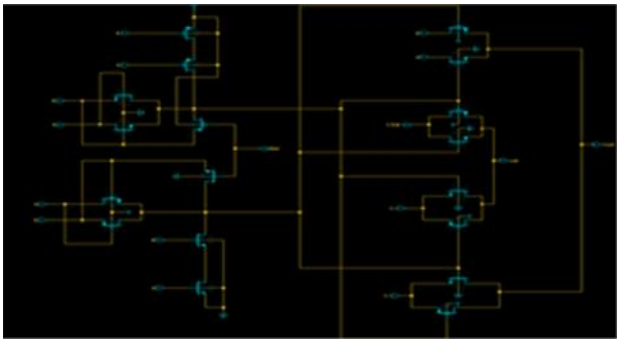

Fig.1: Composited Full Swing schematic of Excl- OR/Excl-NOR with 10T

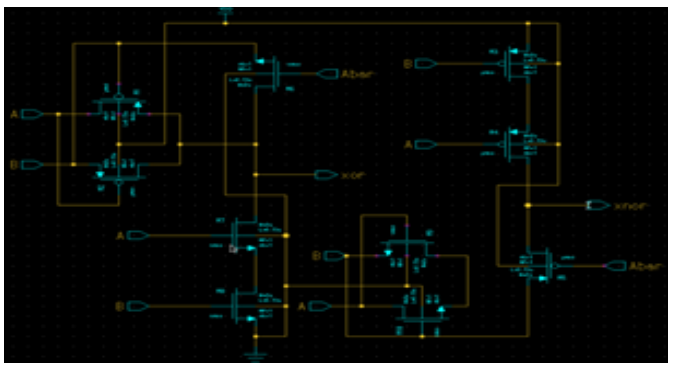

Fig.2: Implemented Full Swing Schematic of Excl- OR/Excl-NOR with 10T

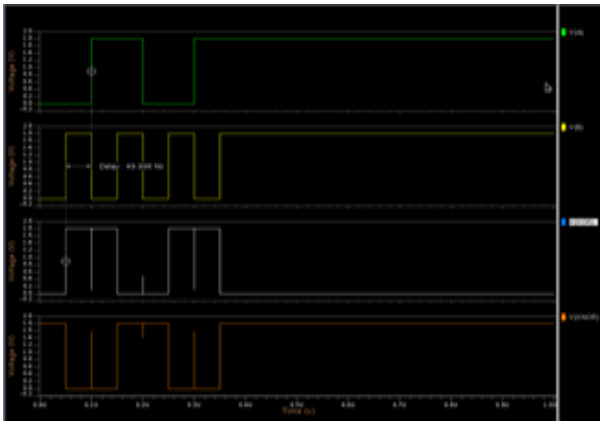

Fig.3: Composited Full Swing simulated Waveform of Excl-OR/Excl-NOR with 10T

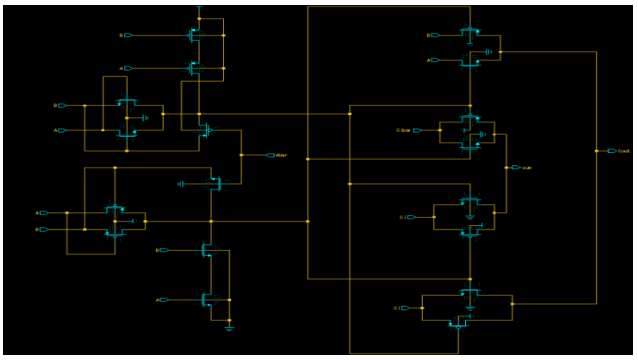

Fig.4: Projected schematic of FADD using PTL logic with 22T

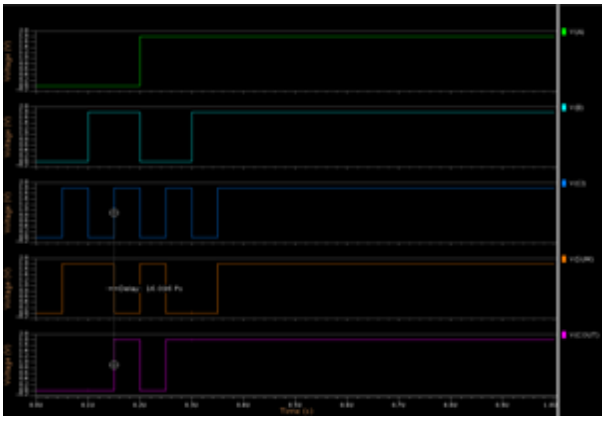

Fig.5: Projected simulated waveform of FADD using PTL logic with 22T

Table 1: Simulation outcomes of Excl-OR/Excl-NOR and Full Adder designs

Design	Technology used	Power Dissipation (nw)	Delay (ns)	Power Delay Product (PDP)femtojoules (fJ) 10^-18 Joules
Full swing PTL Excl- OR/Excl-NOR	130nm	0.827	49.79	0.041
Full swing PTL combined Excl-OR/Excl- NOR	130nm	0.827	49.79	0.041
FA-22T using PTL logic	130nm	8.926	0.016	0.143

Conclusion

In this literature, we first implemented the Excl-OR/Excl- NOR designs. So from the analysis due to inverters in the design, and due to closed loop of Excl-OR/Excl-NOR it is becoming disadvantage. So because of closed loop, the factors like the delay, resultant capacitance, and power consumption of the design getting maximized. Such that we implemented another Excl-OR/Excl-NOR design to overcome those constraints. So, at end the implemented Excl-OR/Excl-NOR have designed two composited FADD structures with several appliances. And to minimize the size of transistor we used the novel technology such that the design achieves better agility, efficiency and concurrence. So after the simulation of composited FADD structure this gives better achievements. And the implemented CFA-22T shows that PDP upto among the implementations. And these designs have delay of 0.016ns and power consumption of 8.926nw is better over another FADD structures. The implemented CFA-22T acts with less delay and power consumption over other at every point of situations. So all FADD structures are sensitive to PVT changes.

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