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An Innovative Design of Decoder Circuit using Reversible Logic

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Abstract

Reversible logic has been widely used in the field of VLSI. In this paper, we introduce a method that enables the designers to implement this technique in their decoder circuits. In Logical Reversibility is not allowed for Fan-out and Feed-back. It is primarily used for applications in various sectors such as Computer Graphics, High Performance Computing, and Nanoscale. This paper presents a reversible logic circuit with respect to its energy consumption. It is mainly useful for minimizing the need for power supply. The comparison study on garbage output and quantum cost of gates is presented.

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Introduction

Power consumption has become an important factor when designing combinational circuits. By using a Reversible Decoder, designers can reduce the overall power consumption while maintaining the same performance. Reversible logic has gained popularity due to their ability to minimize the power dissipation. Due to the rapid decrease in size of the chips, the transistor count has increased. This has caused the energy dissipation to become a major barrier to the evolution of nano-computing. The concept of reversible logic states that an operation can be reversed if it does not involve the energy-conversion or the change in entropy. The computational device's state is only revealed once it has been used. No other information about it can be lost.

In computing, reliability refers to the ability to retain all of the information about a computational state. This means that no data can be lost. logical reversibility is a type of reversibility that can be utilized after the physical reversibility. Physical reversibility is the process of keeping energy and heat in balance. When a voltage level changes from positive to negative, computing systems stop giving off heat. This is because the energy needed to make the change is usually dissipated. Instead of changing the voltage, the circuit elements will gradually transform charge from one region to the next. Due to the nature of digital logic designs, it is very important that the outputs are always connected to the correct state of inputs in order to perform their intended function. This technology will affect various aspects of programming. It will also have to be used to provide optimal efficiency. Some limitations are also considered when designing circuits with reversible logic. These limitations include notallowing Fan out design and Feedback design. With outputs, we can obtain complete knowledge of our inputs. However, with the use of outputs, we can also conserve information. Some of the cost metrics that are used to evaluate the performance of reversible circuits are:Garbage outputs, number of gates, constantinputs, etc. They are kept alone and without performing anyoperations. The number of gates required to implement a gate is called quantum cost. It is simply the number of gates that are needed to complete a circuit. Quantum Cost is the number of elementary orprimitive gates needed to implement the gate. It is nothingbut the number of reversible gates (1x1 or 2x2 or 3x3 or 4x4 etc) required toconstruct the circuit. A delayed circuit design is a cost-effective method for measuring delays. It can be modeled as a series of discrete time slices and is commonly used for estimating depth and duration. The binary decoder is a type of logic circuit that is commonly used in digital electronics to convert the binary value to the output pattern. The binary decoder is a combinational logic circuit that outputs a binary value. It is commonly used in digital electronics.

In this paper, the design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost. All the corresponding results have been shown further.

Reversible Logic Gates

A reversible logic gate is a device that has one-to-one mapping. It outputs both the n-input and the output. Direct fan-out is not allowed in reversible circuits. Instead, fans are achieved through additional gates. A reversible circuit should have at least four logic gates. Generally, it should be designed to have a low complexity level. A reversible circuit design takes into account many factors such as complexity, performance, and number of gates used in it.

- The number of constant inputs (CI): The number of constant inputs is a function that indicates the number of inputs that are constant.

The number of garbage outputs (GO): The number of garbage outputs (GO) in a reversible logiccircuit is very important to achievereversibility.

- Quantum cost (QC):The quantum cost is the cost of a primitive gate that's required to realize a circuit. It shows the number of gates that are needed to get the circuit started.

Basic reversible logicgate

FeynmanGate

Feynman gate is a 2×2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

Double Feynman Gate(F2G)

Figure 2 shows a 3×3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P,Q,R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

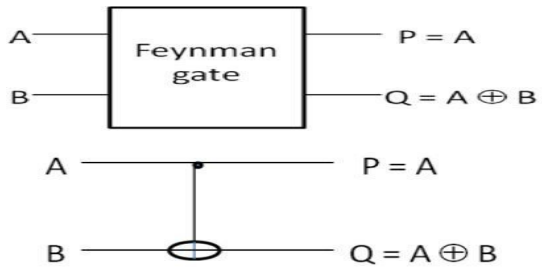

Fig. 1: Feynman gate

Table1: Truth table of Feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

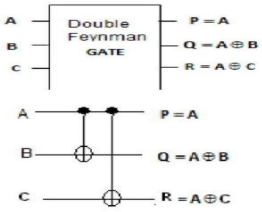

Fig. 2: Feynman double gate (F2G)

Table2: Truth table for F2G

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

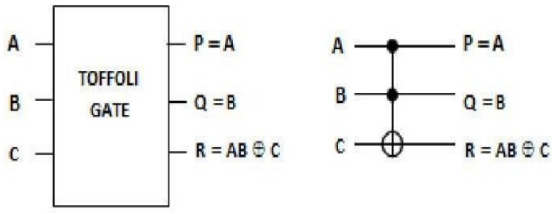

Fig. 3: Toffoli gate

Table 3: Truth table for Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

ToffoliGate

Figure 3 shows a 3×3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB ⊡ C. Quantum cost of a Toffoli gate is5.

FredkinGate

Figure 4 shows a 3×3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output isdefined by P=A, Q=A′B ⊡ ACand R=A′C ⊡ AB. Quantum cost of a Fredkin gate is 5.

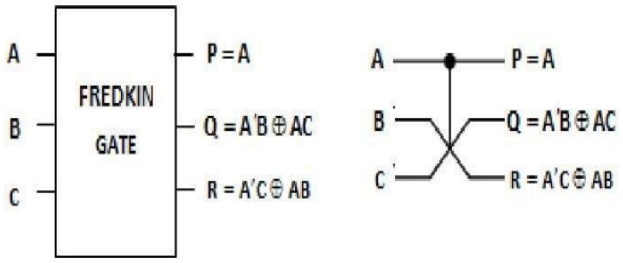

Figure 4: Fredkin gate (FRG)

Table4: Truth table for FRG

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Decoder

A binary decoder is a type of logic circuit that processes binary information. It works by converting the input data to a unique output. Data multiplexers are commonly used in a wide range of applications. They can be used in a variety of configurations, such as data demultiplexing, data conversion, and memory and port-mapped I/O. A binary decoder is an electronic device that uses multiple input and output signals to convert a given set of binary values. There are many types of binary decoders, each of which has its own unique characteristics. In most cases, a decoder is an electronic circuit that outputs a variety of signals simultaneously. In addition to having the usual data inputs, some decoders have “enable” inputs. When these are negated, all outputs are forced to be inactive. A binary decoder is capable of converting binary information from an n input signal to 2n unique output signals. A binary decoder is a device that can convert binary information from an n input signal to 2n unique output signals. It can also output different binary values depending on the decoder’s function. A binary decoder is typically implemented as a stand-alone integrated circuit or a more complex multi-purpose IC. It can be written in either a hardware description language or a binary format. Standardized ICs are often used for decoders. These are typically used for low-voltage input signals.

Basic Decoder 2x4

Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The **block diagram** of 2 to 4 decoder is shown in the following figure 5.

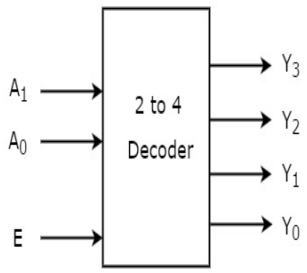

Fig. 5: Block diagram for Decoder 2 to 4

Table 5: Truth Table for Decoder 2 to 4

Enable	Inputs		Outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

One of these four outputs will be ‘1’ for each combination of inputs when enable, E is ‘1’. The **Truth table** of 2 to 4 decoder is shown in table 5.

From Truth table, we can write the **Boolean functions** for each output as

$$Y_3 = E.A_1.A_0$$
$$Y_2 = E.A_1.A_0'$$
$$Y_1 = E.A_1'.A_0$$
$$Y_0 = E.A_1'.A_0'$$

Each output is having one product term. So, there are four product terms in total. We can implement these four product terms by using four AND gates having three inputs each & two inverters. The **circuit diagram** of 2 to 4 decoder is shown in the figure 6.

Therefore, the outputs of 2 to 4 decoder are nothing but the **min terms** of two input variables A_1 & A_0, when enable, E is equal to one. If enable, E is zero, then all the outputs of decoder will be equal to zero.Similarly, 3 to 8 decoder produces eight min terms of three input variables A_2, A_1 & A_0 and 4 to 16 decoder produces sixteen min terms of four input variables A_3, A_2, A_1 & A_0.

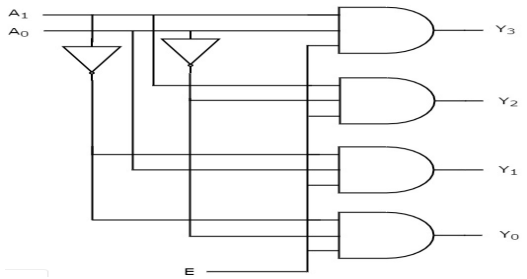

Fig.6: Logic Diagram for decoder 2 to 4

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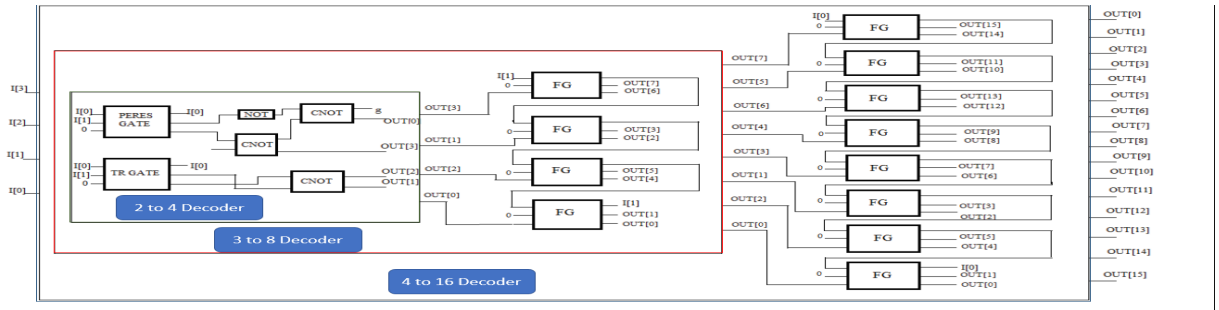

Fig. 7: Proposed Circuit diagram for 4x16 decoder using lower order decoders

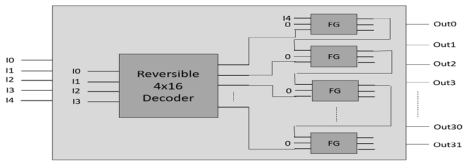

Fig. 8: Reversible 5 x 32 decoder

The higher order decoders can be designed using the available lower order decoders. The higher decoders for example are 3x8 decoder, 4x16 decoder and 5x32 decoder. We can find the number of lower order decoders required for implementing higher order decoder using the following formula.

$$Required\ number\ of\ lower\ order\ decoders = \frac{m_2}{m_1}$$

Where,m1is the number of outputs of lower order decoder. m2 is the number of outputs of higher order decoder.

Therefore, we require two 2x4 decoders for the design of one 3x8 decoder, two 3 to 8 decoders for implementing one 4 to 16 decoder and two 4x16 decoders for the implementation of one 5x32 decoder.

Reversible Decoder

There are various proposals being presented for the design of combinational and sequential circuits, such as adders, subtractors etc. In this paper, the author has presented a novel 4x16 decoder design which uses quantum cost less than the previous design. For designing 2x4 decoder gates, the old fredkin gates are replaced with newer ones like peres gate, TRgate, NOT gate and CNOT gate. The whole design is done using CNOT, Peres, and Fredkin gates.

The Quantum Cost is better than the other reversible Logic gates. The number of gates needed to design 4x16 decoder is 18. These gates are divided by the total quantum costs of each gate. Different types of reversible decoder circuits are commonly used for different applications. Some of these circuits are composed of gate, adder, and multiplexers. This concept is proposed to enable the simultaneous output of a single output to the required number of outputs. It can be done by using the Feynman gate. In cases where Fan-out is not allowed, the concept of parallelizing a single output to a number of outputs is introduced. It can be done by implementing the 4x16 reversible decoder.

Simulation Results

The simulation results for various ordered decoders were presented below. They were derived using the ISE Design suite of Xilinx.

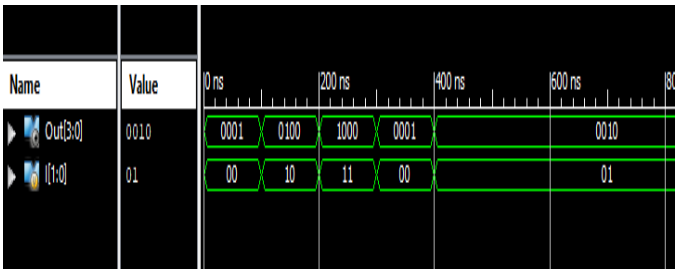

Figure 9: Simulation Results for 2to4 Decoder

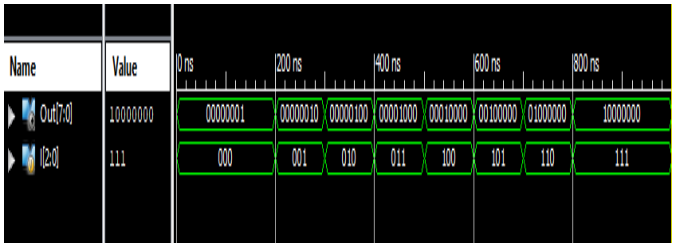

Fig. 10: Simulation Results for 3to8 Decoder

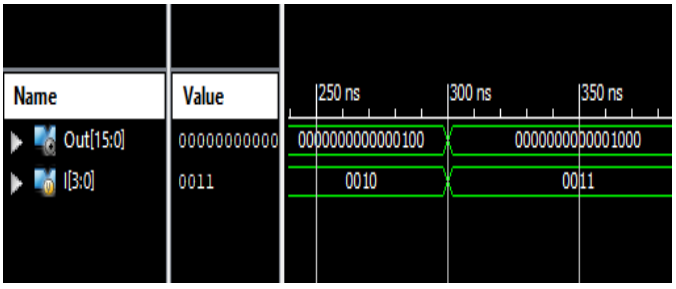

Fig. 11: Simulation Results for 4to16 Decoder

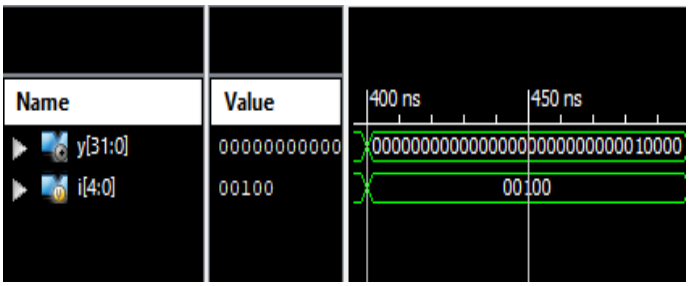

Fig. 12: Simulation Results for 5to32 Decoder

Combinational circuits using Decoder

A decoder takes n input lines and output lines. These lines can provide the sum of minterms for the given input variable. A decoder can generate the binary digits that form the logical sums of a given function. It can also be used to form a circuit with the same logic. A decoder that can generate both the logical terms and the non-zero minterms can be used to create a circuit with any boolean function. Simulation results for various types of adder/ Subtractors, Full adder, Full Adder/Subtractor, 2-bit binary comparator, Multiplexers of size 8x1, 16x1 and 32x1 using decoders are shown in the figure below.

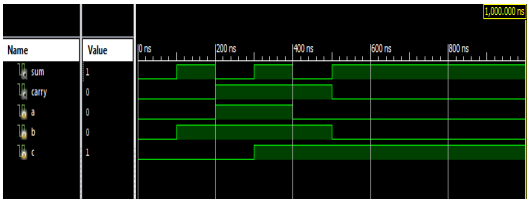

Fig. 13: Simulation Results for Decoder based full adder

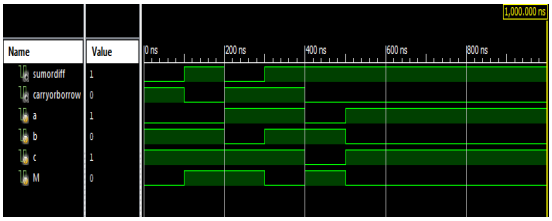

Fig. 14: Simulation Results for Decoder based full adder/subtractor

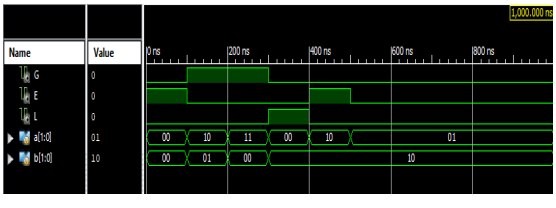

Fig. 15: Simulation Results for 2-bit binary comparator

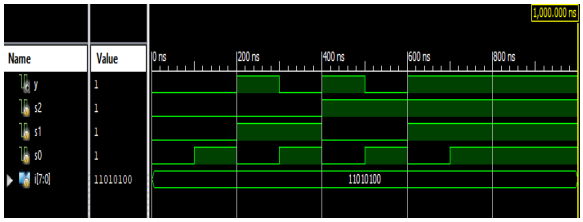

Fig. 16: Simulation results for 8x1 MUX using decoder

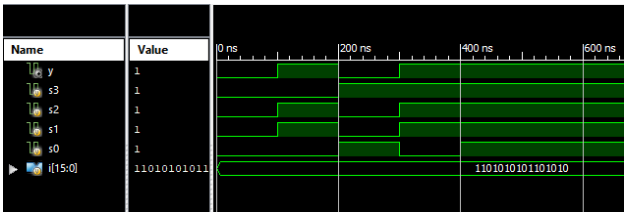

Fig. 17: Simulation results for 16x1 MUX using decoder

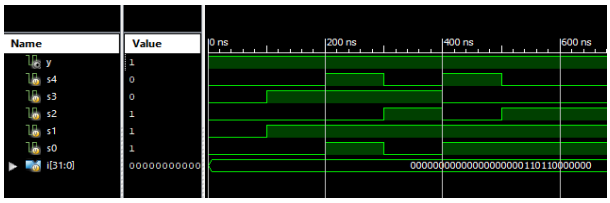

Fig. 18: Simulation results for 32x1 MUX using decoder

Conclusion

Power consumption has become an important factor in designing combinational circuits. By using Reversible Decoder, it is possible to reduce it to an optimum level. This project presents various combinational circuits such as fulladder, multiplexer, comparator, and so on. These are designed for use with minimal cost and minimum garbage output.

These circuits are designed to provide a low-cost and high-quality output. They can be commonly used for minimizing garbage and quantum cost. For 3x8 decoders, the 2x4 decoder can be used followed by 4 fredkin gates. For 4x16 decoders, the 3x8 decoder can be used followed by 8 fredkin gates. This concept of designing multiple output to required number of inputs simplifies the work of logic circuits. This concept is commonly utilized in reverse logic circuits to increase the number of outputs. Combinational circuits are used to implement various digital circuits with higher performance.

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