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An Improved Design of Low-Power High-Speed Accuracy Scalable Approximate Multiplier

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Abstract

Approximate multiplication is a technique that can be used to reduce energy consumption and improve accuracy. Multiplication is a fundamental function of many error-tolerant applications. The proposed accuracy-controllable multiplier can be dynamically adjusted to meet the accuracy requirements. It can generate a carry-maskable product with a defined length. The proposed algorithm can dynamically modify the carry propagation length for optimal accuracy. The proposed tree compressor has a partial product tree that is approximated by the carry maskable adder. The partial product tree is computed by the proposed multiplier. The proposed approximate multiplier is proposed to consist of an ATC and a carry-maskable adder. The ATC and the CMA are both power-efficient and feature a simple circuit structure.

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Introduction

Most commonly, image processing and recognition applications are tolerant of small inaccuracies. This function is typically used in high-complexity applications where computational accuracy is not an issue. However, it can also be used to reduce power consumption. Approximate computing is a technique that can reduce the power consumption and increase the reliability of error tolerant applications. This procedure is commonly used in error tolerant domains.[1] Different kinds of error-tolerant applications have varying requirements when it comes to accuracy. If the accuracy of multiplication is set, power will be wasted if it is not required. If it is dynamically reconfigurable, then approximate multipliers should have the same accuracy requirements for different program phases. The paper aims to develop an approximate multiplier designthat can dynamically control the accuracy of a given function. This design can be configured to work seamlessly with various carry propagation adders. A carrymaskable adder is proposed to enable a programmer to dynamically modify the operation of a carry propagation adder. The masking carry propagation of the CPA is achieved by replacing it with theproposed CMA. A tree compressor is used to reduce the accumulation layer depthof a partial product tree. A term that simplifies the process of achieving power andaccuracy requirements is introduced. This concept simplifies the process of implementing a partial product reduction (PPR) component. An approximate multiplier is a combination of acompressor and adder. It is commonly used in the design of calculators. This multiplier was implemented in Verilog HDL. It is a combination of the conventional and approximate multipliers.

The remainder of this paper is organized as follows. Section II reviews previous literature works. Section III introduces the accuracy scalable approximate multiplier after explaining the tree compressor and the CMA. Section IV evaluates the multipliers experimentally and simulation results were presented. Section V presents our conclusions.

Literature Work

The adder is a basic component of most multipliers. Mahdiani et al.[2] proposed the lower-part-OR adder. It is

commonly utilized for adding the lower bits and the precise adders for the upper bits. It uses the same concept as our proposed CMA, but it uses a dynamically reconfigurable method. A carry propagation delay reduction technique was proposed by Liu et al. In this study, Liu et aL.[3] proposed an approximate adder to reduce the carry propagation delay of partial product accumulation. They proposed a recovery vector that can improve the accuracy of an operation. The recovery vector can be selected with the help of a designer.

In order to reduce the size of the multiplier, Hashemi et al.[4] propose a technique that uses the following k bits for both inputs. Intricate techniques were proposed to reduce the size of a multiplier by detecting the leading bits of an input and selecting the following k bits for both inputs. Both[3] and[4] allow a static trade-off between power consumption and accuracy. The ability to maintain a static trade off between power consumption and accuracy is very useful in terms of reducing system complexity. The power consumption and accuracy limits are statically controlled. The recovery vectors and input operands are defined during the design process and are not dynamically controllable, unlike with our proposed multiplier.

A system-level technique that would disable a part of the combinational logic was proposed by Moons et al [5]. It can also trade off accuracy for power. It can change the number of pipeline stages and voltage scaling modes. Our proposed multiplier disables a part of the logic in the CPA that enables the reduction of power consumption. It does not require a pipeline system or control circuits.

Accuracy Controllable Multiplier

The design of the multiplier has 3 integral parts: (i) AND gate used for partial product generation; (ii) PPR using an addertree; and (iii) addition to produce the finalresult using a CPA. Powerconsumption and circuit complexity are dominated bythe PPR [6], and the multiplier's critical path is dominated bythe propagated carry chain in the CPA [7].

This section is organized as follows. Section III-A explainshow the partial product layer is simplified by the approximatetree compressor. Section III-B introduces the CMA. Finally, Section III-C presents the overall structure of the accuracy scalable approximate multiplier, which uses the proposedadder and treecompressor.

A. Approximate Tree Compressor

Figure 1(a) shows an accurate half adder, for which thefollowing equation can be obtained:

$$\{c,s\} = a + b = 2c + s = (c + s) + c$$

where {,} and + denote concatenation and addition, respectively. a XOR b generates c and s is generated by a AND b, so (c + s) can be generated by a OR b. Based on theabove, consider the basic logiccell shown in Fig. 1(b), forwhich the following equations results

$$p = c + s$$
$$q = c$$
$$\{c,s\} = a + b = p + q$$

An incomplete adder cell or an iCAC is a cell that shows the truth about a given adder Table I. Ascan be seen, q is equal to c. While p is not equal to s, the precisesum can be obtainedbyadding p and q, so the iCAC is not an approximate adder but an element of a precise adder. By extending the above equation to m bits, the followingequation can be obtained:

$$A + B = P + Q$$

where A, B, P, and Q are m-bit values, the bits of whichcorrespond to a, b, p, and q, respectively. A row of eight iCACs, used for 8-bit inputs, is shown in Fig. 2.

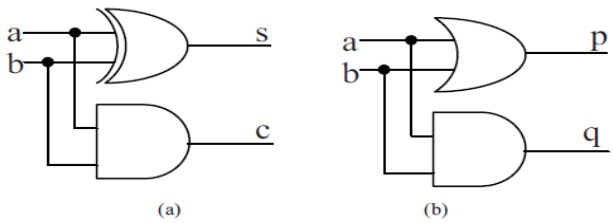

Fig. 1: (a) Accurate half adder and (b) Incomplete adder cell

Table I: Truth Tables for Accurate Half Adder And Incomplete Adder Cell

Inputs		Outputs			
		Accurate half adder		iCAC	
a	b	c	s	q	p
0	0	0	0	0	0
0	1	0	1	0	1
1	0	0	1	0	1
1	1	1	0	1	1

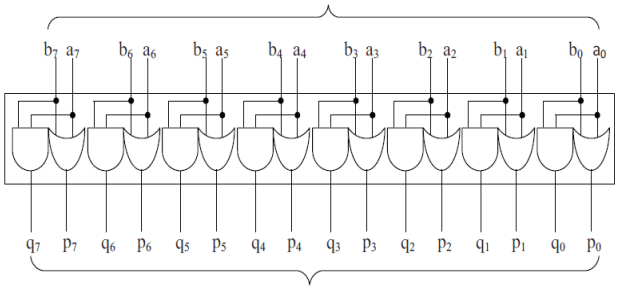

Fig. 2: A row of incomplete adder cells with two 8-bit inputs

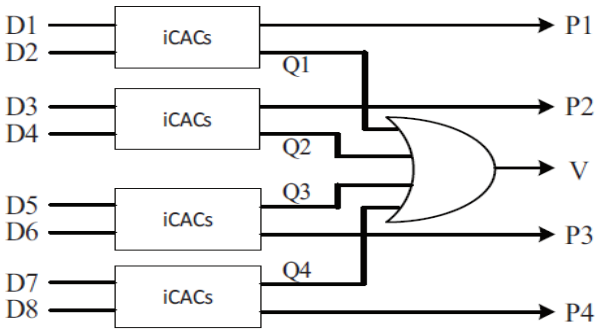

Fig. 3: Structure of an approximate tree compressor with eight inputs

Lets us see the example of an 8-bit adder with the two inputsA = 01011111 and B = 00110110. The accurate sum S is10010101, while the row of iCACsproduces P = 01111111 andQ = 00010110. Resultant equation is

$$S = P + QS = P + Q \quad (1)$$

While S is obtained from P and Q, P can be used as anapproximation for S, and Q can be used as anerror recoveryvector for the approximate sum P.

Two 8-bit inputs:

A = {a7, a6, a5, a4, a3, a2, a1, a0}

B = {b7, b6, b5, b4, b3, b2, b1, b0}

Two 8-bit outputs:

Approximate sum: P = {p7, p6, p5, p4, p3, p2, p1, p0}

Error recovery vector: Q = {q7, q6, q5, q4, q3, q2, q1, q0}

Converting the row of iCACs to n from two to three is an efficient method to get the n/2 Qs. If the sum of the two Qs is equal to one, the number of Qs becomes reducedto one. Remember that P is greater than S and Q is equal to C. OR gates can be used to generate an approximate sum of the n/2 quints without losing accuracy.

The approximate sum is the compensation vector that relates to the accuracy of the tree. It is named after the approximate tree compressor. An ATC with eight inputs is called an ATC- n. The structure of its eight inputs is shown in Fig. 3. The rectangles represent the rows and the number of iCACS in each row. For example, if there are four miCACs in D1, D2, etc., then four rows of m-bits are required to build an ATC-8. To construct the ATC-8, we need to construct four approximate sums, four correctness recovery vectors, and four error compensation gates.

B. Carry-Maskable Adder

A carry-maskable CMA is proposed to enable precise control of the accuracy of the data. It is similar to a k-bit CPA in that it has a carry-maskable half-adder and a carry-maskable full adder. The structures of the carry-maskable partial and fulladders are presented in Fig.4.

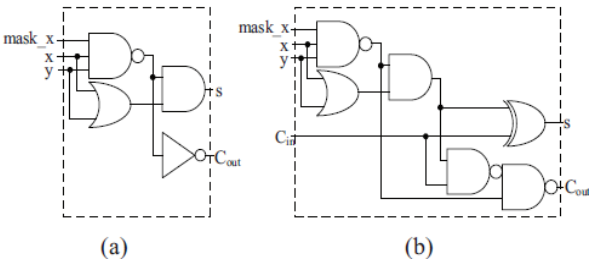

Fig. 4: (a) Carry-maskable half adder, (b) Carry-maskable full adder

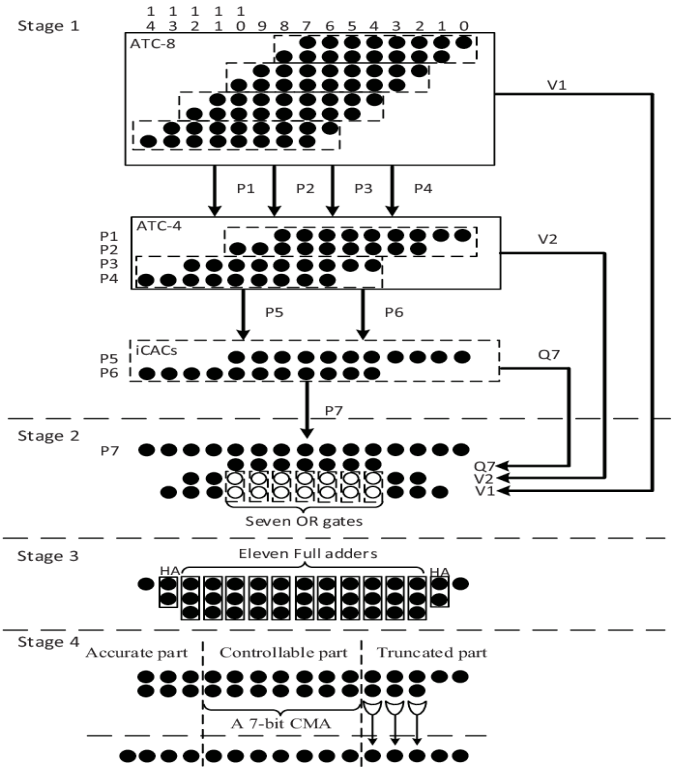

Fig. 5: Structure of 8-bit Multiplier with 8x8 partial products

In the proposed half adder, when mask_x is 0, S is equal to x OR y and Cout is equal to 0. If mask_x is 1, then the mask_x is equal to the xOR b and the xAOR y. When mask_x is enabled, it does not function as an accurate half adder. It can also be turned on by default. The proposed adder is similar to the Half adder in that it works as an accurate adder when mask_x is enabled. It outputs either Cout or S, depending on the option.

C. Overall Structure

An n-bit multiplier consists of 2^n rows, each of which has n partial products (PP), so there are nxn PPs in total. Usingthe ATC-n introduced in the previous section, the rows can be replaced by $n/2 + 1n/2 + 1$ rows. Figure 5 shows an example of an8-bit multiplier with 8 x 8 PPs. The PPR is performed in threestages (Stage 1, Stage 2, and Stage 3) and the CPA is performedin Stage 4. The PP

generation step is not shown. Each dotrepresents a PP. The least significant bit (right side) is bit 0, andthe most significant bit (left side) is bit 14. The solid rectanglesin Stage 1 represent ATCs and the dashed rectangles represent rows of seven iCACs. Every row of iCACs includes PPs that are not processed: for example, the PP at position 0 in the firstrow and the one at position 8 in the second row of the first iCAC block in ATC-8 are not processed.

In Stage 1, eight rows of PPs are reduced to four rows (P1,P2, P3, and P4) and one accuracy compensation vector (V1) byan ATC-8. The four rows are further reduced to two rows (P5and P6) and another accuracy compensation vector (V2) by anATC-4. A final row of iCACs then processes P5 and P6 andgenerates P7 and Q7. In summary, Stage 1 uses an ATC-8, anATC-4, and a row of seven iCACs to compress the 8 x 8 PPsto four rows (P7, V1, V2, and Q7).

In Stage 2, there are four PPs for each of bits 4 to 10. Inorder to achieve a lower path delay, OR gates are used to sumV1 and V2 approximately. The empty circles for V1 and V2represent the bits which are summed using OR gates. Seven ORgates are required in total and the four rows are compressedto three.

In Stage 3, full adders and half adders are used to compressthe three rows to two. Two half adders are required for bits 1and 13, and eleven full adders are required for bits 2 to 12.

Addition using a CPA is required after PPR to produce thefinal result. For an 8-bit Wallace tree multiplier, the length of CPA is 13. In Stage 4, the CPA is divided into three parts inorder to reduce the length of the carry propagation. Since thelower bits are not significant for accuracy, bits 0 to 4 are definedas the truncated part and three OR gates are used to generate thevalues for bits 2, 3, and 4 of the final result. Because there is nocarry out from the truncated part, the length of the CPA isreduced to 10. Since the upper bits are the most significant foraccuracy, bits 12 to 14 are defined as the accurate part, and threeaccurate adders are used to generate the values for these bits ofthe final result.

The precision-scalable part of the CPA is between the accurate and truncated parts. This part is very important for both pathdelay and accuracy. In Stage 4, bits 5 to 11 in the CPA arereplaced by a 7-bit CMA. Note that every 1-bit CMA has amask_x signal. The u-bit upper bits are configured as a 2-input or 2-out CPA gate. The lower bits are used as mask_x signals. When u =7, it operates as a 7-bit CPA, while u = 0, it operates as a 2-input OR gate. This feature cuts the power consumption by reducing the switching activity in some logic gates.

Simulation Results

The proposed scalable accuracy approximate multiplier was implemented using the Verilog HDL language in version

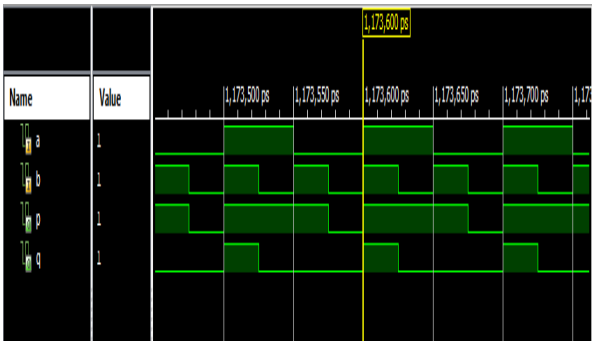

Fig. 6: Simulation result for Incomplete adder cell

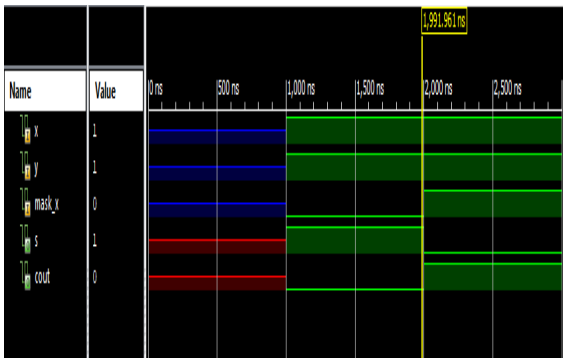

Fig. 7: Simulation result for Carry Maskable Half Adder

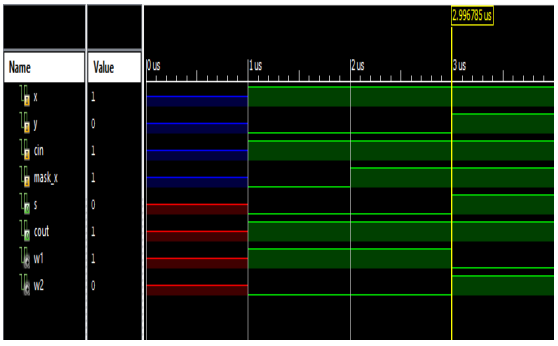

Fig. 8: Simulation result for Carry Maskable Full Adder

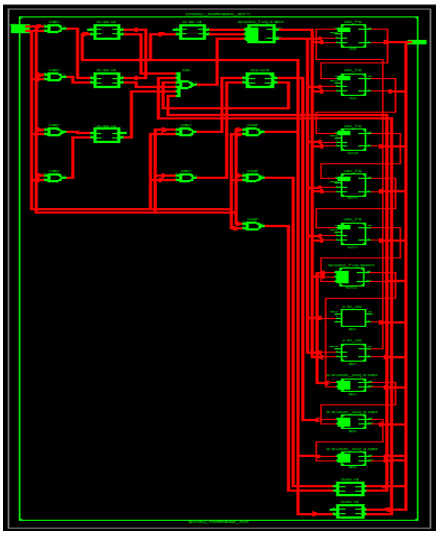

Fig. 9: RTL Schematic for 8x8 Accuracy controllable Multiplier

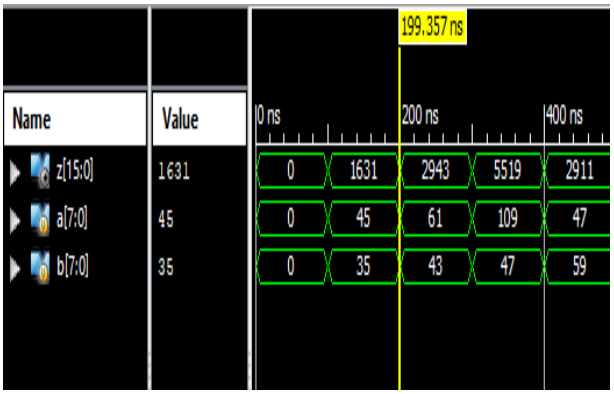

Fig. 10: Simulation result for 8x8 Accuracy controllable Multiplier

14.7. The following figures show the simulation outputs of the code.

Conclusion

In terms of signal processing and image processing, approximate computing is commonly utilized for processing complex and non-complex tasks. An approximate multiplier that is accurate-scalable has been proposed in this paper to reduce power consumption and provide a shorter critical path delay. The proposed carry maskable adders can be dynamically controlled through a set of controllability parameters. The carry maskable adders are commonly used for carry cell calculations. The proposed CMA achieves its dynamic controllability by implementing carry maskable adders. The simulation results for the carry maskable adders have already been shown. The implementation of these adders simplifies the calculation of the accuracy multiplier.

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