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Design of Unbalanced Ternary Logic Gates and Arithmetic Circuits

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Abstract

The design of ternary Logic gates–Ternary NAND, Ternary NOR and Standard Ternary Inverter based on the 18nm FinFET technology is proposed. The Ternary logic systems replaced Existing Binary logic systems with their good operating speed, energy efficiency, information density and Reduced circuits like chip area and interconnections. Instead of using large Resistors, the proposed model consists of 18nm FinFETs, reducing the number of resistors used. The proposed ternary logic gates are then used to carry the arithmetic operations that are basic and implement various complex functions. These ternary logic gates show the significant advantages of chip area, energy and power consumptions, denser fabrication and component count. The ternary half- adder and ternary half-subtractor circuits are then implemented by utilizing the proposed gates and then verified through the simulations. The results are then compared with the existing designs of MOSFET based Ternary logic gates. The parameters like power consumption are compared with the current MOSFET models, and then the proposed models are simulated. For simulations, Cadence Virtuoso tool and MATLAB are used to verify the authenticity of proposed designs.

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Introduction

Digital circuit designs are linked with the Binary logic, which has two possible values, which are 0 and 1 or 'true' and 'false' from the past many years. The various operations related to arithmetic plays a vital role in digital circuits. As mentioned above, the binary logical values are used as discrete values of charge or voltage, current. The primary design issues related to the binary logic implementation in the computing systems are in the range of nanoscale, the 'interconnect limitation'. The integrated circuit designs comprise several interconnect lines, which leads to the delay, noise, and increase in power consumption. Interconnects are the crucial components that identify the integrated circuits' performance based on which the semiconductor devices are being scaled continuously. To address this critical issue, there is an emerging technology known as Multiple-Valued Logic (MVL), which is a stable solution for managing the delay and other issues mentioned above related to the interconnects in modern circuits. The implementation of MVL circuits brought various benefits compared to the Binary logic for digital system designs. The first and essential advantage of MVL is that it can transmit or send more information through each wire, and in each memory cell, it can store more than one bit of data.[1] At the same time, Binary systems can hold only a single bit of information for each cell.

Hence, we can say that the implementation of MVL based designs enhances storage capacity and reduces the number of interconnects. MVL simplifies the routing of wires and integrated circuits based on packaging. In the interconnects, the implementation of MVL design

resulted in area reduction and power dissipation in ultra-high-density FPGAs and SOCs.[2,3] MVL was playing a vital role and emerged as a promising alternative to the binary logic systems. These MVL designs help implement very high-density logic and method of information with the operational speed very high, reduction in chip area, and the lower computational stages.[4] In this modern technology, MVL is also widely used to design various logical and arithmetic operations. Due to this, MVL uses more than two logic levels to carry out the processing and computing. Based on this criterion, MVL is divided into ternary, which is base three or quaternary, which is base four and so on, depending on the number of levels in logic.[5]

Taking all these into consideration, along with the issues belonging to the hardware implementation, Ternary logic systems based on the radix 3 is the most significant method of implementing the MVL systems.[6] However, these MVL systems are more sensitive to crosstalk effects and noise.[7] Thomas fowler is the inventor who first reported the ternary in 1840[8] of English origin. "SETUN" is the computing machine invented by Sergei Sobolev and Nikolay brusentsov, who are Russian inventors, based on the number logic present in the ternary in the 1950s. Ternary numbers were having two central representations;[9] the first representation is the balanced representation, -1, 0 and 1 are the logical voltage levels by which ternary numbers are represented. Another one is unbalanced representation, and this representation uses 0, 1 and 2. These logic gates were first implemented using CMOS technology. So, in CMOS transistor dimensions, there is a higher sensitivity of logic systems. MVL used by arithmetic and logical designs has faced many challenges in terms like parameter variation, gate control reduction, short channel effect and high leakage power.[10] For the betterment of MVL circuit designs, various types of technologies such as advanced 18nm FinFET, carbon nanotube field-effect transistors (CNTFET), quantum-dot cellular automata (QCA), and many more have been introduced. Among all these technologies, advanced 18nm FinFET technology is used in this paper and also, there is an implementation of arithmetic circuits based on the proposed models on the FinFET.

FinFET

One of the ongoing technology trends handling the semiconductor industry is the adaptation of the FinFET processes.

It is a metal-oxide-semiconductor field-effect transistor (MOSFET) which will be built on a substrate in which the gate is placed on the channel consisting of two, three, or four sides as shown in Fig. 1, called the multi-gate device, and these sides are wrapped around the canal which in result forms a double gate structure. These devices, which contain drain and source regions, comprises fins on the silicon surface and hence given the generic name "FinFETs". These FinFET devices will generally have maximum current density and high speed in switching times than the standard planar CMOS technology.

Ternary Logic Gates

In this system of ternary logic, the unbalanced logical numbers are '0', '0.5' and '1', denoted by 0V, *VDD*/2 and *VDD*, respectively. But in the conventional binary system, we have only two levels of logical values, '0' is represented by 0V and '1' is represented by the *VDD*. The numbers can be expressed either way, like the balanced mode or the unbalanced mode in MVL systems. So, while implementing the negative voltages, some difficulties are raised, which results inconsistently, and the balanced method is rarely used. In this work, primarily, the unbalanced representation is used. The following table gives a clear idea of the ternary logic levels (Table 1).

This Table I shows that the ternary logic levels have an indeterminate form that is the third logic responsible for more information transmitter. This ternary logic is responsible for higher speed calculations of the arithmetic and logical operations.

Existing models of Ternary gates based on MOSFETs

1. *Ternary inverter*: The ternary inverter is a logical device that has three output combinations when we provide single possible input, and is divided into three categories, namely positive ternary inverter (PTI), Negative ternary inverter (NTI) and Standard ternary inverter (STI). The STI can generate three possible output voltage levels for three inputs. Where both

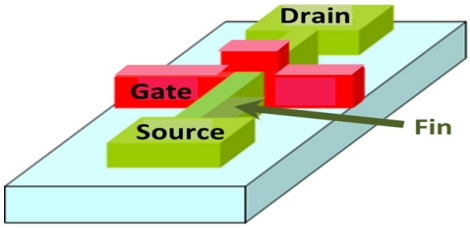

Fig. 1: FinFET.

Table 1: Logic Levels And States Of Ternary Gates

Logic level	Operation / State
0	False
0.5	True
1	Indeterminate

NTI and PTI will take only two output voltage levels, as shown below in the truth table representation.

Table 2 shows the truth table with three inputs 0, 1 and 2. For input 2, the outputs are zeroes for all three inverters. Mathematical equations related to the STI, PTI and NTI are in unbalanced representation as shown.

$$Y_0 = f_0(x) = 1 - x$$
$$Y_1 = f_1(x) = \{1 \ if \ x \neq 2; 0 \ if \ x = 1\}$$
$$Y_2 = f_2(x) = \{1 \ if \ x = 0; 0 \ if \ x \neq 0\} \quad (1)$$

The Fig. 2 shows a ternary inverter using MOSFETs where the input is given to the two FETs as shown in the Fig. 2, and the capacitor is connected to the output as shown above.

2. *Ternary NAND & Ternary NOR:* The following ternary NAND and ternary NOR gates are based on the MOSFETs for the two inputs X1 and X2 are represented by the below equations as shown

$$Y_{NAND} = \overline{min\{X_1, X_2\}}$$
$$Y_{NOR} = \overline{max\{X_1, X_2\}} \quad (2)$$

Table 3 shows the truth table for both Ternary NAND and Ternary NOR, which uses X1 as input one and X2 as input two and also the Ynand and Ynor as the outputs as shown.

The circuits shown in Fig. 3 are ternary NAND and ternary NOR circuits, respectively, implemented based on the MOSFETs. These circuits are more extensive, and there are some drawbacks involved in the size. The comparison between the MOSFET and FinFET gives a clear idea about the fault of MOSFET over FinFET.

Tabl 2: Truth table of STI, PTI & NTI

Input	STI (Y0)	PTI (Y1)	NTI (Y2)
0	1	1	1
0.5	0.5	1	0
1	0	0	0

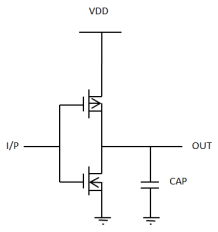

Fig. 2: Ternary inverter using MOSFETs.

B. MOSFET VS FinFET

Fig. 4 shows illustrates a FET, which is planar, and the red color line shows where the fin will coincide with the gate on a FinFET. In this modern technology, we require more computational power; more transistors are needed to achieve this, leading to larger chips. So, we have only one way to accomplish this computational power. It is to reduce the transistor's size, but if we decrease the dimensions of the transistor, the distance from source to drain also reduces the gate electrode's ability to maintain the flow of current in the channel region. Because of this, planar MOSFETs will bear short-channel effects.

Hence, FinFET devices play a vital role in exhibiting rude channel behaviour. FinFETs also have switching times

Table 3: Truth table of TNAND & TNOR

Input X1	Input X2	Y NAND	Y NOR
0	0	1	1
0	0.5	1	0.5
0	1	1	0
0.5	0	1	0.5
0.5	0.5	0.5	0.5
0.5	1	0.5	0
1	0	1	0
1	0.5	0.5	0
1	1	0	0

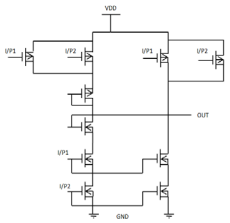

Fig. 3: ternary NAND circuit using MOSFETs. (b) ternary NAND circuit using MOSFETs.

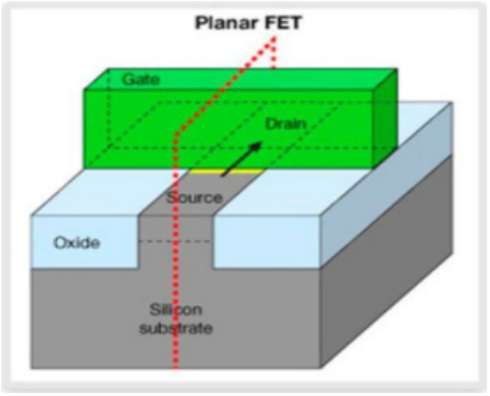

Fig. 4: Plane FET, the red line shows where the fin will coincide with the gate on FinFET.

and current density, shorter and higher, respectively, compared to conventional planar MOSFET technology. Hence FinFETs can cover the drawback of MOSFET in the proposed design.

Proposed models using 18nm FinFET

A. Ternary Inverter

The ternary inverter above in Fig. 5 is designed using 18nm FinFET and gives three standard outputs for the single possible input.

B. Ternary NAND & Ternary NOR

The circuits shows in (Fig. 6) are the proposed circuits that use the 18nm FinFET technology, which reduces the complexity and short channel effects. To increase the ease of computational speeds and for the faster processing of arithmetic and logical functions. The proposed models are shown below in Fig. 6.

The circuits shows, which are Fig. 6, are based on 18nm FinFET and consist of P-type and N-type FinFETs. Based on the above ternary gates, the arithmetic circuits are then implemented. The half subtractor and half adder using ternary logic are implemented and designed using the proposed ternary gates, as shown below.

C. Ternary Half adder & Ternary Half Subtractor

The following circuit is proposed using some binary gates and ternary gates based on the FinFETs to reduce the complexity as the previous models use MOSFETs. The proposed model logical circuit is given in Fig. 7.

The circuit consists of a decoder and other subcircuits like binary NAND, ternary NAND, not, summer and adder. Among them, the primary input circuit is a decoder.

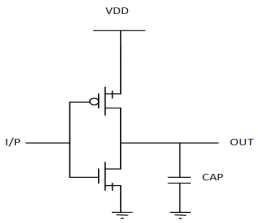

Fig. 5: Ternary Inverter using 18nm FinFET.

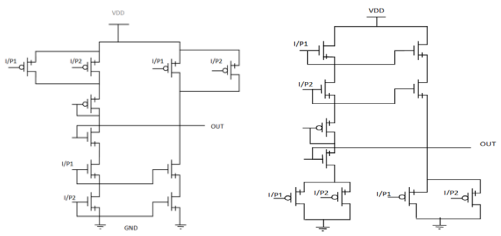

Fig. 6: (a) Ternary NAND circuit design using 18nm FinFET. (b).Ternary NOR circuit design using 18nm finFET.

The internal circuit is designed using 18nm FinFETs, as shown in Fig. 8.

The Fig. 8 represents the decoder circuit used in both half adder and subtractors. The truth table of the decoder circuit is as shown below.

From Table 4, it is observed that the states {0, 1, 2} representing the voltage levels {0, *VDD*/2, *VDD*} which are of three-level are converted into two-level, i.e. {0, 2}. Hence, we can conclude that the central role of the decoder here is to convert ternary logic or three-levels into binary logic or two-level. In a ternary system, the number of digits needed is log3 to the base two times shorter than binary logic. Both the binary as well as ternary half adders have the sum and carry. In binary half-adder design, the carry and the sum outcomes take only two logic values, whereas, in the ternary, they take three possible output logic values. Table 5 represents the table of values which gives a clear idea.

The output equations of half adder(ternary) by using Karnaugh map from Table V can be derived as shown below:

$$Sum = A_2B_0 + A_1B_1 + A_0B_2 + 1 \cdot \left(A_1B_0 + A_0B_1 + A_2B_2 \right) \quad (3)$$

$$Carry = 1 \cdot \left(A_2B_1 + A_2B_2 + A_1B_2 \right) \quad (4)$$

Similarly, we use the same proposed design models for the following circuit as shown below in the Fig. 9.

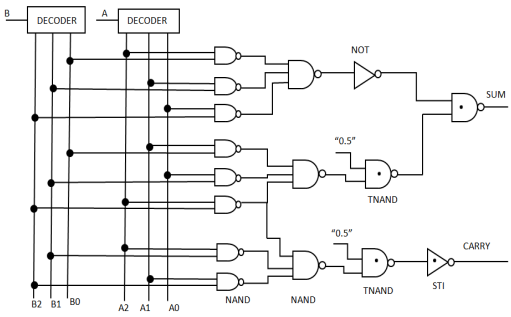

Fig. 7: Schematic of ternary Half adder.

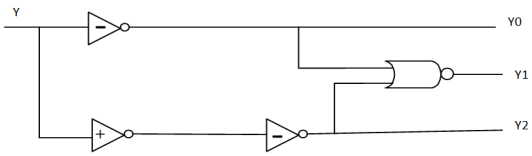

Fig. 8: Schematic of decoder.

Table 4: Truth table of decoder

Input (Y)	Input X2	Y NAND	Y NOR
0	1	0	0
0.5	0	1	0
1	0	0	1

Table 5: Truth table of ternary half adder

Input A	Input B	SUM	CARRY
0	0	0	0
0	0.5	0.5	0
0	1	1	0
0.5	0	0.5	0
0.5	0.5	1	0
0.5	1	0	0.5
1	0	1	0
1	0.5	0	0.5
1	1	0.5	0.5

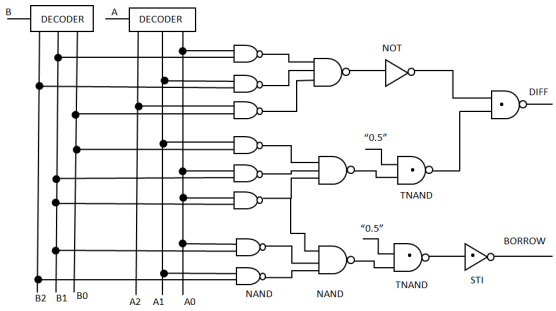

Fig. 9: Schematic of ternary half-subtractor.

The half-subtractor (ternary) shown in Fig. 9, produces two outputs difference and borrow. It is a combinational logic circuit. This circuit subtracts one bit from the other. The output equations are as follows.

$$Diff = A_0B_1 + A_1B_2 + A_2B_0 + 1 \cdot \left(A_1B_0 + A_2B_1 + A_0B_2 \right) \quad (5)$$

$$Borrow = 1 \cdot \left(A_0B_1 + A_0B_2 + A_1B_2 \right) \quad (6)$$

The circuit's schematic contains proposed decoders, Binary NAND gates with two inputs and three inputs, binary inverter, proposed STI, and three proposed TNAND gates.

D. Sub circuits of Ternary half-adder and half-subtractor using 18nm FinFET

The proposed design contains different subcircuits that are designed using FinFETs in cadence virtuoso software. Some of the gates are to be developed in the software to implement these circuits and create the symbols of the following gates, 2-input binary NAND gates, 3-inputs binary NAND gates, binary inverter, proposed STI and three proposed TNAND gates (Fig. 10).

The proposed circuits both consist of decoder circuit shown in Fig. 10 and consists of PTI and STI. The truth tables of PTI, STI and NTI are shown in Table II above, and the remaining circuits are 2-input binary NAND gates, 3-input NAND gates, binary inverter and TNAND gate. The binary NAND gate (both 2-inputs and 3-inputs) is shown in

Table 6: Truth table of Ternary Half-Subtractor

Input A	Input B	SUM	CARRY
0	0	0	0
0	0.5	0.5	0
0	1	1	0
0.5	0	0.5	0
0.5	0.5	1	0
0.5	1	0	0.5
1	0	1	0
1	0.5	0	0.5
1	1	0.5	0.5

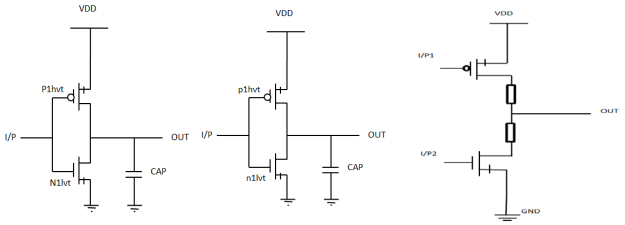

Fig. 10: (a) PTI, (b) NTI, (c) STI

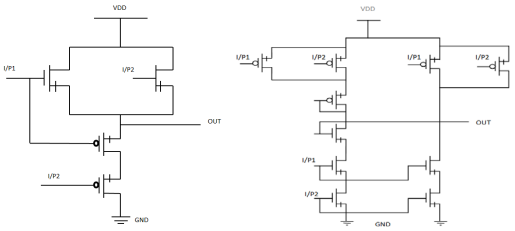

Fig. 11: Schematic of (a) Binary NAND b)Ternary NAND gate.

Fig. 11 below, and the number of 2-inputs binary NANDs used is 15, and 3-inputs NANDs are 3.

The TNAND used in Fig. 6 are represented in Fig. 11, as shown.

Experimental Findings and Simulation Results of Proposed Design

The proposed model or design has been simulated on the Cadence Virtuoso tool using the FinFET node model. The output of the decoder circuit used in the invention is shown in Fig. 12. The decoder returns three results in ternary logic for the given input in ternary logic in the truth table in Table 4.

The transient responses of both half adder and subtractor are shown in Fig. 13 and Fig. 14, respectively. The produced responses of these circuits after simulation were similar to the truth tables shown in table-5 and table-6 for given inputs. The parameters of proposed circuits like power consumption, total delay and PDP

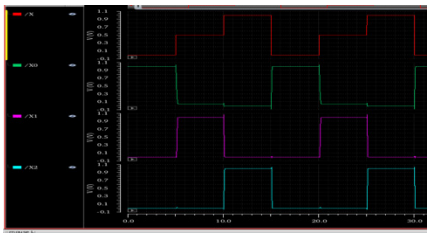

Fig. 12: Transient response of decoder.

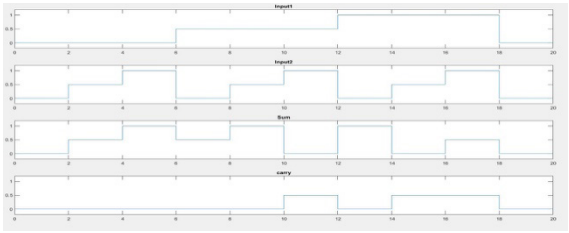

Fig. 13: Response of ternary half adder.

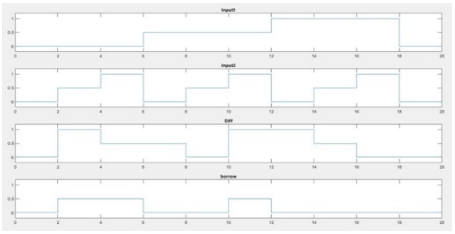

Fig. 14: Response of ternary half subtractor.

Table 7: Comparison of Power Consumption Between Existing And Proposed Models

The proposed design has produced power consumption results, which are slightly better than the existing models of MOSFETs.

Configuration	Power consumption (nW)
Existing ternary half adder using 32nm MOSFET	8.38
Existing ternary half subtractor using 32nm MOSFET	7.95
Proposed ternary half adder using 18nm FinFET	6.73
Proposed ternary half subtractor using 18nm FinFET	6.54

are compared to the existing model parameters. The comparison table is shown in the below table, numbered as table-7.

The output of the ternary half adder is compared with the truth table shown in Table 5, and it is the same as the values in the truth table.

The output of the ternary half subtractor is compared with the truth table shown in Table 6, and it is the same as the values in the truth table. Now let us look into the power comparisons of the existed models to the proposed models.

Conclusion

The Ternary circuits half adder and subtractor proposed in this paper are designed using ternary logic, which has improved compared to the drawbacks of the binary logic. These circuits are created using 18 nm FinFET, and the parameter power consumption has improved compared to the previously proposed designs. The proposed arithmetic circuits designed were simulated in Cadence Virtuoso software. The simulated results validated the correct operation of the realized circuits. The FinFETs have shown various advantages in the proposed method, like suppressing short-channel effects, better channel control, faster-switching speed, higher drain current, lower switching voltage, and lower power consumption. Hence the proposed design showed slight benefits compared to the existing model.

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