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Research Article

DESIGN OF RELIABLE AND EFFICIENT MANCHESTER CARRY CHAIN ADDER BASED 8-BIT ALU FOR HIGH SPEED APPLICATIONS

AGUS RISTONO*, PRATIKTO BUDI
[1,2]Industrial Engineering Department, University of National Development , Indonesia
Email id : agus.ristono@upnyk.ac.id
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ABSTRACT
This paper gives a detailed design and implementation of an 8-bit ALU for using Manchester carry chain adder in order to minimize the delay and power. The designed ALU is simulated using cadence virtuoso 45 nm process technology. The obtained results were compared with the existed results and its clearly indicates the proposed 8 bit ALU is more reliable and accurate with the existed architecture ,And also it occupies less area and faster.

keywords: Arithmetic and logic unit(ALU),Manchester carry chain full adder, Low power and less area.

INTRODUCTION

With the advancement of the technology, increasing the demand for the digital electronic devices enormously. According to Moore's law [1-3] the number of transistors has been doubled for every 36 months. As results it increases the interconnection over the circuit ,therefore delay and power should be increase rapidly.Now a day's majority of the microprocessors and digital signal processors(DSP) dynamic power consumption becomes one of the serious issue.As dissipation of the power is more, linearly it will degrades the reliability of the device. However the dynamic power being as a activity it could not be eliminated completed but it should be minimized considerably. Many of the electronic devices ALU is one of the basic unit and typically it will performs all types both arithmetic and logical operations. The widely used full adders in ALU were ripple carry adder, carry skip adder, Manchester adder and koggstone adder respectively. The basic symbol for ALU as shown in figure 1.

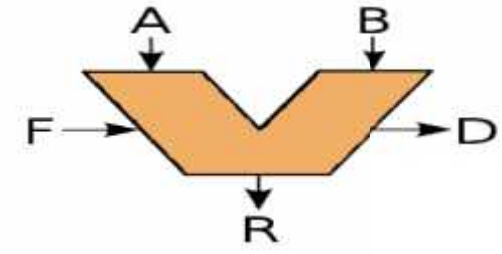

Figure 1:Symbol for ALU.

The rest of the paper is organised as follows: section 2 describes the background and earlier work of ALU. Section 3 describes the operation of the single bit ALU and section 4 gives the performance of 8 bit ALU and its simulation in 45nm technology, finally section 5 concludes the conclusion.

Background of ALU

ALU is a core part for the most of the present day digital computers. It executes the operations such as increment, decrement, addition, subtraction ,AND,OR,XOR,XNOR, etc. The ALU receives the information from register and performs the desired operation based on the control signal. The kind of operations to be performed is given by table1.the block diagram of ALU as shown in figure 2.And corresponding operations of the ALU as shown in table2 respectively.

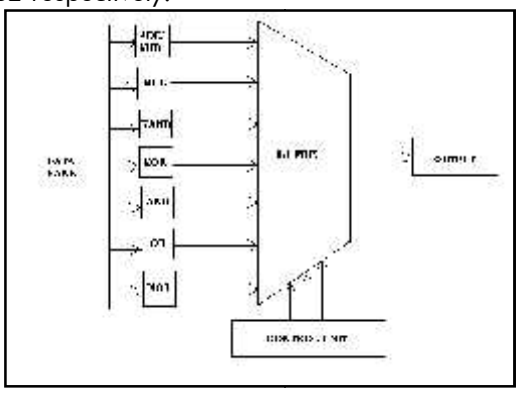

Figure 2:Block diagram of ALU.

Operations of ALU

(1) If s0="0",s1="0" and s2="0" then the ALU is performs the OR operation.
(2) If s0="0",s1="0" and s2="1" then the ALU is performs the XOR operation.
(3) If s0="0",s1="1" and s2="0" then the ALU is performs the XNOR operation.
(4) If s0="0",s1="1" and s2="1" then the ALU is performs the AND operation.
(5) If s0="1",s1="0" and s2="0" then the ALU is performs the INCREMENToperation.
(6) If s0="1",s1="0" and s2="1" then the ALU is performs the DECREMENToperation.

(7) If s0="1",s1="1" and s2="0" then the ALU is performs the ADDITION operation.
(8) If s0="1",s1="1" and s2="1" then the ALU is performs the SUBTRACTION operation s respectively.

Table 1: Indicates the operations of ALU

S2	S1	S0	operation
0	0	0	OR
0	0	1	XOR
0	1	0	XNOR
0	1	1	AND
1	0	0	INCREMENT
1	0	1	DECREMENT
1	1	0	ADDITION
1	1	1	SUBTRACTION

1-Bit ALU

ALU is the heart of the all digital computers and hardware systems [4-8].the basic architecture of the 1 bit ALU as shown in figure 3.the architecture consists of XOR,AND,MUX and inverter gates respectively. A and B will acts as the input for the 1 bit ALU and selection lines s0,s1 and s2 is going to decides the type of operation to be performed.The 1 bit ALU is going to perform the mainly four basic operation such as AND,OR,ADDITTION,SUBTRACTION respectively. which are represented by table 2.

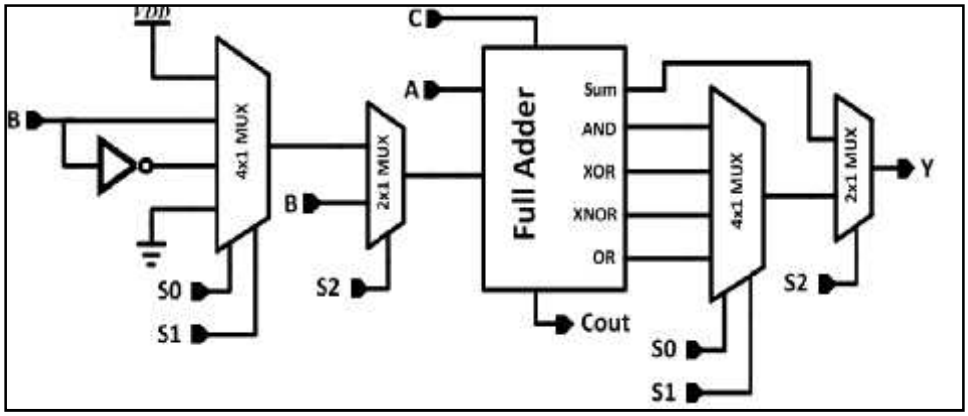

Figure 3:Logic diagram of 1-bit ALU.

Table 2:Operation performed by 1-bit ALU.

ALU OPERATION CONTROL LINES

Operation			Function
So	S1	S2	
L	L	H	AND
L	L	H	OR
L	H	L	ADD
H	H	L	SUB

8-bit ALU using Manchester carry chain adder

The 8 bit ALU is designed using Manchester carry chain adder(as shown in figure 4), which is responsible for doing arithmetic and logical operations. Which contains different number of modules such as 2* 1 multiplexer,4*1 multiplexer. Figure 4 depicts the circuit diagram of the 8 bit ALU. Here each input consists of 8bits ranging from (A0,A1,-----A8) and input B consists of ranging from(B0,B1,-----B8) respectively. Those can be divided in to two modules such as (4*1 and 4*1 multiplexers)[9-12].

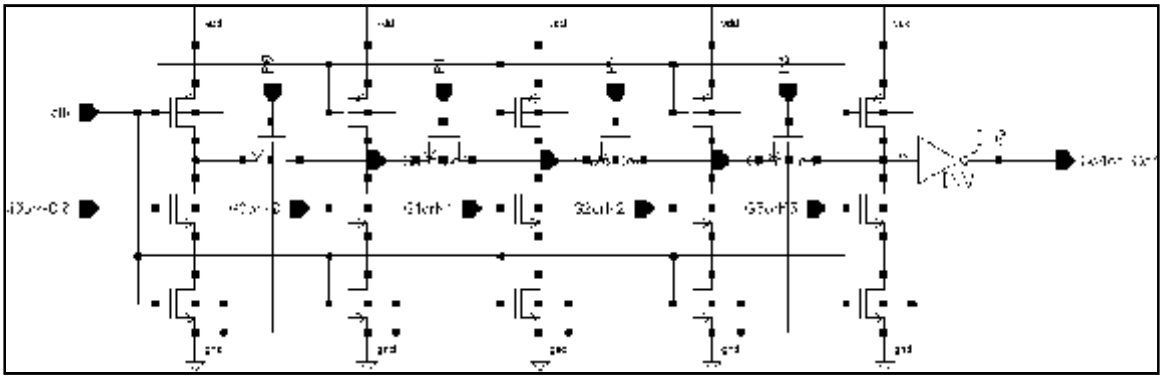

Figure 4:Manchester carry chain adder

simulation setup

The proposed 8 bit ALU is designed and simulated using the cadence virtuoso using 45 nm technology and spectre as a simulator. The voltage were applied ranging from 0.45 to 0.9v and estimated its delayparameters.we have applied a set of input combinations such as A=10110101 and B=11010101 and observed its output at different combinations ait was satisfied and produced the faith full results.the block diagram of 8 bit ALU as shown in figure 5 respectively.

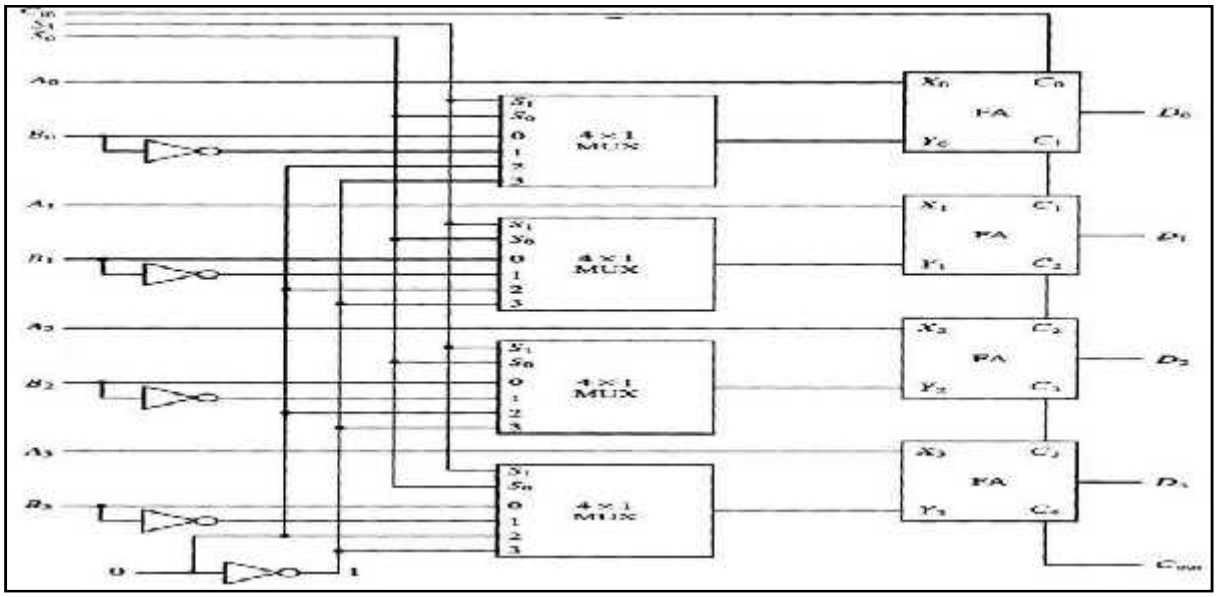

Figure 5 :8 bit ALU using Manchester carry chain adder.

Obtained results from 8-bit ALU

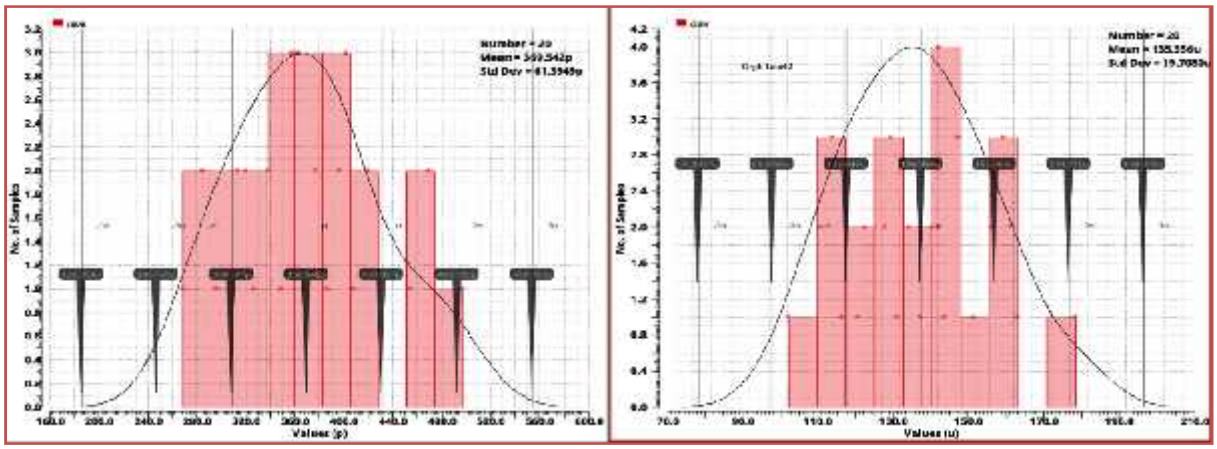

Figure 6 : variation of delay represented in histogram

Conclusion

This work represents the design of 8 bit ALU sing Manchester carry chain adder using technology of 45nm. from the simulation results ALU is consumes the less power and very small area with required swing respectively. the present design will up holds the threshold voltage of the MOSFET, however in high density chips it could switched significant level with respect to load.

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