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A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder

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Abstract

The primary component in most digital circuit representation, including the microprocessor data path element and the digital signal processor, is the binary adder. Binary Adders, which are arithmetic circuits used to add two binary digits, have their application in basic adders like full-adder and half-adder. Therefore, related study on improvement of efficiency of binary adder circuits is being done. In a Digital system, the critical logic component is Binary Adder. In VLSI executions, the best executable adders are parallel prefix adders. In many of the circuits such as multiplexers, memory elements and such alike, binary adders are basic element. Hence, the complete system performance can be improved, by improving the speed of binary adders, which also improve the speed of computing system. Area and power reduction are the main idea of designing of any circuit in the data path design of VLSI. The major requirement for processors and systems of high-performance, is always multiplication and addition with high-speed. In VLSI execution, the element having supreme performance is Parallel-prefix adders which are also known as carry-tree adders. This paper deals with the architecture and performance of the Carry-Select Adders (CSEA), Ripple-Carry Adders (RCA) and Carry-Skip Adders (CSKA). In the Implementation of CSKA, Carry-Select Adders (CSA) and RCA, Vivado Design tool is used for the execution, simulation, logical verification, and synthesizing is shown.

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Introduction

In any digital circuit, binary adders play an important role to add two logic bits. Not only as an important logical element but also in other units such as dividers, subtractors arithmetic logical units (ALU), and multipliers. Hence, any improvements made in binary addition can generate boosting of working of the entire system, by enhancing the performance of the computational system. RCA has the more advantages over many circuits as it carries out the carry of each adder and gives it as input to the next binary adder which reduces the time required to carry out the output. The RCAs are designed using multiple full adders which are connected parallelly to add N-bit number. Initially, the first full adder is given a carry to avoid the errors. The problem of using ripple carry adder is time complexity. The first full adder of RCA waits until the carry is generated. Carry-chain becomes a major problem in the binary adder circuits. As the input bits increase the carry chain also increases in size without any exception. Due to the increased carry-chain, there is a propagation delay, which leads to the decrement in speed efficiency. Fig. 1 shows an example of an 8-bit binary adder circuit.

One can observe that carry propagation, from Least Significant Bit (LSB) to the Most Significant Bit (MSB), is the longest possible path, which is also the worst case. To improve the carry chain propagation, we must accelerate the carry chain, for which different circuits are designed. Circuits such as CSKA, CSA and RCA are selected to improve the carry-chain propagation.

Although the Ripple carry adder are simple and efficient but they are slow. The reason behind this, is that the propagated carry has to go through all full-adder blocks, present in the circuit, to produce the final output. With drawback in each of these adders, the next circuit comes into picture, overcoming the previous adder drawback. This paper deals with architecture of RCA, CSA and CSKA for n bit, area required for each of the circuits and simulated results for each of the circuit.

The implementations that have been executed throw some light on the need required to use each of the circuit. When speed and not area is essential factor one can go carry select adder rather than ripple carry adder but if area is the needed factor then ripple carry adder is the best option out of three circuits mentioned. Vivado implementation section discusses about the efficiency in using Vivado software and its design flow.

Architecture of each of the circuit with an analysis on area required and propagation delay are done under the Architecture section. Finally some conclusions on the efficiency of each of the circuits and Vivado design metrics are given.

Vivado Implementation and Design Flow

Vivado design suit delivers ease of use, design productivity ahead a generation and system level integration. Enhanced system implementation is done by Vivado, as it pushes the device-density envelope which fits more components into a single device and makes the way faster. Low power and Powerful performance with predictable results can be expected, as the system consumes low power while using Vivado. Vivado Design Suite delivers unparalleled runtime and memory utilization as one require the less time to get desired output. The Vivado design suite delivers it faster than programmable logic devices. It accelerate the system integration with C-based IP Generation with Vivado High-Level Synthesis to provide better results.

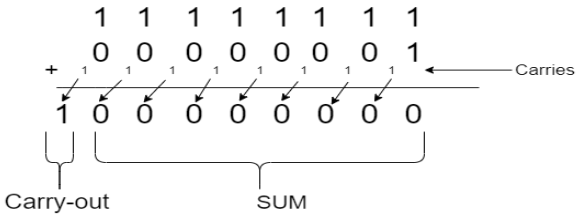

Fig. 1: Binary adder of 8-bit.

It is a Model-based digital signal processing (DSP) design integration using System Generator for DSP to generate the binary and other type of signals (Figure 2).

A. RTL logic

The RTL schematic of the vivado design flow (Fig. 3) gives us the overview of circuit and the number of gates required for the implementation. The RTL source files specify the project files and those sources can be used for code development, analysis, synthesis and implementation. Vivado design suite support multiple source file type which include Verilog, very high speed integrated circuit hardware description language (VHDL), system and XDC. The vivado simulator allow us to run the behavioural simulation of each source that is added to the source file. The ".vhd" file gives us the delay and output time of each bit. When the synthesized netlist file is available, vivado implementation provides all the features necessary to optimize, place and route the netlist file onto the target device. The vivado simulator allow us to dump the code onto the field programmable gated array (FPGA) device where we can see the needed result of the code written in the source file. Debug signals can be identified in the RTL design source which can be identified at their position by giving a message in a new dialogue box. While we run

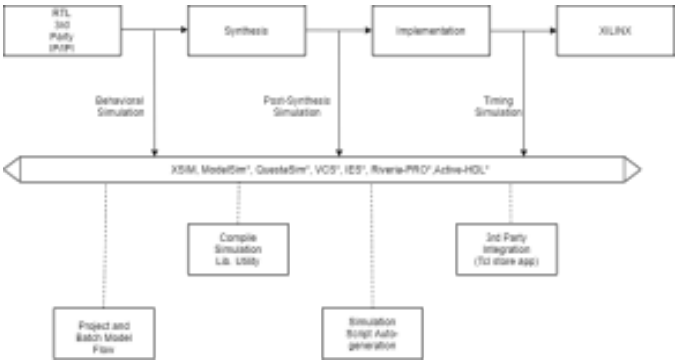

Fig. 2: Simulation Flow of Vivado.

Fig. 3: RTL Logic.

the behavioural simulation the timing diagrams of each input and output can be seen.

Architecture

A. RCA

This is the simplest and easiest way of implementing binary addition where the carry-in to a bit is given by carry-out of previous bit. Each bit produces sum and as well as carry-out, which in turn is given to next bit as carry-in. As each carry bit is getting rippled to next stage, hence the name Ripple-carry adder.

A 4-bit ripple carry adder is shown in Fig. 4.

The realization of this adder is performed by cascading full adders. A 4-bit ripple adder requires 4 full adder blocks; hence n-bit requires n-full adders in series. In the Fig. 4, the trapezoidal block represents each full adder. It can be inferred from the Fig. 4 that from the input (a0, b0) to the sum (s3), represents the critical path. The drawback of this method is that each carry-in has to keep looking for previous full-adder's carry-out. As this is negligible for small bits but has a major time delay as the bit size increases.

One more way to realize the ripple carry adder is to implement using NOR gates. Each full adder requires total of 9 NOR gates for implementation. Therefore, the area for 4-bit ripple carry adder is 36 units and for n-bit it simply is, 9n.

The worst-case propagation delay for sum of m-bit can be written as

T_{sum}=2m+4, where m represents number of bits.

The worst-case propagation delay for carry of m-bits can be written as

T_{carry}=2m+3, where m represents number of bits.

O(n) can be stated as, the delay in propagation for RCA of n-bit.

B. CSA

Due to the propagation delay present in ripple carry adders, it becomes less effectual when the input length increases.

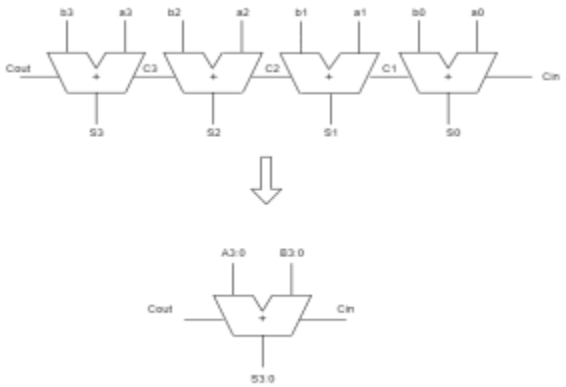

Fig. 4: 4-bit Ripple-Carry Adder.

Each carry-out has to travel through every block of full adder to produce the final carry out. This increases the propagation time in ripple carry adders and hence, are of little use when the input increases. This can be overcome by using CSA. At first RCA circuit calculates carryout and sum for carry-in=0. As, input to the combinational circuit is given by output of the full adder, i.e., the carry-out of the full adder circuit is given as input to the next stage. When this process is completed, then combinational circuit selects final result (both sum and carry) in order to generate the correct output. The increased delay in this modified CSLA without using Multiplexers, when compared to the regular CSLA and modified CSLA using BEC,[9] can be taken as a disadvantage (Fig. 5).

The method implemented in Carry select adders is done with the fact that carry generated at the end of each block is either "1" or "0". The circuit can be duplicated and each of the carry (either "1" or "0") can be given to each full adders. The circuit design using full adders and multiplexers is given in Fig.5. Simply this circuit used two Ripple Carry adder circuits, one having a carry, "1", and another of carry"0".

A 16-bit carry select adder can be seen in Fig.5 where 2×1 multiplexer is used and carry-in from the previous block as the select signal. In the Fig.5 four 4-bit blocks are shown for the carry select adder. Here the full adder block doesn't have to wait until the previous carry-out is generated, as each of the carry can be either "1" or "0", which are generated by ripple carry adders and are multiplexed to give the final carry-out.

The area taken by the setup can be calculated as follows. For n-bit carry select adder, if we consider that size of each fixed block is m-bit, then such p m-bit groups together make n-bit carry select adder. In such a case, we can observe that there are (2n-m) full adders, (n-m) multiplexors and (p-1) AND/OR logic.

As we have already mentioned that each full adder has area of 9 units, hence total area can be calculated as

$$9(2n-m) + 2(p-1) + 4(n-m) = 22n - 13m + 2p - 2.$$

If we consider the Fig.5 where n=16, p=4, m=4 the total area is 306 units whereas for the ripple carry adder of 16-bit, the area is 9×16 is 144 units. We can observe that in terms of area, ripple carry adder is efficient than

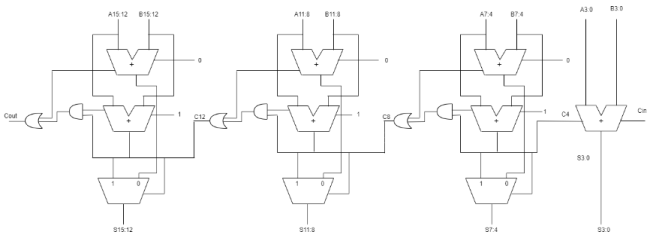

Fig. 5: 16-bit Carry-Select Adder circuit.

carry select adder but in terms of propagation delay, carry select adder is efficient than ripple carry adder, as carry select adder has delay as half of the delay of ripple carry adder, as shown in Table 1.

The propagation delay of carry select adder is O(sqrt(n)).

C. CSKA

This type of adder is used to improve the worst delay of the Ripple Carry adder. This is achieved by cascading several bits of Carry skip adders into blocks. In this, a carry is checked if it will propagate to next block or not, hence this is also called as Carry-Bypass adder.

$$C_{i+1} = G_i + P_i.C_i$$

The carry-out of each block is totally dependent upon the carry-in and propagate signal. If Pi:j=1, then carry-in is allowed to pass through the particular bit, else Gi:j determines the carry-out. With little changes in the Ripple carry adder (i.e., extra logic), the delay can be reduced.

If the central block size is larger than the end block size then further enhancements in reduction of delay can be obtained. When the concatenation schemes are combined with the Conv-CSKA model, this structure is generated. Hence, this is denoted by C-CSKA. The ability to use simpler carry skip logics is provided by this structure. 2:1 Multiplexers are replaced by AOI/OAI compound gates in this structure and when the propagation of carry through the skip logics takes place, we can observe that it becomes complemented.

Lower area, delay and lesser power are seen in the gates with less transistors than 2:1 multiplexer.[18] In general, let us consider dividing the n-bit adder into m k-bit then there are m-2 skip logic blocks and 3 units is the area of each skip block. Hence, we get the total area as 9n+3(m-2). For example, for 16-bit Carry skip adder, n=16, m=4, k=4. The area can be calculated as 9 × 16 + 3 (4-2) = 150 units, which is approximately is same as that of ripple carry adder of 16-bit, as shown in Table 1.

O(sqrt(n)) is the general, delay in propagation of Carry-Skip adders for n-bit.

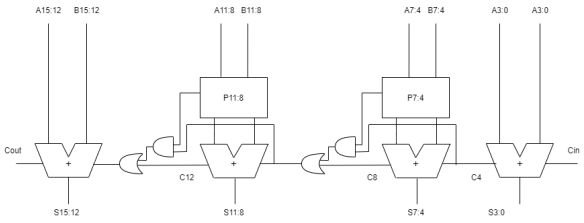

Fig. 6: 16-bit Carry-Skip Adder.

Table 1: Area in units of different adders

Type of Adder	Area	Propagation delay
RCA	144	O(n)
CSA	306	O(sqrt(n))
CSKA	150	O(sqrt(n))

Results

The results obtained to simulation of each of the adders mentioned are given below. Simulated analysis using Vivado for Ripple-Carry adder are given for 16-bit, 32-bit, 64-bit, 128-bit and n-bit are from Fig.7 to Fig.11.

The simulated results using Xilinx for Carry-Select Adder for 8-bit is given in Fig.12.

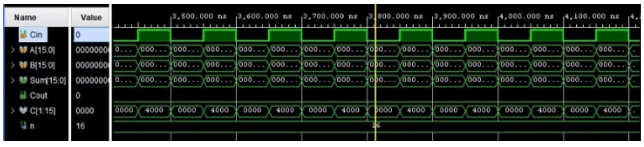

Fig. 7: 16-bit RCA.

Fig. 8: 32-bit RCA.

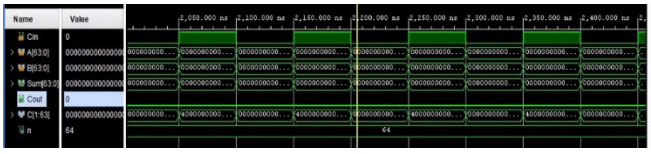

Fig. 9 : 64-bit RCA.

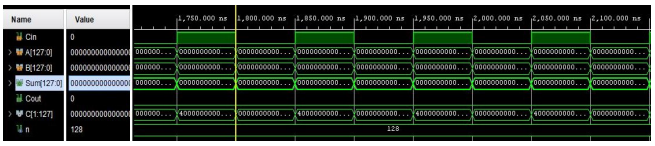

Fig. 10: 128-bit RCA.

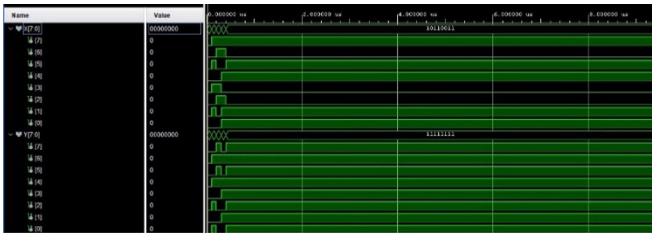

Fig. 11: 8-bit CSKA

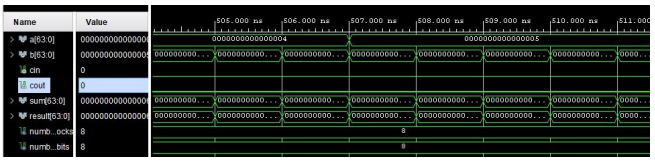

Fig. 12: 64-bit CSKA

The output simulated for Carry-Skip Adder for 64 bit and n-bit are given in Fig.13 and Fig.14, respectively.

Conclusion

The research paper gives an overview of high-speed area efficient adder with its architecture for all the 16 bit, 32 bit, 64 bit and 128 bit adders are implemented using Vivado design suite using VHDL with efficient to all the users with ease of access. Among all the adders namely, Ripple-Carry adder, Carry-Select adder and Carry-Skip adder the Carry-Skip adder performs well as it consumes low power and has better efficiency when compared to other adders. It also consumes less area. The high-speed adders are used for efficient implementation of multipliers and other complex FFT's and DFFT's. The simulated models of above graphs would give one the best start for further research and give over-view of the n-bit Ripple-Carry adder, Carry-Select adders and Carry-Skip adders.

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