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ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic

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Abstract

In recent times, 5G technology is an emerging advancement in the communication system. Because of its improved properties such as bandwidth, speed, connectivity etc., it has various applications in different areas. To acquire these properties in communication systems, the internal architecture for transmission and reception must be advanced. In early generations, irreversible logic gates with CMOS technology were used for FFT (Fast Fourier Transform) implementation, an essential aspect of communication. The primary concern of using irreversible gates is the increased complexity and power consumption. Another concern is heat dissipation due to reduced area of the chip (or chip size), because of which there is some loss of information during transmission. These fundamental causes can be resolved entirely by using reversible logic, which consumes less power, provides high performance and speed, and has low heat dissipation. This paper describes an Application-specific Integrated Circuit (ASIC) implementation of reversible Radix 2 Butterfly (R2B) FFT using reversible logic effectively. Reversible R2B FFT as a whole (i.e., both forward and reverse FFT) utilises reversible adder/ subtractor (both half adder (RH) and full adder (RF)) and reversible multiplier instead of generic combinational circuits. The design procedure is using Xilinx 14.2i for simulation and synthesis of Reversible R2B FFT.

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Introduction

Telecommunication plays a vital role in the advancements of technology. It is one of the core aspects of the evolution of various fields. If there was no further evolution in telecommunication, neither the transmission rate would increase, nor the technologies were advanced. Starting with 1G (where G stands for generation), we came away long to 5G. We are using 4G technology (which uses wireless broadband), and further research will improve 5G to acquire all essential properties.

Fig. 1.1 shows the advancements in each generation, and Fig. 1.2 tells us about the data transmission rate, which is discussed further in detail.

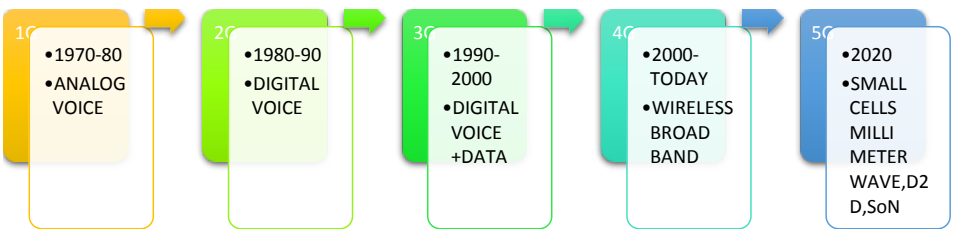

Fig. 1.1: Advancements in technology in each generation

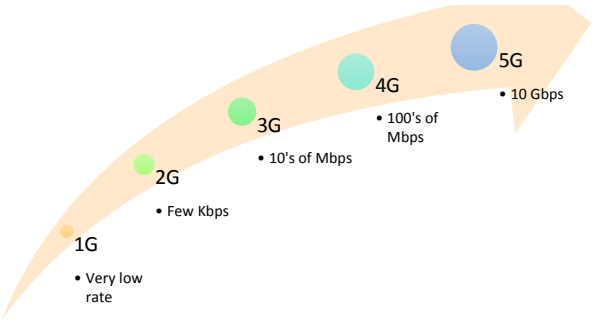

Fig. 1.2: advancement in data transmission rate

At first, there was no such name as 1G. In the early 1970s, Analog voice transmission came into existence with a very low data rate. It was the era of communication models like simplex, half-duplex and duplex later. It was called 1G after the evolution of 2G, i.e., the 2nd generation.

In the early 1980s, 2G came into practice that lasted for a long time. The advancements made in 2G were digital voice communication with crucial features like Global Systems for Mobile Communication (GSM), General Packet Radio Service (GPRS) and Enhanced Data rates for GSM Evolution.

- **GSM:** This allowed data transfer with a data rate of a few kbps (around 30-40 kbps).2G technology with GSM was the time when mobile phones emerged with immense popularity.
- **GPRS:** This was similar to GSM. The additional feature was that it allowed data transfer with a data rate of up to 110kbps.
- **EDGE:** It allowed communication with a high data rate of up to 135 kbps used today in some applications.

In the 1990s, 3rd generation came into play with many advanced techniques and improved data transmission rate. 3G allowed data rate up to 2 Mbps which was a vast increase then. The features included digital voice communication and data and email conversations of significant texts, high-speed browsing of data, uploading videos with more security. 3G used vital elements, namely CDMA and EDGE concepts. CDMA (Code Division Multiple Access) played a significant role in providing a high data transmission rate and healthy connectivity.

To date, we are using the 4th generation in telecommunication which made use of wireless broadband. The key features in 4G were internet protocol (IP), the high data rate of up to 100 Mbps (a vast increase in data rate from 2 Mbps to 100 Mbps). 4G allowed wireless services, mobility, mobile multimedia and customised service for personal use.

5G (5th generation) came into existence in 2020 with its limited features to date. 5G aims to provide higher bandwidth with low power consumption, high-speed transmission, improved connectivity and new IoT (Internet of Things) based applications. The key features to be provided are:

- **Massive MIMO (Multiple-input Multiple-output):** It is a wireless communication system that transmits more information using several transmitters and receivers. MIMO in 5G increased the capacity of antennas which covers greater volume.
- **UDN (Ultra-Dense Networks):** It is the technique used to handle massive traffic in the network. It makes use of small cells to ensure better connectivity and high coverage.
- **D2D (Device-to-Device) connectivity:** As the name itself says, it is a way of direct communication (user to user) without any intervention of base stations
- M2M layer (Machine to Machine): This provides communication between two machines that exchange information in both ways, i.e., wireless or wired.
- **AI applications:** The mobile featured with internal AI features with add additional advantage to 5G (for example, road traffic information and avoiding accidents)
- **Battery:** The lifetime of the battery and speed to charge are improved.

To ensure 5G features, the networks used for communication must be effective. Before FFT, DFT (Discrete Fourier Transform) used in the early days. The samples in discrete format were transmitted using a mathematical equation. It used a more significant number of adders and multipliers. For example, if we consider 2-point DFT, it uses two adders and four multipliers. In generic representation, DFT uses **N(N-1)** adders and $\mathbf{N^2}$ multipliers for N input samples. Because of high complexity (increase in the number of adders and multipliers with the increase in data), FFT is adapted, using $\mathbf{N\log_2 N}$ adders and $\mathbf{(N/2)\ \log_2 N}$ multipliers in its algorithms. FFT plays a vital role in communication systems to ensure better transmission. Fast Fourier Transform is an approach to compute DFT or IDFT (Inverse Discrete Fourier Transform) using butterfly diagrams. We can also implement FFT using Radix-2, Radix-4, Radix-8 approach. The combined approach results in effective results with high efficiency.

Generally, there are two basic algorithms to implement FFT. They are

1. Decimation-in-time (DIT) FFT
2. Decimation-in-frequency (DIF) FFT

Both the algorithms use equal computations (equal number of adders and multipliers). The significant differences between them are

- DIT FFT uses bit reversed order (for example, sample 1 (001 in binary format) is considered the bit reversed order is sample 4 (100)) of input sequence whereas DIF FFT uses generic order
- The output of DIF FFT is bit reversed order while the output is in the general order in DIT FFT

- Considering computations in FFT, additions performed before multiplication in case of DIT FFT and vice versa in DIF FFT

The processor with FFT functionality uses irreversible logic gates (such as AND, OR, NAND, NOR etc.) with CMOS technology to transfer digital data. According to Moore's law, the transistor count doubles every two years in an integrated circuit. The chip size is considered an important criterion that has reduced from 22nm to 7nm (to date). Due to an increase in the number of transistors and reduced chip size, the spacing between transistor reduced. The reduced spacing between the transistors results in various limitations of using irreversible gates in communication for advanced technologies. Some of them are:

1. Increased complexity due to decreased size
2. High power consumption
3. Information loss
4. Heat dissipation
5. Decreased performance (in terms of efficiency, speed when compared to present technology)

Due to advancements in technology, we require an efficient model to meet the need for 5G technology. An Application-Specific Integrated Circuit designed using reversible gates provides an efficient FFT.

Reversible gates are the gates in which the number of inputs equals the number of outputs. The unused outputs terminals in reversible gates are called garbage outputs. Adding additional applications to the processor or chip designed helps us in the reduction of garbage outputs. Reversible computation provides high speed and high density, which adds an advantage to the application. It has zero heat/power dissipation due to reversible operation performed by reversible gates. Zero heat dissipation can be verified using the second law of thermodynamics. The conditions for reversible logic gates are

1. It must be logically reversible (to obtain each other uniquely from inputs and outputs)
2. It must be physically reversible (acquiring inputs from outputs)

In general, Reversible gates have 1x1 mapping of data due to which reconstruction of inputs from outputs is possible and vice versa. Some of the basic reversible gates are the Fredkin gate, Toffoli gate, interaction gate, switch gate, etc. The combinational circuits like adders/subtractors, multipliers, encoders, decoders, multiplexers etc., are designed using these basic gates.

ASIC is typically designing a chip for a specific application that meets the purpose of the designer.

The significant advantage of using ASIC is low power consumption. Unlike a general-purpose integrated circuit, it utilises less area as it is limited to a particular application. Another advantage of ASIC is that the IC is energy efficient. The circuits designed for R2B FFT using reversible logic gates ensured using ASIC implementation as its primary goal is to compute and transfer the information for the given inputs and outputs at a given instance of time.

This paper discusses the in-depth implementation of R2B FFT (Its algorithms, computation, butterfly implementation etc.,), ASIC flow (various steps involved in designing the IC), reversible logic (both reversible adder/subtractor and reversible multiplier), a processor for FFT (for 5G) acquired simulation results and comparison of the proposed model with that of an existing model. We can be further modified using a combined circuit consisting of Radix-2, Radix-4, Radix-8 for much more effective results

Proposed Methodology

R2B FFT

FFT is used to calculate Discrete Fourier Transform (DFT) with a minimum number of computations. The DFT of a given input signal x[n] of length N is

$$X(K) = \quad 0 \leq k \leq N-1$$

Where twiddle factor

Similarly, the Inverse Discrete Fourier Transform (IDFT) is

$$x(n) = (1/N) \quad 0 \leq n \leq N-1$$

FFT uses butterfly diagrams for the computation of smaller results and combines them at the end at various stages. Radix-2 FFT is one of the categories of Cooley-Turkey algorithms. It typically divides N point DFT into N/2 butterflies at each stage until the DFT computation completes (by representing N in terms of 2^x, we get the number of stages (x) in FFT). Fig. 2.1. shows the Radix 2 butterfly diagram of 2-point FFT.

In the proposed model, we use DIT FFT (R2B). DIT algorithm is as follows

Let us consider 8-point input sequence x(n) [N=8]

1. The bit reversed order of x[n] taken as input to the butterfly diagram at stage 1.

(For example, for x [0], the bit reversed order of zero (000) is zero (000), so we consider x [0] as the first sample. Similarly, for x [1], the bit reversed order of 1 (001) is 4 (100), so we consider x [4] as the second sample. In this way, we get bit reversed order of the given sequence)

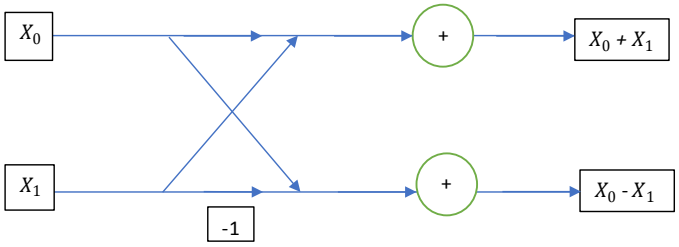

Fig. 2.1: Butterfly diagram of Radix 2 (2-point) FFT

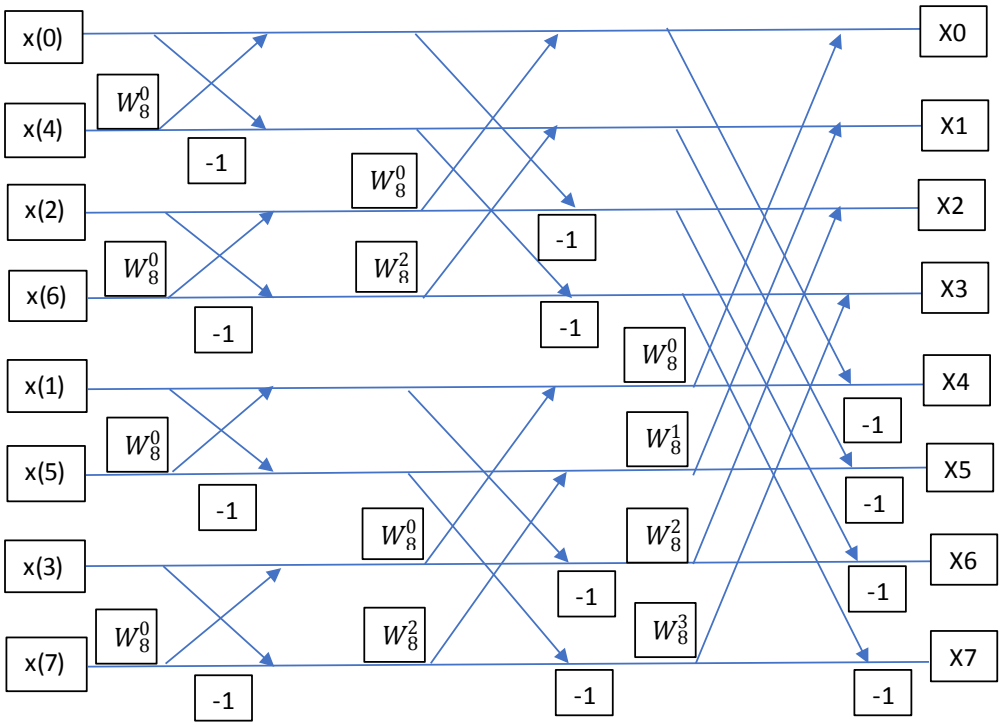

Fig. 2.2: 8-point DIT FFT butterfly diagram

2. In DIT FFT, we first perform addition and then multiply with the twiddle factor () (calculate using twiddle factor formula from 0 to (N/2)-1)
3. At the final stage, we get the required DFT sequence in generic order.

Fig. 2.2 shows 8-point R2B FFT using DIT algorithm where twiddle factors are given by

$$W_8^0 = 1$$

$$W_8^1 = 0.707 - 0.707j$$

$$W_8^2 = -j$$

$$W_8^3 = -0.707 - 0.707j$$

DIT FFT has a significant advantage over DIF FFT since it doesn't need any output reordering. Besides, DIF FFT takes more time for computations when compared to DIT FFT. That is why it is used in various real-time applications like signal processing, image processing, speech processing etc., (Figure 2.2)2

ASIC implementation

ASIC flow is one of the effective procedures to design a chip for a particular application. It has various steps, as shown in Fig. 2.3.

Step-1: Chip specification

Here, the designer specifies all the requirements (like purpose/need, hardware, features, architecture and specific requirements). After this, we proceed with RTL code (to design) and testbench (to verify).

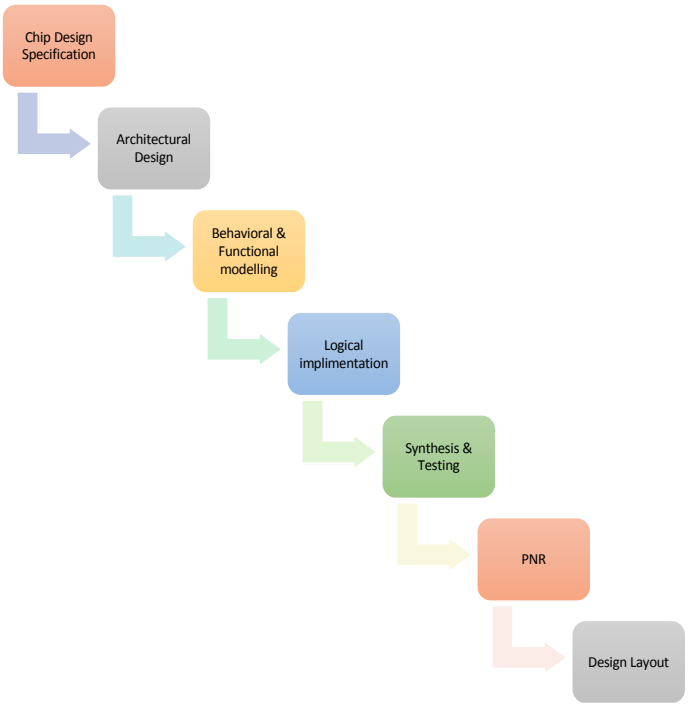

Fig. 2.3: Steps involved in ASIC implementation

Step-2: Architectural design

After knowing the specifications, we divide the tasks into subtasks, or we build functional blocks. The main aim of the architecture is to provide ASIC chip with better performance. All the specifications such as cost, area, time, feasibility, reduction of resources is achieved using better architecture.

Step-3: Behavioural and functional modelling

Functional modelling checks functionality, behaviour and logic at the entry level. The RTL code is written in HDL (Hardware Descriptive Language, in the proposed methodology, we use VHDL (Very High-Speed Integrated Circuit Hardware Descriptive Language)), and the test benches are verified. This comes under behavioural simulation. At this stage, the designer gets to know whether the code is correct or not and whether the requirements are fulfilled or not.

We have two simulation tools, namely functional tools and timing tools. The functional tool verifies logic implementation at entry-level, whereas timing tools checks whether time requirements are met and it is delay-free.

Step-4: Logical implementation

After functional modelling, the designer starts to develop a design model. In this, we create valid representations for the circuit modules and thus carried out using logic domain

Step-5: Synthesis and testing

After the generation of RTL code with test benches, RTL code is converted into gate level. This comes under logical synthesis. If the synthesis meets the time criterion, we proceed with Design for Test (DFT). To obtain high accuracy, we have various techniques to accomplish. They are

- Scan path insertion
- Memory Built-in-Self-Test (BIST)
- Automatic test pattern generator (ATPG)

Step-6: PNR

PNR stands for placement and routing.

In placement, we divide IC into smaller portions and ensure that cells are placed in the correct position with proper spacing. It has four phases, namely pre and post placements, placement and post-placement after and before Clock Tree Synthesis (CTS). CTS is used to reduce errors in time/ delay by providing a clock for all the blocks of the sequential circuit in the design.

Routing deals with the connection of internal blocks like cells, ports, macros with the metal. It has two steps, namely global routing (deals with the estimation of channel congestion) and detailed routing (deals with the connection of each element)

Step-7: Design layout

It is a significant step in the development of the chip. We may use full- customised, semi- customised or programmable ASIC implementations, and each has a different layout. The full-customised layout is more flexible when compared to other layouts. Layout deals with circuit and their interconnections which is generally done using a computer.

Reversible Adder/Subtractor and Reversible Multiplier

Reversible Half (H) adder/subtractor

Reversible half is used to perform both half-adder and half-subtractor operations.

Both Half-adder and Half-subtractor are digital combinational circuits with two inputs and two outputs (basically, 4 I/O terminals). Table-2.1 and Table-2.2 show the truth tables of half adder and half subtractor.

Reversible Half uses single circuitry to perform half adder and half subtractor. The reversible half (A/S) uses reversible logic gates such as reversible AND, reversible OR, reversible XOR/XNOR in the internal architecture. It also uses a multiplexer, resolver and OR gate. Fig.2.4 shows the block diagram of Reversible Half A/S.

Table 2.1: Truth table of half adder

Input1	Input2	Sum	Carry
1	1	0	1
1	0	1	0
0	1	1	0
0	0	0	0

Table 2.2: Truth table of half subtractor

Input1	Input2	Difference	Borrow
1	1	0	0
1	0	1	0
0	1	1	1
0	0	0	0

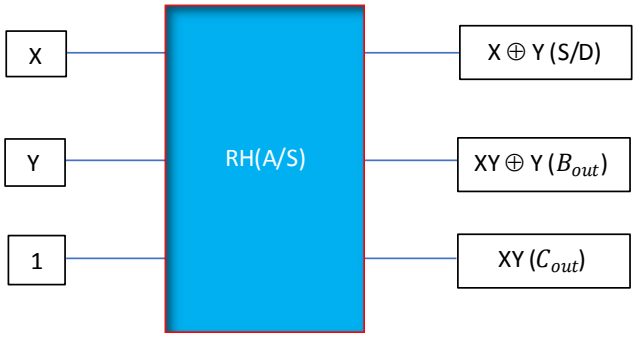

Fig. 2.4: Reversible Half Adder/Subtractor
(Where X - input1, Y - input2, 1 - enable pin)

Reversible Full Adder/subtractor

Reversible Full is used to perform both Full-adder and Full-subtractor operations.

Both Full -adder and Full -subtractor is digital combinational circuits with three inputs and two outputs

(basically, 8 I/O terminals for reversible logic). Table-2.3 and Table-2.4 show the truth tables of the Full adder and Full subtractor. As shown in Fig. 2.5, the Reversible Full Adder/Subtractor is designed using two Reversible Half A/S.

Table-2.3: Truth table of full adder

Input1	Input2	Input3 (Cin)	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table-2.4: Truth table of full subtractor

Input1	Input2	Input3 (B_{in})	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

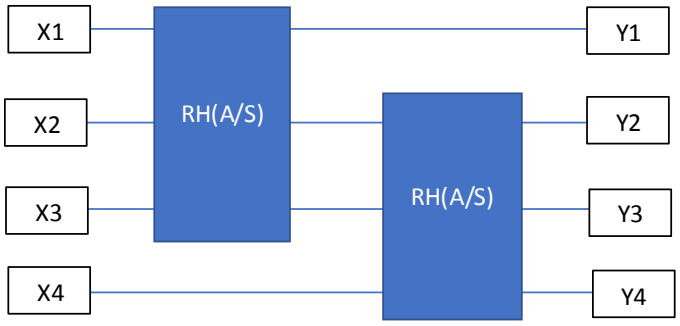

Fig. 2.5: Reversible Full (A/S) using Reversible Half (A/S)

Reversible Multiplier

The reversible multiplier used to perform multiplication with twiddle factor and data. Internally, it multiplies binary data by using reversible adders itself. It has two steps,

1. Computation of partial products.
2. Adding all the partial products

A reversible multiplier circuit consists of a PPG (partial product generator) and a ripple carry adder (in most cases)

Partial product generation

For an nxn reversible multiplier, we require nxn 2-input AND gates. The AND gate operations are performed using reversible logic gates. To reproduce the signal, we use reversible logic gates in the nxn multiplier because we cannot have a fanout for a gate. We can use any reversible logic gates. For example, we can use a combination of Peres gates and Feynman gate to develop a partial product generator, or the use of the same reversible logic gates can serve the purpose.

Summing of partial products

The addition of all partial products can be performed using any adder circuits based on the requirement. Adders using reversible logic gates are used in a reversible multiplier. We use a Reversible Half adder and a Reversible full adder to compute the required products. To design an nxn multiplier, we use n reversible half adders and n^2-2n reversible full adders.

Fig. 2.6 shows the internal circuitry of 2-point DIT FFT using reversible logic.

We use reversible adder and subtractor, reversible multiplier and twiddle factor generator. The primary purpose of the reversible twiddle factor generator is to provide the required twiddle factor to the reversible multiplier circuit. We can use a sine waveform generator which generally produces both real and imaginary part of the twiddle factor with less power consumption and high accuracy. The sine waveform generator can be developed using reversible logic gates, which produce an error during propagation. This error can be minimised using the error compensation table included in the reversible twiddle factor generator.

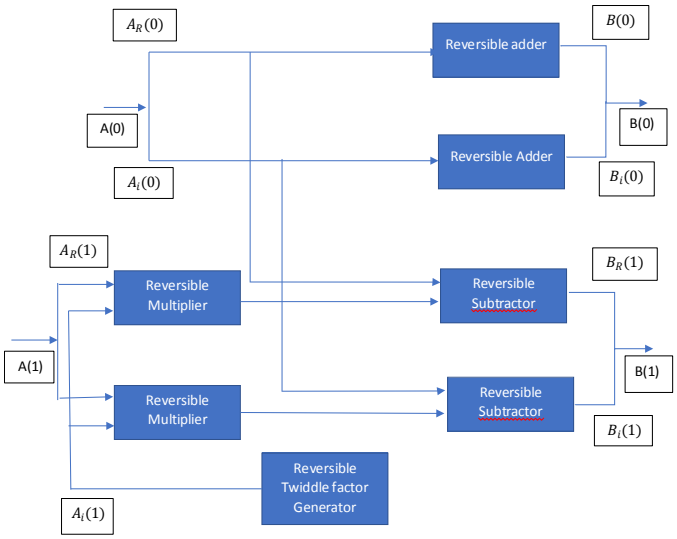

Fig. 2.6: Internal architecture of 2-point DIT FFT algorithm

FFT processor for 5G

FFT is one of the signature algorithms in the OFDM (Orthogonal Frequency Domain Multiplexing) system. we can opt the architecture of FFT as shown in Fig. 2.7. It generally has two 16-bank single port memory blocks with 28-bit data width (14-bit each for both real part and imaginary part), a BFP (Block Floating Point), which is a memory block used to keep the exponential data and a processing element. The processing element has a butterfly unit, a Coordinate Rotation Digital Computer (CORDIC) unit, a scaling unit and an aligning unit. The butterfly unit is the area where we use reversible logic gates in designing FFT. In this area, all the computations are performed. CORDIC unit is used to store information about twiddle factors and is much faster than standard storage. The scaling unit and aligning unit are used to keep the values in place and support the processing element to provide output.

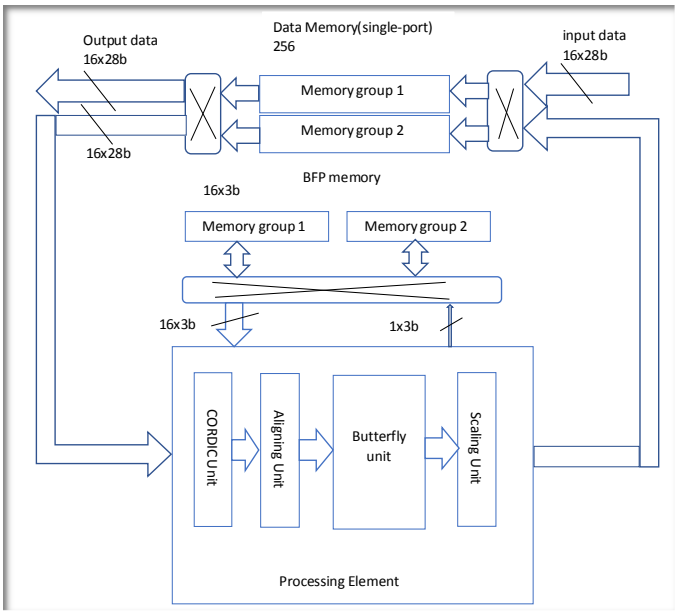

Fig. 2.7: Architecture of FFT processor for 5G technology

Simulation Results

To design the proposed model, we use ASIC implementation, which uses Xilinx and Cadence as primary tools. It has four steps. They are

1. VHDL code
2. Simulation
3. RTL schematic/ synthesis
4. Layout

VHDL implementation of the proposed model

VHDL is a platform used to build codes for digital circuit. The proposed model has a reversible adder/ subtractor block which plays a vital role in designing reversible multiplier and twiddle factor generator.

After the completion of designing the code, we perform a test bench. The executed test bench provides the output required, such as transient response, gate-level schematic etc. It is used to check the behaviour and the correctness of the circuit, which helps further simulation and synthesis.

Simulation results of Reversible Half A/S

The primary purpose of the simulation is to check the timing and delay. It also verifies the behaviour and functionality of the design (proposed model). It is used to show the logical outputs by checking the functionality of the circuit (designed using VHDL code). This helps us to check whether we are getting desired outputs or not.

Fig. 3.1: Shows the Reversible Half Adder/Subtractor simulation result, which is a building block of the overall circuit.

Pin diagram and RTL Schematic/Synthesis

A pin diagram is a block that shows overall inputs and output ports and their mapping. After creating the testbench for the proposed model, we get a pin diagram of the circuit designed. Fig. 3.2 shows the pin diagram of the proposed reversible R2B DIT-FFT for 8-point input.

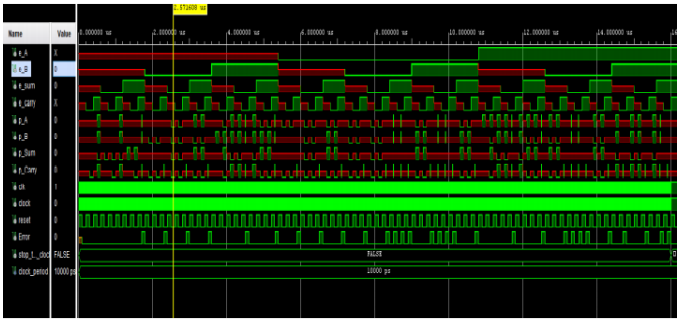

Fig. 3.1: Simulation results of RH A/S

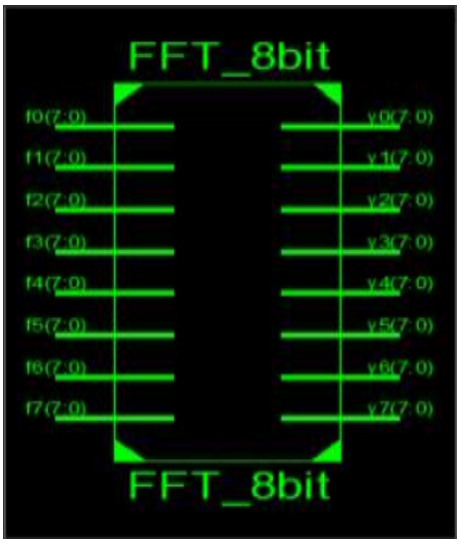

Fig. 3.2: Pin diagram of 8-point reversible R2B DIT-FFT

Register-transfer-level or simply RTL schematic is used to represent/create a high-level circuit. This, in turn, helps us to deduce low-level or desired outputs. It is one of the primary tasks that are carried out in chip designing. It is considered the initial step, an optimised display of all the gates/devices used.

Fig. 3.3 shows the RTL schematic of reversible R2B FFT for 8-point input. It consists of various stages in 8-point DIT-FFT. The first stage has four (N/2) 2-input butterfly diagrams followed by two (N/4) 4-input butterfly diagrams and finally one (N/8) 8-point butterfly diagram. (Here, N is eight as we considered 8-point DIT-FFT).

After completing the synthesis process, we proceed with the layout, usually done in software tools. Layout deals with circuit and their interconnections which is generally done using a computer. The layout is considered a crucial stage before chip manufacturing as the whole circuit is ruined if the connections are not proper. This is considered to be the last step in ASIC implementation, after which fabrication takes place.

Design Summary

As shown in above table 3.1, we used approximately 3% of the total available slice registers, 18% of bonded IOBs (Input Output Blocks). The LUTs (Look Up tables) are used composed of 57 %, of which 14% is slice LUTs, and 43% is fully used LUTs.

In this way, the proposed model further proceeds with layout and then chip manufacturing/ fabrication.

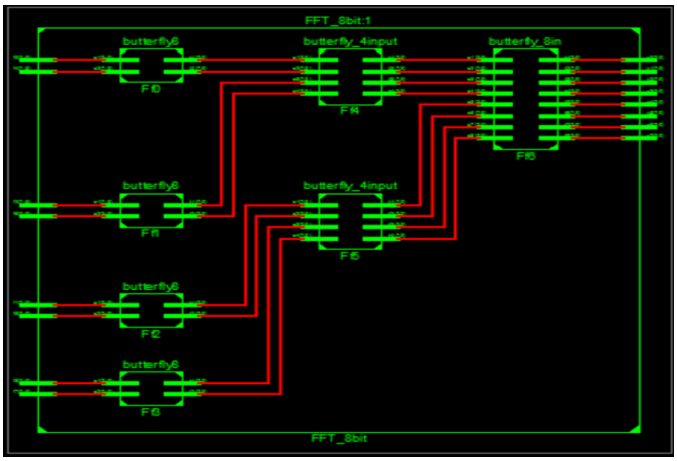

Fig. 3.3: RTL schematic of 8-point reversible R2B DIT-FFT

Table 3.1: Estimation of all the components

Logic utilization	Used	Available	Utilized (approx.)
slice register	3115	92120	3%
slice LUTs	6756	47560	14%
fully used LUTs	3008	6865	43%
bonded IOBs	44	240	18%

Conclusion and Future scope

This paper introduces an Application-specific Integrated Circuit (ASIC) implementation of reversible Radix 2 Butterfly (R2B) FFT using reversible logic for 5G technology. To accomplish this, we used reversible logic gates to form the internal circuitry of R2B FFT. All the combinational circuits like adder/subtractor, multiplier, twiddle factor generator, and the FFT processor used in FFT were developed using reversible logic. With the advancements in technology, the requirement for more efficient and accurate models has increased (in terms of power, weight, area, cost etc.). This criterion is completely fulfilled using the proposed model. It has several improvements when compared to the existing models. In the proposed model, we develop a VHDL code (using Xilinx) which is simulated and synthesised, and after successful synthesis, the layout is created. This practical layout can then go through the fabrication process to develop a chip. The whole proposed work uses ASIC flow. In future 5G technology, the OFDM layer can utilise this proposed model in the physical layer. This has various applications in areas (in biomedical, signal/image processing, telecommunication, quantum computing etc) which brings out an efficient model for advanced technologies.

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