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Realisation of Performance Optimised 32-Bit Vedic Multiplier

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Abstract

This paper demonstrates the improved adaptation of the Vedic Multiplier using the Vedic standards, which includes old sutras. In this paper, current and proposed model are examined. Verilog HDL is utilized to execute the improved adaptation of Vedic Multiplier. Streamlined proposed model can likewise be utilized to achieve higher-request bits duplication exercises up to 32 bits. Vedic Multiplier up to 32-bit, the reproduction results are examined. These outcomes showed that the streamlined Vedic multiplier changed the execution improvement measurements, for example, time delay, also in device use too. Alongside this, a correlation is made among existing and enhanced proposed model to recognize about the presentation improvement measurements.

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Introduction

Indian mathematics will have a name as Vedic mathematics and was brought to light in the early twentieth century. This Vedic mathematics consists of 16 principles which are known as Sutras. "Veda" is known for acquiring the full knowledge and gift of Vedic Mathematics that the Indians delivered to the globe millions of ages ago, and these formulas and principles are now used in engineering technology, including in silicon chips. Vedic mathematics is also implemented to resolve the tangled calculations involved. It is mainly due to the fact that these principles are natural ones, can quickly be learnt and can do complex calculations with ease within a fraction of seconds.

Vedic mathematics can help in the real-life applications in many ways. It is1700 times faster than conventional mathematics. Math fear complexity can be eradicated. Improved performance in results and academics is observed. It increases intelligence and mental agility, sharpens mind as well. Speed and accuracy can also be maintained. Memory is enhanced and boosts the confidence.

Multipliers assume a significant part in the present computerized signal preparing and different applications as shown in the Fig. 1. In high execution frameworks like chip, DSP and so forth expansion and duplication of two double numbers is essential and regularly utilized number juggling activities. Statics shows that over 70% directions in microchip and the vast majority of DSP calculations perform expansion and duplication. In this way, these activity rules the execution time. That is the reason; there is need of high velocity multiplier. The interest of rapid handling has been expanding because of extending PC and sign handling applications.

Multipliers can be divided into hardware and software multipliers. In Ancient systems, no hardware multiplier exists and multiplication was simplified by micro program implementation. The micro program required instruction cycles in order to complete process of multiplication. For high-speed requirement of systems, hardware multipliers are required. In today's micro processors contains arithmetic logic units (ALU) which is a hardware multiplier. Hardware multipliers can be further classified into two categories: parallel and sequential array multipliers. Sequential multiplier comprises a process of continuously summating the shifting and multiplicand. Sequential multiplier has an advantage such as simple circuit and less area. The disadvantage of sequential multiplier is that it is slower.

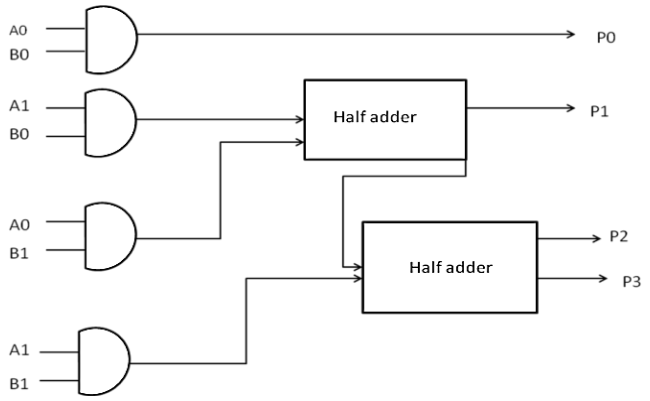

Fig. 1. Basic Multiplier Circuit

Considering parallel array multipliers, the addition of partial products is performed by using a linear adder array. The speed is much faster in parallel than of a sequential multiplier because of parallel operation.

As the Vedic multipliers are considered one among multipliers, they have a vital role in today's wide variety of applications, such as digital signal processing. As technology is advancing, many scholars are targeting the following features to include in multipliers. They are: Low consumption of power, Speed must be high, Layout in regular terms and area must also be less, VLSI implementation.

But Multiplier also includes some of the drawbacks that are needed to overcome. Some of the disadvantages of the multipliers include: Consumption of power is high, Time taken for multiplication process is more, Speed of processing has been less, Components in the multipliers occupy more area.

Literature Review

Vijaya Lakshmi Bandi et al.[1] developed a paper that consists of a modified full adder that has minor delay is used in Vedic Multiplier when compared to the construction of Vedic Multiplier using BED adder. It is synthesized using Xilinx ISE 12.2 software. In this paper, LUT's is reduced by 7.5% when contrasted to the standard Vedic Multiplier. Also, slices reduced by a factor of 6.31 % with respect to standard Vedic Multiplier.

Challa Ram et al.[2] developed a paper that consists of a Binary to Excess Converter, which is used in Vedic Multiplier. Memory utilization is quite less when contrasted with a conventional Vedic multiplier. This paper also describes about array multiplier is compared with Vedic multiplier and the results shows almost similar in terms of power, slice registers, delay, IOBs. It is programmed and simulated in VHDL and Xilinx.

Paras Gulati et al.[3] developed a paper that consists of three various adders are utilized in the Vedic Multiplier. Those are Ripple Carry, Kogge Stone and Modified Carry Select Adders. It is programmed and implemented in Verilog and Xilinx software.

Akila et al.[4] developed a paper that consists of the Vedic Multiplier realizing Modified Adder. To improve the parameters like area, speed, delay, modified Carry Select Adder is used. It is implemented in Xilinx software.

Josmin Thomas et al.[5] developed a paper that consists of various adders such as Carry Select, Ladner Fischer, Brent Kung, Carry Look Ahead, Kogge Stone Adders, and compressor are few that compared. With respect to power and area, Carry Select Adder (CSLA) is far better when contrasted with various other adders. Carry Look Ahead Adder (CLA) is advanced in terms of speed.

M. Antony et al.[6] developed a paper that consists of a multiplexer-based adder and is used for Vedic Multiplier. By using this, results proved better in aspects such as minor delay, more speed. It is programmed in Verilog and synthesized using Xilinx.

Kokila Bharathi et al.[7] developed a paper that consists of a Modified full adder that utilizes multiplexer is implemented in Vedic Multiplier. Results showed much better in terms of low consumption. It is programmed in Verilog HDL.

Bhavani Prasad et al.[8] developed a paper that consists of a Modified Carry Select Adder and is utilized to design the Vedic Multiplier. It proved that the implementation of this Vedic Multiplier is better in aspects of delay, speed, area. Simulation is done by using ModelSim and programmed in Verilog HDL.

Manoranjan et al.[9] developed the paper "Speed Comparison of 16*16 Vedic multiplier", which consists of "Nikhilam" Sutra, Vedic Multiplier is drafted. It is programmed and synthesized in VHDL and Xilinx.

Sreehari et al.[10] developed a paper that consists of new compressor architecture is compared with the existing model architecture. Results showed better outcomes concerning area, speed, power.

Therefore, in this paper, the proposed model does include few improvements to the existing model of the base paper accordingly to achieve higher power efficiency, higher speed and lesser area consumed. Also, the time delay will be reduced comfortably using this improved version of the 32-bit Vedic Multiplier.

Realization of Vedic Multiplier

In order to know about the Vedic multiplier architecture, basic units of architecture include:

Urdhva Tiryagbhyam

Urdhva Tiryagbhyam sutra as shown in Fig. 2. is one of the Sutras in Vedic Mathematics, and it is also known as "Vertically and Crosswise".

Using this sutra, multiplication of two given numbers can be performed. For example, we need to calculate the product of two numbers, 28 and 64. This task becomes simple when this sutra is applied. Firstly, we find the vertical product of the units' digits of the numbers 28 and 64. Its outcome is 32; 2 is fixed at the units' place of the result, whereas 3 is the carry.

We now sum the crosswise products between 28 and 64, i.e., (2x4) + (8x6) = 56. The carry is now added, and it becomes 59. 9 will be fixed at the tens' place, and now they carry 5. Finally, find the vertical product of the tens' digits of the numbers 28 and 64. The value is 12, and when the carry is added, it becomes 17. Keep this number at the hundreds' place. The result thus obtained by this process is equal to 1792. This is how the multiplication of numbers can be performed using this Urdhva Tiryagbhyam sutra.

Half Adder

The Half-Adder is a rudimentary building block for adding two numbers. Here, two inputs, when applied to a half adder, produces two outputs. In half adder, the addent and the augent bits are input states, i.e., X, Y, and carry - 'C' and sum - 'S' are the output states (Fig. 3).

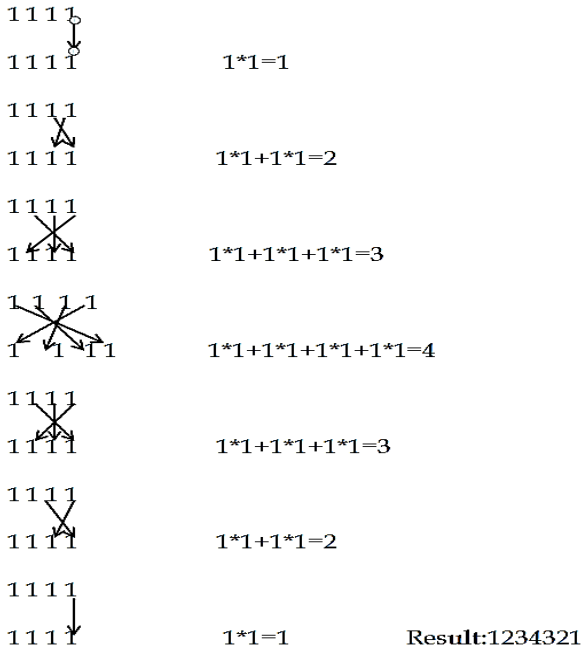

Fig. 2. Urdhva Tiryagbhyam Sutra

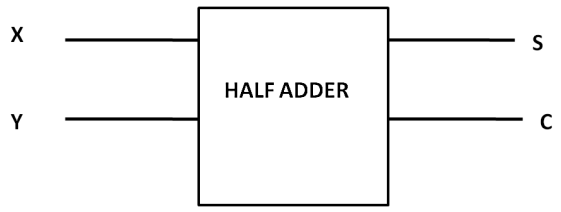

Fig. 3. Half Adder

S = X XOR Y
C = X AND Y

Full Adder

The two half adders with or gate combine to form a full adder. A full adder adds three numbers. These three numbers are 1 bit in size. Inputs are X,Y and consider Z is the Carry input. Sum – 'S' and Carry - 'C' are the outputs (Fig. 4).

S = (X XOR Y) XOR Z
C = X AND Y OR Z(X XOR Y)

2-Bit Binary Multiplier

A multiplier of binary in size is used in electronics and computers in order to calculate the product of any two numbers. Half adder modules of 2 in number are required to realize a binary multiplier [11]. It is used to implement to multiply two binary numbers. The below diagram explains for a 2-bit multiplier where X0-X1, Y0-Y1 are the inputs and, when they are multiplied, gives the output of S0S1S2S3.

X1 X0
X Y1 Y0

X0Y1 X0Y0
X1Y1 X1Y0 x

S3 S2 S1 S0

$S0 = X0*Y0$ (1)

$S1 = X0*Y1 \ \ XOR \ \ X1*Y0$ (2)

$S2 = X1*Y1 \ \ XOR \ \ (X0*Y1)*(X1*Y0)$ (3)

$S3 = X1*Y1 \ \ AND \ \ (X0*Y1)*(X1*Y0)$ (4)

The model of a 2x2 Binary Multiplier is as shown here in the Fig. 5.

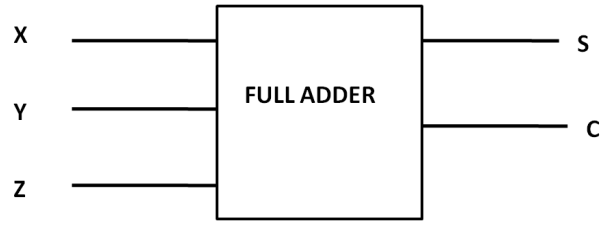

Fig. 4. Full Adder

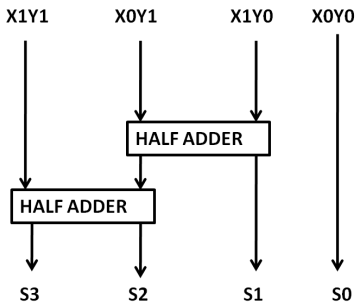

Fig. 5: 2x2 Multiplier

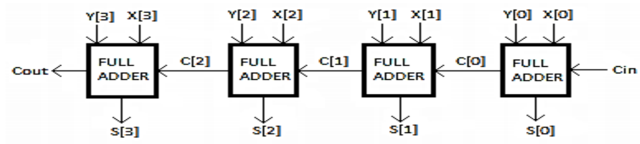

Fig. 6. Ripple Carry Adder

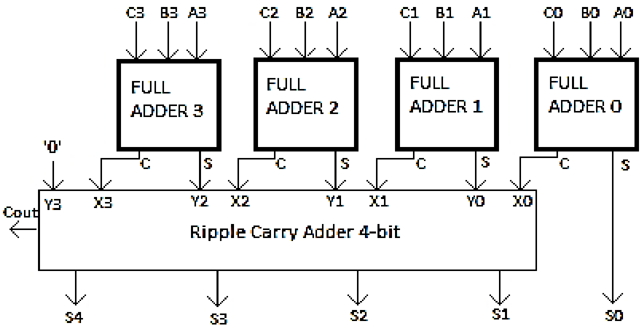

Fig. 7. Carry-Save Adder

Ripple Carry Adder (RCA)

In the Binary Multiplier, Full Adders are used to provide the output of the n-bit binary pattern by implementing an addition operation on it.[11] The carry output of one Full Adder is the input to the subsequent stage, Full Adder and this prescribed above process repeats until it reaches the ending stage.[12]

Below, the Fig. 6. shows the 4-Bit Ripple Carry Adder structure.

Carry Save Adder (CSA)

In the Bi nary Multiplier, Carry-Save Adder (CSA) is quite frequently and a highly used adder circuit in the implementation of high-speed arithmetical calculations of register-transmit pitch design in the electronics field. A carry-save adder comprises of full adders. N-bit CSA consists of N number of full adders (FAs) which are disjoint where each full adder gives the output of a sum and carry bit depending up on the corresponding inputs. CSA has three N-bit inputs and results in two outputs. Big Adders can be implemented using CSA as its operation is much faster than the typical conventional adders.

$$SUM = (A+B+C) \text{ Mod } 2 \quad (5)$$

$$CARRY = ((A+B+C)-SUM)/2 \quad (6)$$

The model of a 4-Bit Carry-Save Adder is as shown here in the Fig. 7.

Existing and Proposed Works

Existing Vedic Multiplier

The Vedic Multiplier is constructed using the concept of Vedic Mathematics which was written and developed by Bharati Krishna Tirtha, first published in 1965. By using this technique, the speed and efficiency increases, and the circuit consume fewer hardware elements. There are approximately 16 sutras and 13 sub-sutras in Vedic Mathematics book.

In both Existing and Proposed model of Vedic Multiplier, "Urdhva Tiryagbhyam" sutra, which is defined as "Vertical as well as Crosswise" is used. In the Existing Model, two Carry-Save Adders replace the parallel Ripple Carry Adders for better speed and efficiency. Two 4-bit inputs X(X3,X2,X1,X0), Y(Y3,Y2,Y1,Y0) and an 8-bit output Z(Z7,Z6,Z5,Z4,Z3,Z2,Z1,Z0),are the information processors using the Vedic Multiplication methodology.

X3 X2 X1 X0
x Y3 Y2 Y1Y0

(X3X2) x (Y1Y0)
(X1X0) x (Y1Y0)
(X3X2) x (Y3Y2) (X1X0) x (Y3Y2)

Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0

A 2-bit multiplier is utilized to compute the half way point responses, and 4 bits is the output.

(X3X2)(Y3Y2) utilizing 2-bit Multiplier produces output: Z33Z32Z31Z30

(X3X2)(Y1Y0) utilizing 2-bit Multiplier produces output: Z23 Z22Z21Z20

(X1X0)(Y3Y2) utilizing 2-bit Multiplier produces output: Z13Z12Z11Z10

(X1X0)(Y1Y0) utilizing 2-bit Multiplier produces output: Z03Z02Z01Z00

The 4-bit CSA is utilized to summate these 4-bit inputs: Z23 Z22 Z21 Z20, Z13 Z12 Z11 Z10 and Z31 Z30 Z03 Z02. Thus, the Vedic Multiplier is designed. The final two Most Significant Bits of the CSA results are the inputs to the OR logical gate. Additionally, final instant 4-bit RCA is restored by the logical 2-bit adder block through which the resultant output of the logical OR gate can be managed easily. One of the inputs to the final instant 2-bit adder is obtained by the result of the OR gate. Correspondingly, a 4-bit RCA logical circuit is a should for the 8-bit Vedic Multiplication prototype model and going so on, the 32-bit Vedic Multiplier is designed as shown here in the Fig. 8.

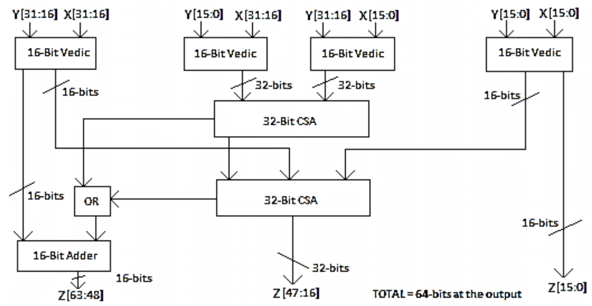

Fig. 8. Existing 32-Bit Vedic Multiplier

Proposed Model of the Improved Vedic Multiplier

In this Presented Paper, we have modified and improved a newer version of the 32-bit Vedic Multiplier, which runs with high speed and efficiency, consumes lesser area, and the time delay is also diminished significantly when differentiated from the Existing Model. This model is also built around the concept of the CSA circuit. Fewer modifications and improvements have been made to the Existing Model of 32-bit Vedic Multiplier for overall better performance, and this new model has been proposed.

Firstly, the 2x2 Binary Multipliers are built using two Half Adders. For one 2x2 Binary Multiplier, 2-bit inputs X(X1-X0), Y(Y1-Y0) and output Z(Z3-Z0) of 4-bit are the information processors which perform the Vedic Multiplication. Likewise, we have created four 2-bit Multipliers. Their multiplication process will be performed using the Carry-Save Adder, which can efficiently compute the sum of three or more binary numbers with high efficiency. The third input is assumed as Cin and the output as Cout. Now, we will design a 4x4 or 4-Bit Vedic Multiplier using the 2x2 Binary Multipliers and CSA.

The improved model of 4-Bit Vedic Multiplier is as shown here in the Fig.9.

Likewise, from the 4-Bit Vedic Multiplier, we will be designing each of the following higher stages of the Multipliers. Utilizing the 4-Bit Multipliers, the 8-Bit Multiplier is developed. Utilizing the 8-Bit Multipliers, the 16-Bit Multiplier is then developed.[13] Finally, utilizing these 16-Bit Multipliers, we have designed the proposed model and improved version of the fast 32-Bit Vedic Multiplier.

The inputs X(X31-X0), Y(Y31-Y0), 32-Bit Carry-Save Adder and the 16-Bit Adder are used[14]as the I/O components in the design of the block model of this improved 32-Bit Vedic Multiplier. Fig. 10. below shows the architecture of the 32-Bit Improved Multiplier.

Methodology

Firstly, the existing version of the 4-bit Vedic Multiplier is nicely designed. Correspondingly, the scale of the Vedic Multiplier is expanded until 32 bits, i.e., 8-bit, 16-bit and then finally 32-bit utilizing the CSA. By utilizing the Binary Multipliers and the CSA again, the improved version of the 4-bit Vedic Multiplier model is implemented. Similarly, this improved Vedic Multiplier range is expanded until 32bits, i.e., 8-bit, 16-bit and 32-bit. Using Verilog HDL, the functionality is designed and synthesized, analyzed using the ModelSim Software, and then the ultimate Synthesis is done by utilizing the XILINX ISE Design Suite.

Experimental Results and Simulation

Simulation Results

The Xilinx ISE Simulator Tool is utilized for the execution of the proposed model for which the test bench is also being programmed using Xilinx tool. The Verilog HDL codes for all the circuit components – 2x2 Multiplier, RCA n-bit, CSA n-bit, 4x4, 8x8, 16x16 and finally, the proposed 32-bit Vedic Multiplier is written and compiled successfully. Then, we have used the ModelSim Software for obtaining the Simulation Results of the different components. Finally, the following synthesis process is performed with Xilinx synthesis tool until 32-bit operations.

The timing waveforms conclude all the possible input and output data bits. The waveforms of Simulation

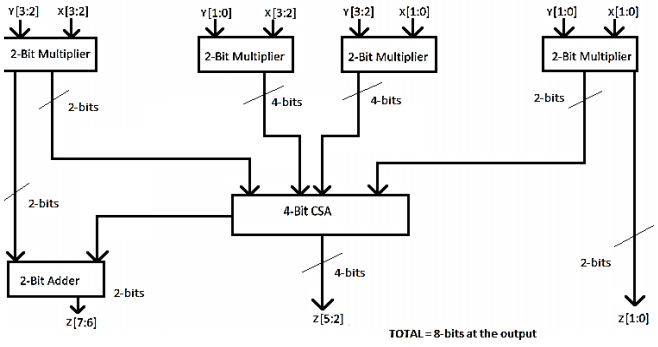

Fig. 9: Improved 4-Bit Vedic Multiplier Model

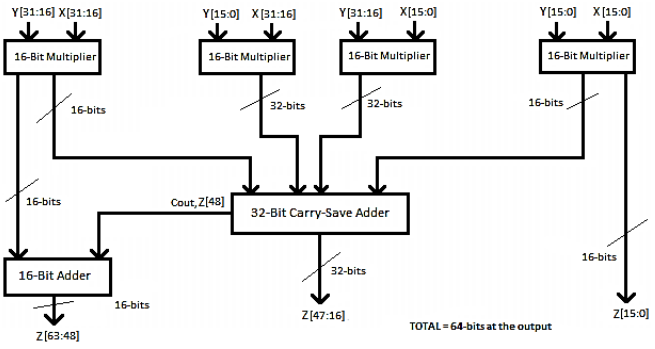

Fig. 10. Improved 32-Bit High-Speed Vedic Multiplier

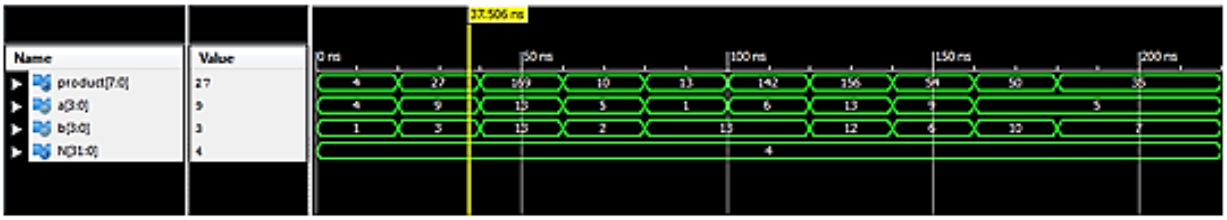

Fig. 11. 4x4 Vedic Multiplier Simulation Outcomes

Outcomes for 4x4 Multiplier are presented in Fig. 11. whereas for 32x32 Proposed Vedic Multiplier, its Simulation Outcome waveforms are illustrated in Fig. 12. Table 2 and Table 3 below displays the obtained values of delay and total no. of consumed LUTs for the respective existing model and the proposed model of our 32x32 Vedic Multiplier.

From the Fig.11., it can be observed how the number of LUTs are allotted, used and using the synthesis results, the information regarding the number of Slice LUTs available and used, the number of the fully used LUT-FF pairs and the total number of the Bonded IOBS used or available for a 4x4 Multiplier are obtained successfully from these Simulation and Synthesis Results. Hence, the time delay for a 4x4 is also gathered successfully by the implementation of the Timing Summaries or Diagrams.

From the Fig.12., it can be observed how the number of LUTs are allotted, used and using the synthesis results, the information regarding the number of Slice LUTs available and used, the numbers of the fully used LUT-FF pairs and the total number of the Bonded IOBS used or available for a 32x32 Multiplier are obtained successfully from these Simulation and Synthesis Results. Hence, the time delay for a 32x32 is also gathered successfully by the implementation of the Timing Summaries or Diagrams.

Comparison of Literature Survey Parameters

Hence, when analyzing each of these literature survey models shown in the Table 1, each model has its own limitations. One of the models has a higher time delay, one has higher number of LUTs, another one has lesser speed

Fig. 12. 32x32 Vedic Multiplier Simulation Outcomes

Table 1: Comparison of Literature Survey Parameters

S.No.	*Title of Paper*	*Author*	*Parameters*	*Limitations*
1	Performance Analysis for the Vedic Multiplier Using the Modified Full Adders	Vijaya Lakshmi et al.	**Delay:** 39.74ns. for 16-bit **LUTs:** 198 for 8-bit	The Time Delay is on a bit higher side when compared to the other models
2	Area Efficient Modified Vedic Multiplier	Challa Ram et al.	**Delay:** 38.82ns. for 16-bit **LUTs:** 1243 for 16-bit	The number of LUTs are on the higher side when compared to the other models
3	Implementation of an efficient Multiplier Using the Vedic Multiplication Algorithms	Paras Gulati et al.	**Delay:** 23.367ns. for 16-bit **LUTs:** 978 for 16-bit	Power Consumption is quite high in this model when compared to other models
4	Comparative Study of Performance Vedic Multiplier on the Basis of Adders Used	Josmin Thomas et al.	**Delay:** 28.644ns. for 16-bit **Slice LUTs:** 93 slices	Consumption of Area or Memory is high in this model when compared to the other models
5	Design of High-Speed Vedic Multiplier Using the Multiplexer Based Adder	Saji. M. Antony et al.	**Delay:** 16.994ns. for 16-bit **LUTs:** 594 for 16-bit	Speed Efficiency is low and Percentage Improvement in Speed is very less when compared to other models

S.No.	Title of Paper	Author	Parameters	Limitations
6	Design of Low Power and High-Speed Modified Carry Select Adder for 16-bit Vedic Multiplier	Bhavani Prasad et al.	**Delay:** 1.6ns. for 8-bit **LUTs:** 231 for 8-bit	Circuit is quite expensive and complex for imple-mentation physically when compared to the other models

and some other models have higher area consumption, complexity, fragility, etc. Thus, to counter all these drawbacks and address all these concerns, a performance optimized realization of 32-bit Vedic Multiplier is designed and implemented. The proposed model showed very promising results in all the parameters. The only drawback of the proposed model is a hike in area occurs at certain point of time which increase the no. of slice LUTs.

Comparison of Existing Model with Proposed Model

Table 2: Existing Vedic Multiplier's Parameters

S.NO	EXISITNG VEDIC MULTIPLIER	DELAY	LUT'S
1	4-bit	14.215	38
2	8-bit	24.186	201
3	16-bit	43.714	903
4	32-bit	68.859	3802

Table 3: Proposed Vedic Multiplier's Parameters

S.NO	IMPROVED VEDIC MULTIPLIER	DELAY(in ns)	LUT'S
1	4-bit	3.873	24
2	8-bit	6.205	124
3	16-bit	9.735	554
4	32-bit	16.195	2346

From all these three tables, Table 1, Table 2and Table 3, the time delay (in ns.) and the number of LUTS for all the 4x4 Multiplier, 8x8 Multiplier, 16x16 Multiplier, 32x32 Vedic Multiplier are computed and tabulated successfully as shown above for the different literature survey models, previous existing model of the Vedic Multiplier and the newly implemented and proposed model of the Improved Vedic Multiplier.

Conclusion and Future Scope

Conclusion

This research article discusses the existing standard Vedic Multiplier design constraints and limitations, and in order to overcome its drawbacks, a new Vedic multiplier prototype is proposed and realized. This proposed and developed method is much more efficient with respect to the time delay than all the existing methods. Higher Speed, Simpler algorithm, power efficiency, increased throughput, area usage and decrease in size are some of the significant gains of this proposed model. This enhanced architecture model is used to accelerate and improve the multiplication among the various existing models.

Future Scope

Vedic multiplier using one CSA rather than two CSA is a major contribution to VLSI industry.

As Moore's law states that the count of transistors doubles about every two years. Also, the speed and capacity for computing increases with count of transistor, Vedic multiplier with one CSA can decrease delay, Consumption of power, Area, increase in speed. With these results, one can save cost, time, and energy. It is very much can be replaced with Vedic multiplier of two CSA in the coming days.

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