ISSN:2582-1458
https://doi.org/10.31838/jvcs/03.01.05

Research Article

Design and performance Analysis of XOR and XNOR Functions at Low VDD Using 130nm Technology

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Received: 06.07.21, Revised: 12.08.21, Accepted: 18.09.21

ABSTRACT

In this presented work we designed CMOS exclusive-OR/ exclusive-NOR gates with the increase in performance than the existing method. The main aim of our project is to reduce the power and increase the performance. Two new methods are proposed to implement the exclusive-OR and exclusive- NOR functions on the transistor level. The first method which consists of CMOS Based exclusive- OR/ exclusive-NOR design. In this method we have less power dissipation and delay which leads to less PDP value. The other one is combined exclusive-OR/ exclusive-NOR design which improves the performance of the prior method. It uses the same number of transistors as but with more driving capability additionally. Simulations are verified through 130nm mentor graphics tool.

Keywords: CMOS, power delay product (PDP), exclusive-OR, exclusive-NOR, mentor graphics tool.

Introduction

Complementary metal-oxide-semiconductor (CMOS), is a type metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions. CMOS technology is used for constructing integrated circuit chips, including microprocessors, microcontrollers, memory chips and other digital logic circuits. CMOS technology is also used for analog circuits such as image sensors, data convertors, RF circuits, and highly integrated transceivers for many types of communication.

Mohamed M. Atalla invented the MOSFET at Bell Labs in 1959, and then demonstrated the PMOS and NMOS fabrication processes in 1960. These processes were later combined and adapted into the complementary MOS process in 1963. RCA commercialized the technology with the trademark "COS-MOS" in the late 1960s, forcing other manufacturers to find another name, leading to "CMOS" becoming the standard name for the technology by the early 1970s. CMOS eventually overtook NMOS as the dominant MOSFET fabrication process for very large-scale integration (VLSI) chips in the 1980s, while also replacing earlier transistor–transistor logic (TTL) technology. CMOS has since remained the standard fabrication process for MOSFET semiconductor devices in VLSI chips. As of 2011, 99% of IC chips, including most digital, Analog and mixed-signal ICs, are fabricated using CMOS technology. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, like NMOS logic or transistor–transistor logic (TTL), which normally have some standing current even when not changing state. These characteristics allow CMOS to integrate a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most widely used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of MOS field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nano meter node and smaller sizes.

XOR gate (sometimes EOR, or EXOR and pronounced as Exclusive OR) is a digital logic gate that gives a true (1 or HIGH) output when the number of true inputs is odd. An XOR gate implements an exclusive or () from mathematical logic; that is, a true output results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) or both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs

are not alike otherwise the output is false. A way to remember XOR is "must have one or the other but not both".

The XNOR gate (sometimes ENOR, EXNOR or NXOR and pronounced as Exclusive NOR) is a digital logic gate whose function is the logical complement of the Exclusive OR (XOR) gate. It is equivalent to the logical connective () from mathematical logic, also known as the material biconditional. The two-input version implements logical equality, behaving according to the truth table to the right, and hence the gate is sometimes called an "equivalence gate". A high output (1) results if both of the inputs to the gate are the same. If one but not both inputs are high (1), a low output (0) results.

Existed Invertor Based Xor/Xnor Gate

Based on the inverter configuration, we can arrange two inverters appropriately for the XOR function as well as the XNOR structure. The layout is sketched in Fig. 3. Analysis of these two cases for the input signals A and B, the output of the second inverter is XOR function. For the structure stated in Fig. 3(a), when A = "HI," 'A' must be "LO." A and A' signals are connected to the VDD end of PMOS and the VSS end of NMOS in the second inverter, respectively. Then the output of the second inverter functions are like a standard inverter, and outputs the signal B'. Therefore, the output signal will be a perfect AB' signal. On the other hand, when A = "LO", 'A' must be "HI." The output of the second inverter will be a poor signal B because it transmits a signal "HI" by NMOS and a signal "LO' by PMOS. That is, if we use only 4 transistors to implement an XOR function, based on the inverter configuration, its output will be complete on AB' but poor on A'B.

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Software Used (Mentor Graphics)

Mentor Graphics is a US-based electronic design automation (EDA) multinational corporation for electrical engineering and electronics, headquartered in Wilsonville, Oregon. Founded in 1981, the company was acquired by Siemens in 2017 and is now known as Siemens EDA.

Mentor Graphics was noted for distributing products that assist in electronic design automation, simulation tools for analog mixed-signal design, VPN solutions, and fluid dynamics and heat transfer tools. The company leveraged Apollo Computer workstations to differentiate itself within the CAE market with its software and hardware.

Mentor Graphics was founded in 1981 by Tom Bruggere, Gerry Langeler and Dave Moffenbeier. The first round of money, worth $1 million, came from Sutter Hill, Greylock, and Venrock Associates. The next round was $2 million from five venture capital firms, and in April 1983 a third round raised an additional $7 million. Mentor Graphics was one of the first companies to attract venture capital to Oregon.

Apollo Computer workstations were chosen as the initial hardware platform. Based in Chelmsford, Apollo was less than a year old and had only announced itself to the public a few weeks prior to when the founders of Mentor Graphics began their initial meetings.

When Mentor entered the CAE market the company had two technical differentiators: the first was the software - Mentor, Valid, and Daisy each had software with different strengths and weaknesses. The second, was the hardware - Mentor ran all programs on the Apollo workstation, while Daisy and Valid each built their own hardware. By the late 1980s, all EDA companies abandoned proprietary hardware in favor of workstations manufactured by companies such as Apollo and Sun Microsystems.

After a frenzied development, the IDEA 1000 product was introduced at the 1982 Design Automation Conference, though in a suite and not on the floor.

Proposed Cmos Based Xor/Xnor Gate:

Based on the CMOS gate theory, the realized circuit using CMOS is shown in Fig. 4.1. This structure needs only 4 transistors, driving capability is more compared to existing method. In general, if the output signal of a circuit comes from VDD or V& directly, we say this circuit has driving capability. It is well known that a transmission gate has no driving capability. If the circuit output will drive other circuits, it does better to cascade a canonical CMOS buffer to do so.

For example, if a function f (0) is implemented by CMOS, then one can resemble the structure for implementing the complementary output f (0)' and attach a tailing inverter. If one uses the proposed

methods of 4-transistor to drive canonical CMOS circuits, it can still work correctly. When the output levels of both 4-transistor cases are poor, an added tailing inverter can improve this defect, and the driving capability is present. Using this technique, it also has the configurations of XOR and XNOR in the below Fig.

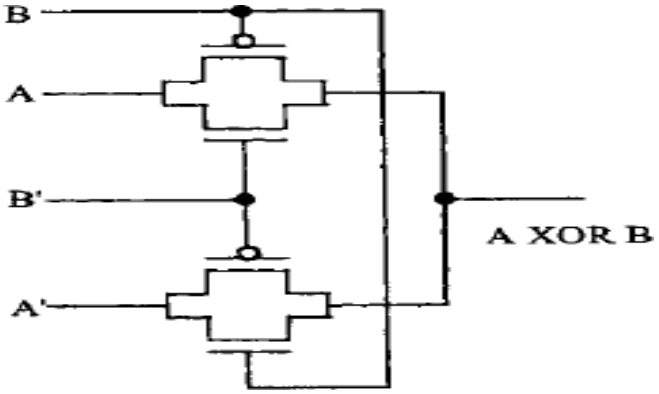

Fig.1: Proposed CMOS Based XOR Gate

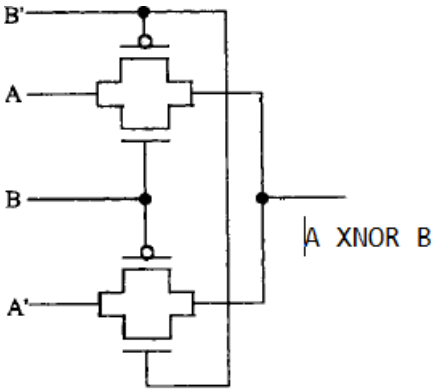

Fig.2: Proposed CMOS Based XNOR Gate

Simulation Results

In this, comparative analysis of Existed Invertor based XOR gate and XNOR gate with proposed CMOS based XOR and XNOR gate has increased performance and decrease of power delay product(PDP). In the other the combination of XOR and XNOR of existed and proposed was varied in its performance. The simulation circuit and their respective wave forms for each operation is shown as below

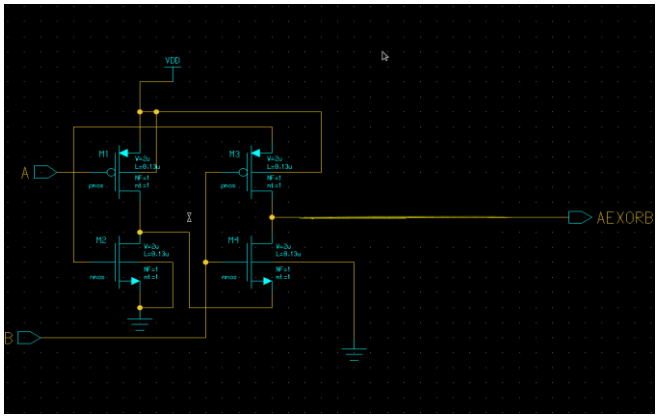

Fig.3: Schematic circuit of Existed Invertor XOR Gate

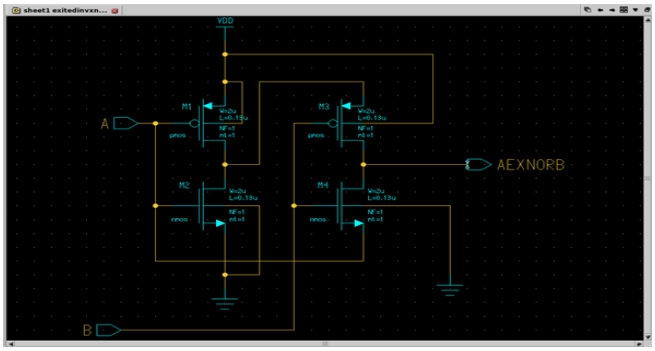

Fig.4: Schematic circuit of Existed Invertor XNOR Gate

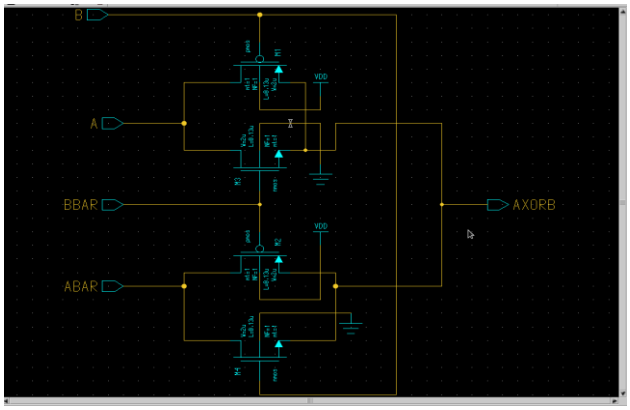

Fig.5: Schematic circuit of Proposed CMOS Based XOR Gate

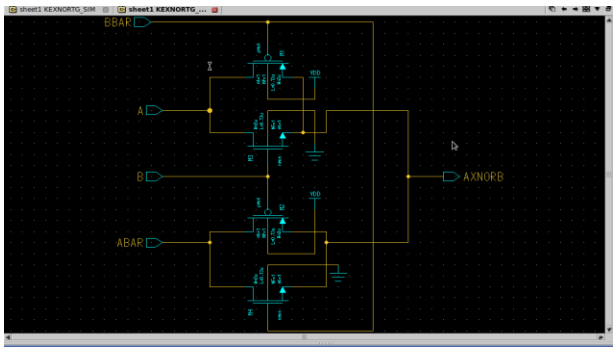

Fig.6: Schematic circuit of Proposed CMOS Based XNOR Gate

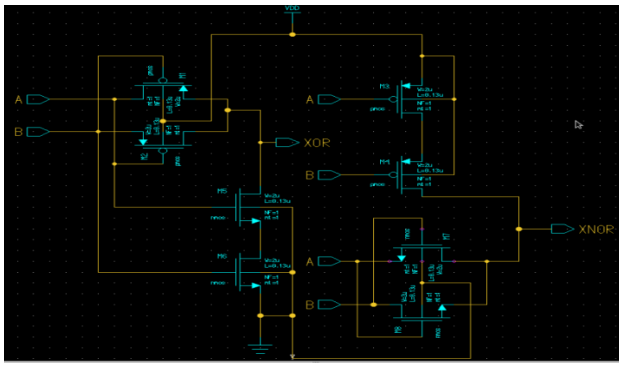

Fig.7: Schematic circuit of Existed XOR – XNOR combined Design

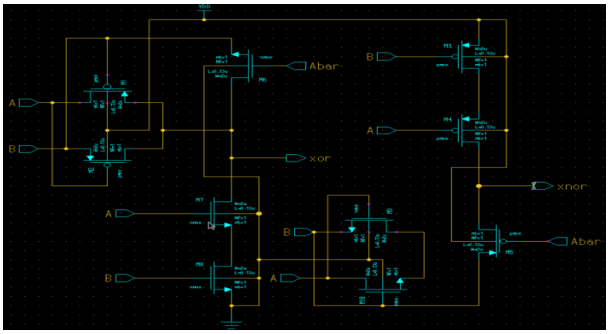

Fig.8: Schematic circuit of Proposed XOR – XNOR combined Design

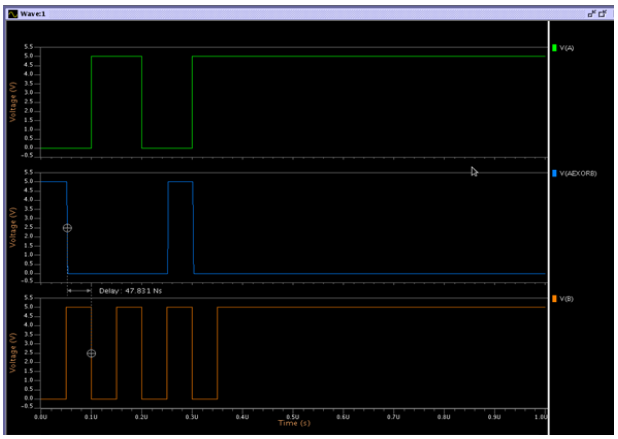

Fig.9: Simulation circuit of Existed Invertor XOR Gate

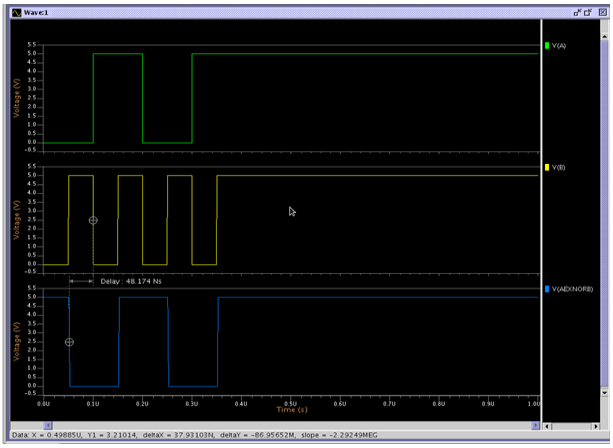

Fig.10: Simulation circuit of Existed Invertor XNOR Gate

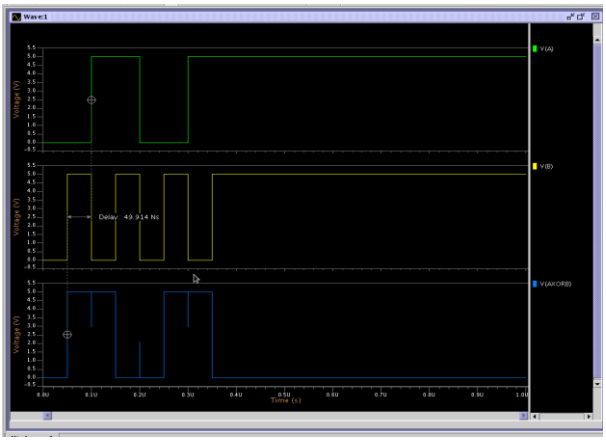

Fig.11: Simulation circuit of Proposed CMOS Based XOR Gate

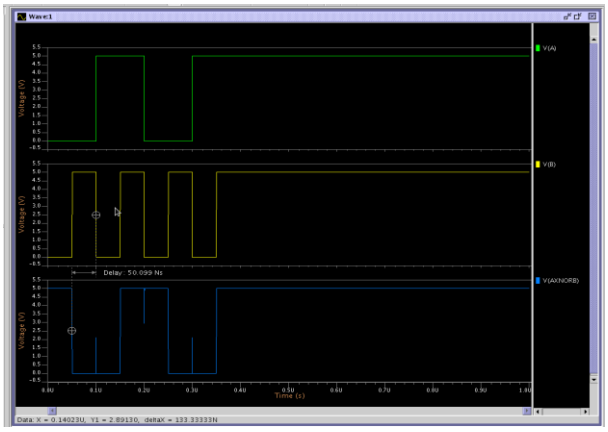

Fig.12: Simulation circuit of Proposed CMOS Based XNOR Gate

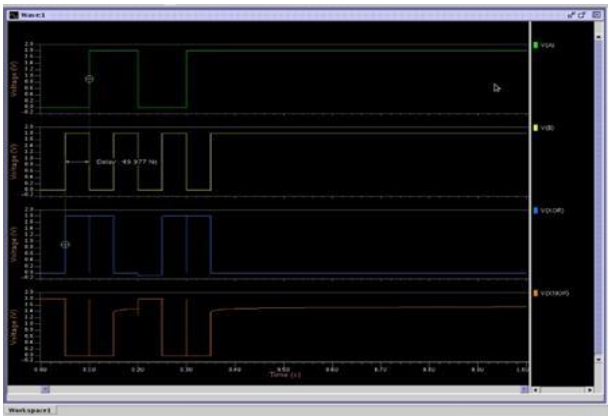

Fig.13: Simulation Circuit Of Existed XOR-XNOR combined Design

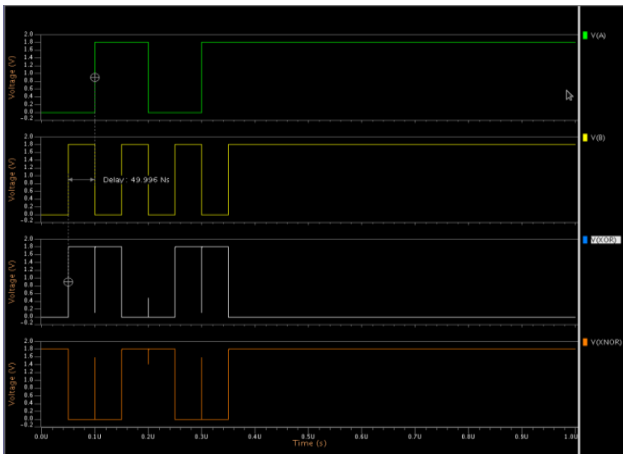

Fig.14: Simulation Circuit Of Proposed XOR-XNOR combined Design

Table 1: Simulation Outcomes of Existed and Proposed methods

S. No	Design	Delay (nS)	Power (nW)	PDP (fJ)
1	Existed XOR	47.831	220.4	10.541
2	Existed XNOR	48.174	152	7.3224
3	Proposed XOR	49.914	97.5121	4.8672
4	Proposed XNOR	50.099	97.5121	4.8852
5	Existed XOR-XNOR combined	49.99	4.856	0.242
6	Proposed XOR-XNOR	49.79	0.827	0.041

Conclusion

In this project, we proposed new configurations of CMOS designs for the exclusive- OR and exclusive-NOR functions. We have designed exclusive-OR in which proposed method has increased performance than the existed one. The Power dissipation and the delay was decreased in the proposed method than the existing method. The other method which states that the combined exclusive-OR and exclusive-NOR was designed. In this method, Proposed method has less PDP value compared to the existed method of the combined and normal methods. Here, we can say that 20% of the PDP value was reduced from the existing method which improves more performance of the circuit. The simulation results are based on 130-nm CMOS technology model, which indicate that the proposed design has high speed and low power over the existed design.

References

1. Sadulla Shaik, "Device-Circuit Interaction and Performance Benchmarking of Tunnel Transistor-Based Ex-OR Gates for Energy Efficient Computing," Journal of Circuits, Systems, and Computers (JCSC), Vol. 29, No. 8, June-2020.
2. Itamar Levi, Alexander Belenky, and Alexander Fish, "Logical effort for CMOS- based dual mode logic gates", IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 22, pp. 1042-1053, May2014.
3. ViacheslavYuzhaninov, Itamar Levi, And Alexander Fish, "Design flow and characterization methodology for dual mode logic", IEEE Access, vol.3, pp. 3089-3101, January2016.
4. VivechanaDubey, Ravi Mohan Sairam," An arithmetic and logic unit optimized for area and power", Fourth International Conference on Advanced Computing & Communication Technologies, pp 330-334,IEEE,2014.
5. AsafKaizerman, Sagi Fisher, Alexander Fish, "Subthreshold dual mode logic", IEEE Transactions on VeryLarge-Scale Integration (VLSI) Systems, vol.:21, issue 5, pp. 979- 983, May2013.
6. Shiksha and Kamal Kant Kashyap," High speed domino logic circuit for improved performance", Students Conference on Engineering and Systems (SCES), 2014, IEEE 28-30 May2014.
7. Sadulla Shaik, K. Sri Rama Krishna, and Ramesh Vaddi, "Tunnel Transistor-Based Reliable and Energy Efficient Computing Architectures with Circuit and Architectural Co-Design at Low VDD," Journal of Circuits, Systems, and Computers (JCSC), Vol. 27, No. 3, 2018,
8. K. Vinay Kumar, Fazal Noor Basha, B. Shiva Kumar, N. V. Siva Rama Krishna .T, "Design of an efficient ALU using low-power dual mode logic", International Journal of Engineering Research and Applications(IJERA),vol. 4, issue 5 (Version 4, pp.81-84), May 2014.
9. Amrendra Kumar Yadav, Bovana Naveen, "The energy penetrating CMOS compositions projected from dual mode logic-based adder", International Journal of Electronics & Communication Technology (IJECT), vol. 6, issue 4, pp. 81-84, December2015.
10. Anantha Reddy K, T. Vasudeva Reddy, "Design and verification of dual mode logic (DML) for power efficient and high performance", International Journal of Advance Engineering and Research Development (IJAERD), vol. 1, issue 12, pp. 1-8, December-2014.
11. Sally Ahmed, "A Compact Adder and Reprogrammable Logic Gate Using Micro-electromechanical Resonators with Partial Electrodes", IEEE Transactions on Circuits and Systems, Vol. 66, Iss. 12, 2019, pp. 2057-2061.
12. Hamed Naseri, "Low-Power and Fast Full Adder By Exploring New EXCL-OR and EXCL-NOR Gates", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 26, Iss. 8, 2018, pp.1481 -1493.