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Research Article

HIGH SPEED AND LOWPOWER GDI BASED FULL ADDER

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ABSTRACT
Full adder is one of the fundamental digital block in the many electronic circuits. As the day by day scaling down the technology(Deep-sub micron level) power consumption becomes one of the primary concern for any portable electronic devices. In this paper our main motto is to design and implement the low power full swing full adder, using GDI (Gate Diffusion input)technique. Simulated full swing GDI based adder using the cadence virtuoso in 180nm technology. and also we conducted the a comprehensive study on different types of full adders and their performances with respect to SERF and 28 T circuits respectively.

Keywords: Full Adder,GDI

INTRODUCTION

With the enormous development of versatile electronic items, the creators are headed to endeavour for longer battery life, higher speed, and improved quality with innovation scaling. which push the market interest for additional what's more and more capacity in Integrated circuit(IC).In many electronic devices addition is one the fundamental operation, these operation can be widely used in many application areas. full adder is one of the basic fundamental electronic circuit which can extensively used to perform the addition operation. A wide verity of full adders have been implemented and simulated using different circuit topologies to perform the single bit addition[1-3].although many of papers has been published on full adders and mentioned in literature survey [4-6] but which produces the different yields in terms of propagation delay, power consumption, size and wiring complexity of the circuit. the basic block diagram of full adder as shown in fig1 and its truth table 1 represents the operation of full adder.

Table 1: truth table of 1bit-full adder.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

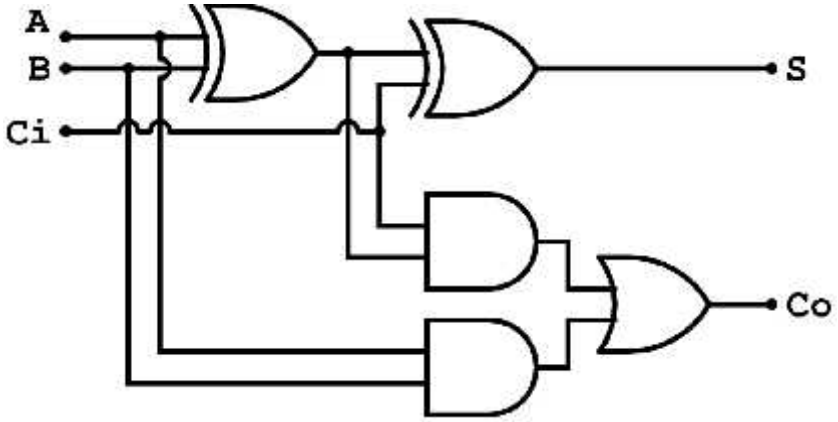

Fig 1:Block diagram of Full Adder.

The rest of the paper is organised as follows section 2 describes the various types of the CMOS type full adders and their comparison 3 explains the GDI based CMOS full adder and simulation results.

Previous work

A wide verity of CMOS full adders cells are proposed to achieve the high speed and low power. Generally full adders have been classified majorly in two types such as classical design, which means the whole circuit can be implemented using only PMOS and NMOS by means of pull up and pull down configuration modelling[7]. On the other hand design of full adder using hybrid style, the circuit can be designed using the more than one logic style[]. in below section we are explaining the different types of full adders using the CMOS architectures respectively.

CMOS full adder using 28 transistors

As shown in Fig:2 the full adder is designed using 28 transistors using convention CMOS topology. Due to more number of transistors which may leads to more power consumption and occupies the huge area. One of the most desired feature and significant advantage is it offers the full voltage swing, better noise immunity and operated at wide range of temperature.

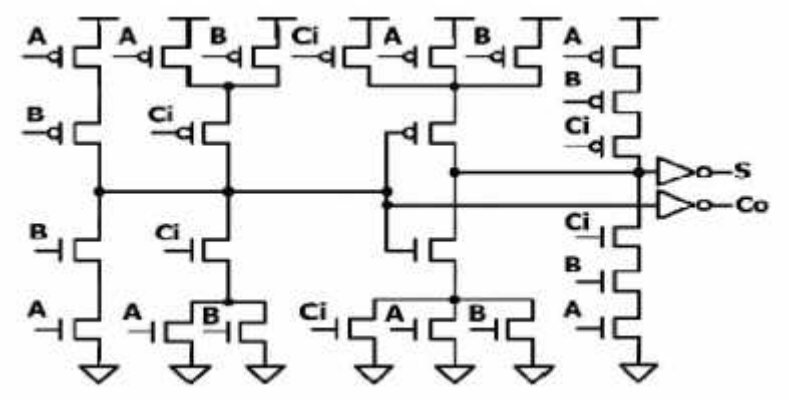

Fig 2: CMOS full adder using 28 transistors.

CMOS full adder using 16 transistors

in order to reduce the number of transistors and decrease the power consumption proposed a full adder by compositing of 16 transistors. The design is combination of XOR and XNOR circuits as well as transmission gate respectively. This 16 transistor adder reduces the power as compared to conventional full adder circuit. the architecture of the CMOS full adder as shown in figure3. respectively[8-10].

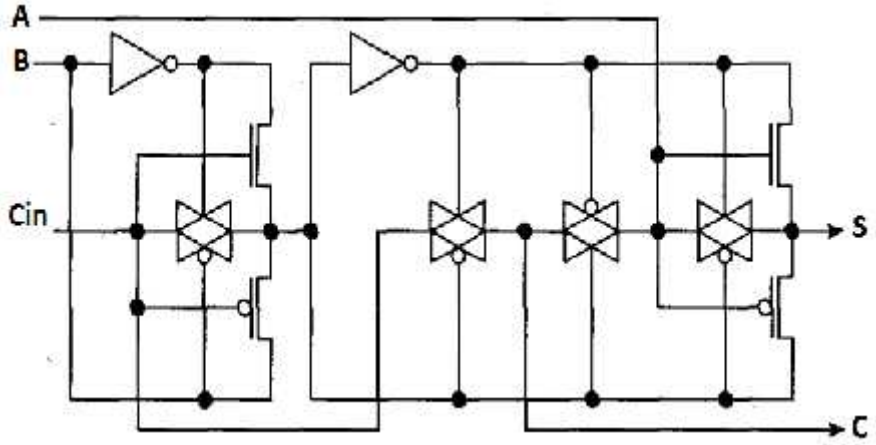

Fig 3: CMOS full adder using 16 transistors.

Static Energy Recovery Full Adder (SERF)

Further to improve the performance of the proposed a full adder using only 10 transistors. this full adder reduces the power and enhances the speed of the circuit to achieve the sum and carry output without reducing the full swing voltage. During the design of the SERF there is no direct connection is between VDD to ground. The capacitor stores the capacitor stores the charge with respect to the supply grounds. figure4. depicts the CMOS SERF full adder.

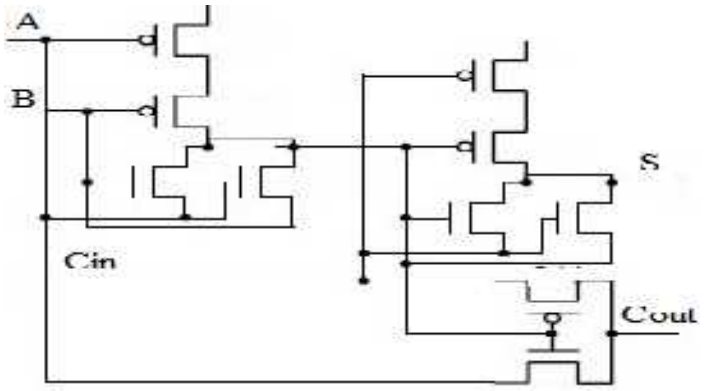

Fig 4: SERF Full Adder

GDI based full adder

The basic GDI cell is designed with the help of CMOS inverters, the architecture consists of PMOS and NMOS transistors. In conventional CMOS inverter PMOS and NMOS substrates are connected to VDD and ground respectively. On the other hand here the diffusion terminals are taken to be input terminals. The basic GDI based cell shown by figure 5 respectively. As the GDI cell is going to perform the different types of the Boolean operations, (inverter, buffer, or, xor, nor, mux)as shown in the table-2.

Table 2. Truth table of CMOS GDI cell

N	P	G	Out	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{A}$	NOT

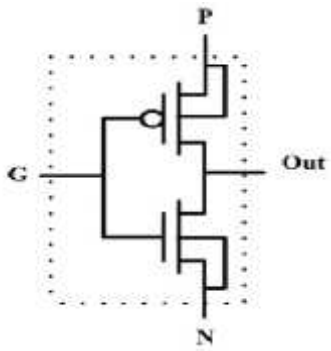

Fig 5: Basic GDI cell.

Proposed GDI full adder

The proposed GDI based full adder is generates the full swing output without need of the any swing restoring circuits. which completely avoids the buffers there the performance can be improved. The possible full swing can be achieved by rewriting the full adder expression in to the equation(1)& (2) respectively. the designed structure as shown in figure 6 and whose layout also drawn using the cadence virtuoso 180 nm technology.verifed the DRC,LVS and RC extraction for the proposed circuit .

$$Sum = \overline{C_{in}}(A\ \mathbf{XOR}\ B) + C_{in}(A\ \mathbf{XNOR}\ B) \qquad (1)$$

$$C_{out} = (A\ \mathbf{XOR}\ B)C_{in} + \overline{(A\ \mathbf{XOR}\ B)}A \qquad (2)$$

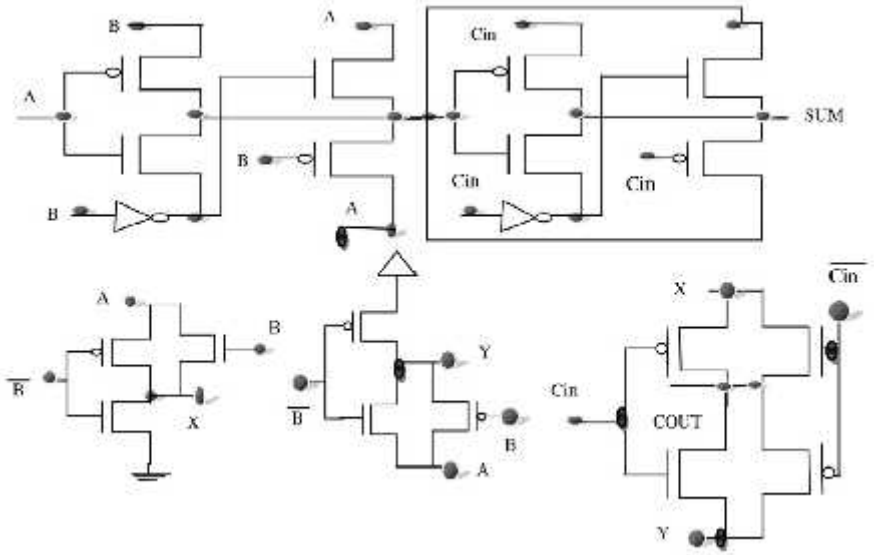

Fig 6: proposed full swing GDI full adder.

simulation setup

In order to measure the metrics of the proposed full adder we have been simulated using the cadence virtuoso 180nm technology, with the supply voltage of 1.8v and ambient temperature of 27^0C respectively. All PMOS and NMOS transistors has Lmin=180nm.we applied the 50ms at transient time and verified the output voltage at all nodes. From the obtained results it consumes the minimum power consumption of 1084nanowatts and maximum power consumption of 1217 and 1084nanowatts.In similar passion the delay was obtained as 22.6 and 31.8ps respectively.

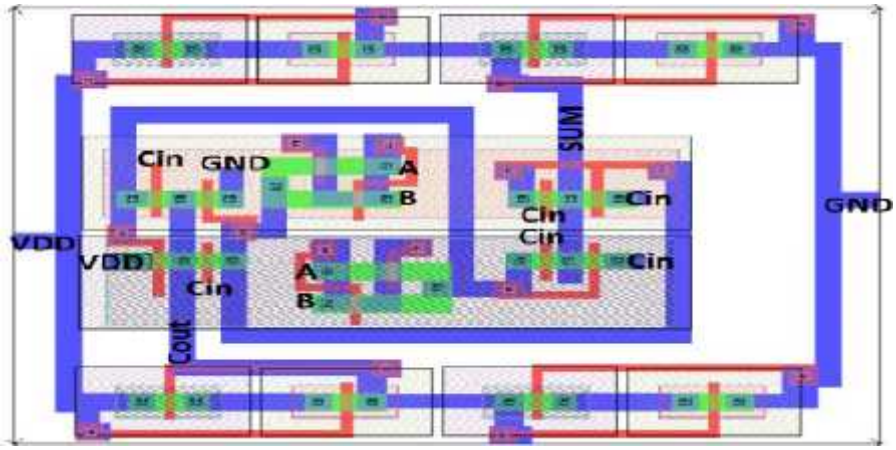

Fig 7: Layout for Proposed full swing GDI full adder.

Conclusion

The proposed GDI based full adder requires the total number of 22 transistors and which produces the output without any degradation. The design opts for high speed ALU and DSP processors without power consumption and produces the fast operation. hence the proposed GDI full adder widely employed for high speed VLSI application.

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