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A Low Power Adiabatic Approach for Scaled VLSI Circuits

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Abstract

Two Phase Clocked Adiabatic Static CMOS Logic (2PASCL) approach is proposed as an efficient power reduction technique in this work to reduce the overall power consumption of any VLSI circuit. One of the most significant area of research in today's VLSI domain is power reduction. By using a complementary phase-shifted voltage source, we can minimize the charging-discharging of the load capacitor in each clock pulse, which plays a vital role in reducing the circuits' dynamic power consumption.[1]

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Introduction

Low power advancements are required by the increased usage of mobile phones, portable electronic devices, and other wireless electronic gadgets. In most digital circuits today, the complementary metal-oxide-semiconductor logic circuitry scheme has been the technique of choice for implementing low-power systems. As clock and logic speeds increase to meet new performance requirements, the energy supply voltage need of this type of circuit is becoming a critical concern in the design of these devices [1], [9], [10]. Energy usage in digital circuitry has become a crucial component in high-speed and portable electronic device applications. One strategy to save energy is to use an adiabatic arrangement. The term 'adiabatic' arises from "thermodynamics" and refers to a system that does not absorb or lose heat during a change. If the transformation is carried out slowly enough, the heat (energy) loss can be minimized to almost nil in an ideal circumstance. Recovering the charge is just another strategy to enhance energy saving. A conventional Complementary metal oxide semiconductor (CMOS) logic circuit does not recover the charge that is depleted in the ground, unlike an adiabatic circuitry. A reasonably strong current travels via both PMOS and NMOS transistors just before occurring of the state transition, either from '0' to '1' or vice versa, as well as the energy stored in the capacitive node is lost during the discharge [2]. Earlier many researchers tried to design basic circuitry or digital systems by using a constant dc power supply. And we all know energy usage in any circuit is directly proportional to supplied voltage sources [3]-[8]. So, to maintain the working condition of any digital system we may keep this magnitude of dc voltage up to a certain level and this increases the power or energy consumption of this particular system in a linear way. And that's why many digital electronics devices don't work properly and may be destroyed at times. In this situation to overcome this problem we need an efficient or effective method to control the excessive usage of the energy. Thus we need to design circuitry in a way so that it can consume less power. It means in a conventional CMOS circuit when the pMOS is on, the current starts flowing through R, and then a charge of Q = CLVdd is pulled out and it will charge the load capacitor up toVdd.[1]

So, it is observed that a large amount of energy is wasted fully in this condition. In this situation if we save this amount of energy by using any approach or method, it becomes very beneficial for that circuitry to enhance the overall performance and the system efficiency. And that's why saving this amount of energy is the main motivation of this work. An adiabatic strategy is one option to reduce power usage. The adiabatic method is a cost-effective way of recycling the energy held inside the load capacitor by

releasing this to the earth. As a result, we present the "2PASCL (2-Phase Clocked Adiabatic Static CMOS Logic) circuit" in this work.

Methodology

We all know that there are so many approaches or methods available to suppress the energy usage of any digital VLSI circuitry.[11]-[17] Out of so many techniques, the use of "adiabatic" techniques to minimize the power usage of any circuitry is one of the best options.[3]. In recent times, the focus of the researchers is to increase the clock and the logic speed of wireless devices to obtain enhanced performance. So, in this manuscript the Two Phases Clocked Adiabatic Static CMOS Logic (2PASCL) circuit is employed as an efficient technique to reduce overall power consumption in digital circuitry.

Adiabatic Logic Principle

To reduce energy waste when charging and discharging, adiabatic switching is frequently employed. The term "adiabatic" refers to a state change without a net gain or loss of heat. To reduce power loss during adiabatic switching, all of the nodes are charged/discharged at a constant current. The circuit is first charged using AC power supplies during specific adiabatic phases, and then the circuit is discharged to recover the initial charge. The way energy is lost in adiabatic logic circuits during any switching transitions is depicted in Fig 1. Because adiabatic circuits use a time-varying voltage source rather than a fixed voltage supply, the rate of switching transition is slower than it is for conventional charging.

By guaranteeing uniform charge transfers across the entire available time, the maximum current in adiabatic circuitry can be greatly decreased. Therefore, the overall power dissipation even during transition period can be reduced in proportion as follows if I is assumed to be the average of the current that flows to CL.

$$E_{diss}E_{diss} = I^2RT_p\, I^2RT_p = \left(\frac{C_LV_{dd}}{T_p}\right)^2 RT_p \frac{C_LV_{dd}}{T_p}\Big)^2 RT_p \quad (1)$$
$$= \left(\frac{RC_LRC_L}{T_p\ T_p}\right)C_LV_{dd}^2C_LV_{dd}^2$$

Theoretically, in adiabatic charging, power dissipation is almost nil when the duration for the drive voltage Φ to shift from 0 V to Vdd [Tp is lengthy]. In this case, discharging through the nMOS transistor takes place when in the pull-down network Φ changes from HIGH to LOW. From Eq. (1), it is clear that the system draws some of the energy which is stored in the capacitors during a given computing step and uses it in subsequent computations when power dissipation is minimized reducing the rate of switching transition.

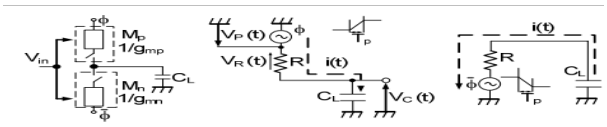

Fig. 1: Charging-Discharging of an adiabatic logic circuit with ideal switches

Circuit Operation

Fig.2 Shows a circuit diagram illustrating the operation of "2PASCL Inverter Circuit" logic. The two diodes, one in the output terminal next to the power clocks supply and the other one is beside the nMOS circuitry to another power clock, are the initial distinction between 2PASCL and constant CMOS logic gates. MOSFET diodes are being used to recover the charges from output terminal, to enhance discharging frequency of internal signal endpoints. This is highly helpful for signal modules with a long string of switching devices before them.[1] The key advancement is the reduction of energy consumption. We may use this to achieve higher amplitude while reducing energy dissipation.

A "phase-shifted split level sine wave voltage" is also delivered to the circuit to reduce "dynamic power dissipation".

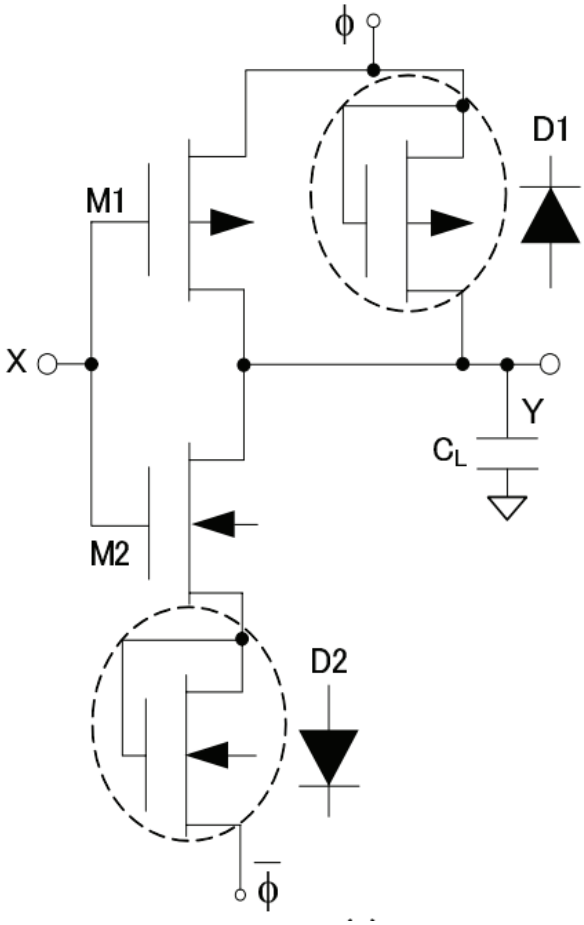

Fig. 2: "2PASCL Inverter Circuit" [1]

To recycle charges out from the output terminal, two MOSFET diodes (D1, D2) are needed. The pull-up network is near one diode, while the pull-down network is near the other. Fig. 3. depicts the "evaluation" and "hold" phases of the 2PASCL operating phase. The voltage driver φ swings up and $\overline{\varphi}$ down during the evaluation phase. The hold, on the other hand, is when the $\overline{\varphi}$ swings up and φ down.[1]

When the output node Y is in Low position and both the pMOS is turned ON during the evaluation stage, CL is charged through the pMOS transistor, leading to a High state at the output terminal. At this stage or phase the transitions of the state are same if pMOS is turned ON and the output terminal is in High state and also if the nMOS is turned ON and the output is in Low position. Finally, discharge occurs through the use of nMOS when the Y node is High and nMOS is ON.

Because of the diodes, the state of Y while the preceding state is LOW remains fixed during the hold phase. When the output node's preliminary state is HIGH, it changes to the diode's threshold voltage. Discharging through the use of diode D1 occurs at this point.

Theoretical Analysis

The transistors channel resistance and the threshold voltage are responsible for power dissipation in adiabatic circuits. An RC model is used to calculate the energy used in adiabatic circuits and Vt is the threshold voltage. The 2PASCL inverter's energy dissipation looks something like this:

$$\begin{aligned} E_{2PASCL} &= E_{2PASCL} = E_{chra(M1)} + E_{dischra(D1)} + E_{dischrg(M2,D1)} \\ & E_{chrg(M1)} + E_{dischrg(D1)} + E_{dischrg(M2,D1)} \\ &= 0.5C_L V_{tp}^2 0.5C_L V_{\varphi p-p}|V_{tP}| + 0.5C_L(V_{\overline{\varphi}p-p} - V_{tn})V_{tn} \\ &= 0.5C_L\left(V_{tp}^2 + V_{\varphi p-p}|V_{tP}| + \left(V_{\overline{\varphi}p-p} - V_{tn}\right)V_{tn}\right) \quad (2) \end{aligned}$$

Where CL is load capacitance; Vtp is the pMOS threshold voltage; Vtn is the nMOS threshold voltage, and $V_{\varphi p-p}V_{\varphi p-p}$ and $V_{\overline{\varphi}p-p}V_{\overline{\varphi}p-p}$, are the supply voltages.

While for theoretical computations, linear ramp waveforms are being used, we are employing split-level sinusoidal waveforms here. The tendency is identical, nevertheless, and this analytical analysis has allowed us to comprehend the main causes of the power dissipation in the 2PASCL inverter. By using $V_{\varphi p-p}V_{\varphi p-p}$and $V_{\overline{\varphi}p-p}V_{\overline{\varphi}p-p}$ as split-level sinusoidal waveforms with a peak-to-peak voltage of 0.9 V, as shown in Eq. (2), we have conserved around 50% more energy than we would have with non-split-level waveforms.

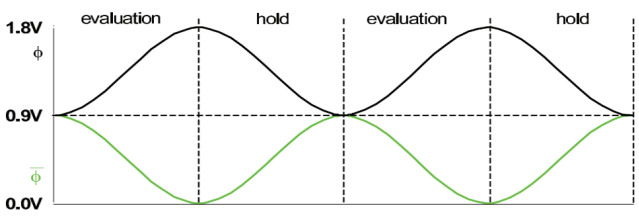

Fig. 3: "Description both the phase of a clocked voltage driver"

Software Used

For our circuit simulation, we have utilized Tanner EDA 2019.2 version. So, using the SPICE Simulator, we design and simulate a "CMOS" inverter, "NOR Gate", a "D flip flop" and a "Half Adder" both with and without the proposed approach. The "average power consumption" of all the circuits is compared and it is observed that the proposed method shows superior performance in all the cases.

Proposed Design

A. CMOS Inverter without 2PASCL

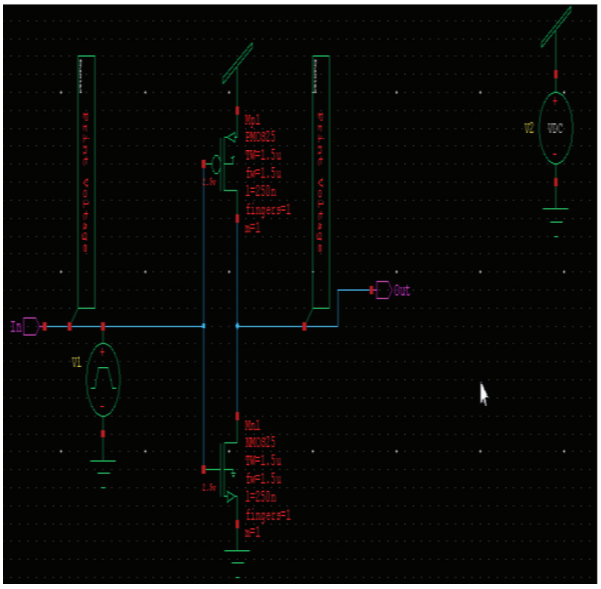

Fig. 4: Schematic of CMOS Inverter without 2PASCL

B. CMOS Inverter using 2PASCL

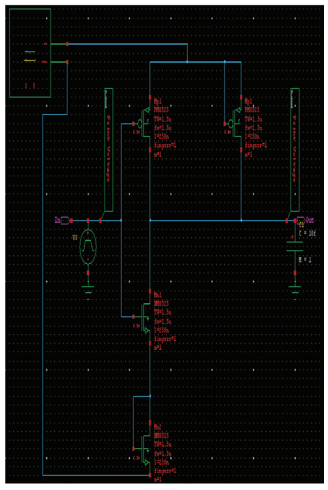

Fig. 5: Schematic of CMOS Inverter using 2PASCL

C. NOR Gate without 2PASCL

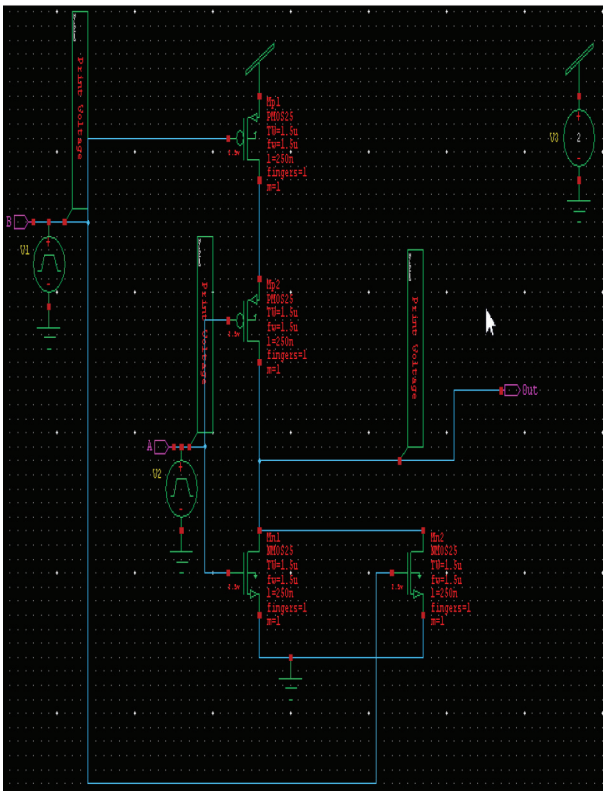

Fig. 6: Schematic of NOR Gate without 2PASCL

D. NOR Gate using 2PASCL

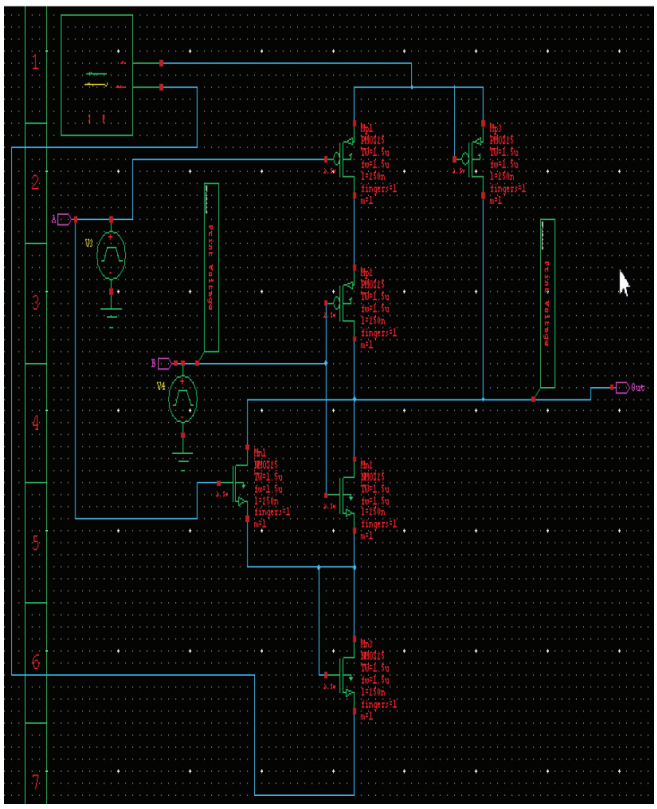

Fig. 6a: Schematic of NOR Gate using 2PASCL

E. D Flip Flop without 2PASCL

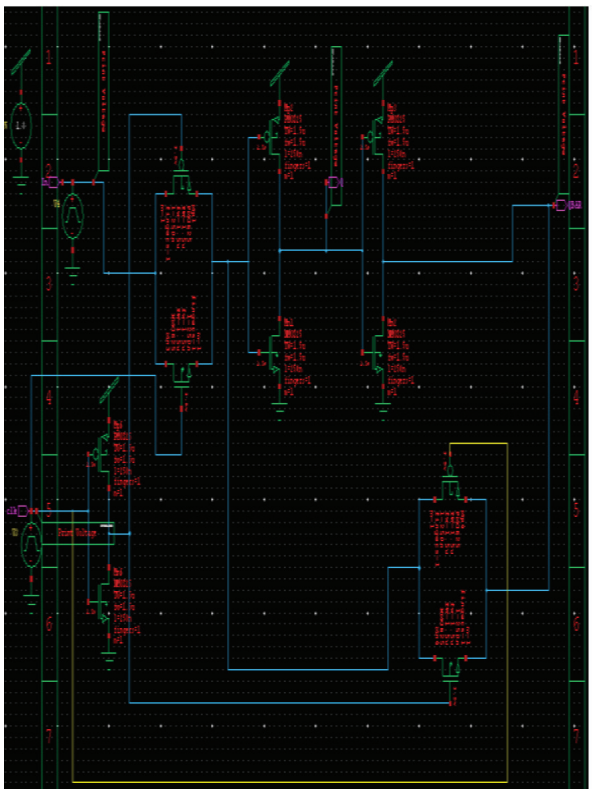

Fig. 7: Schematic of D Flip Flop without 2PASCL

F. D Flip Flop using 2PASCL

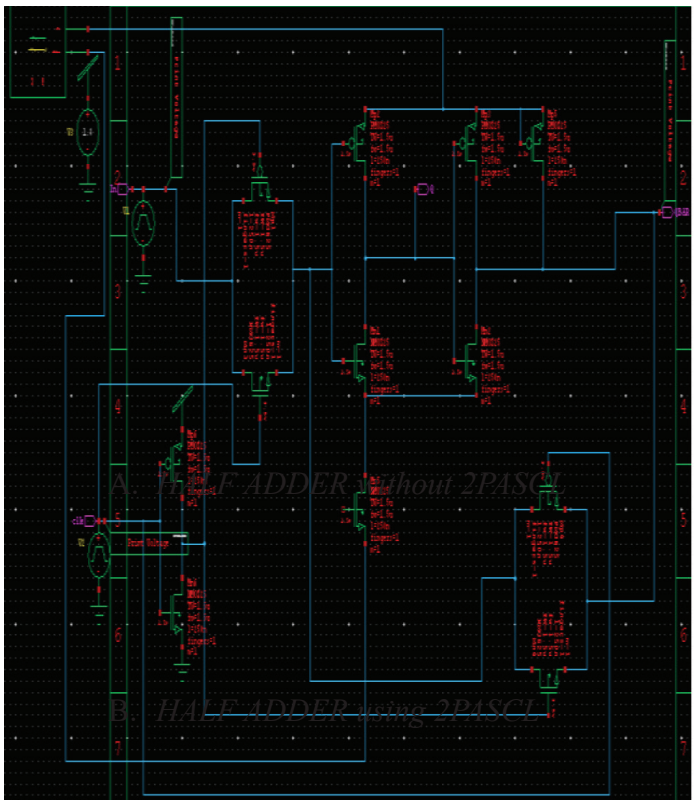

Fig. 8: Schematic of D Flip Flop using 2PASCL

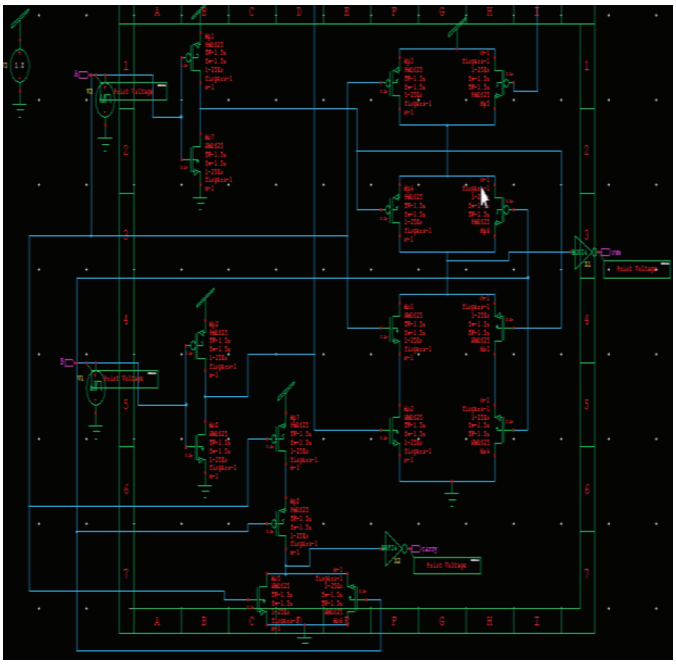

Fig. 9: Schematic of HALF ADDER without 2PASCL

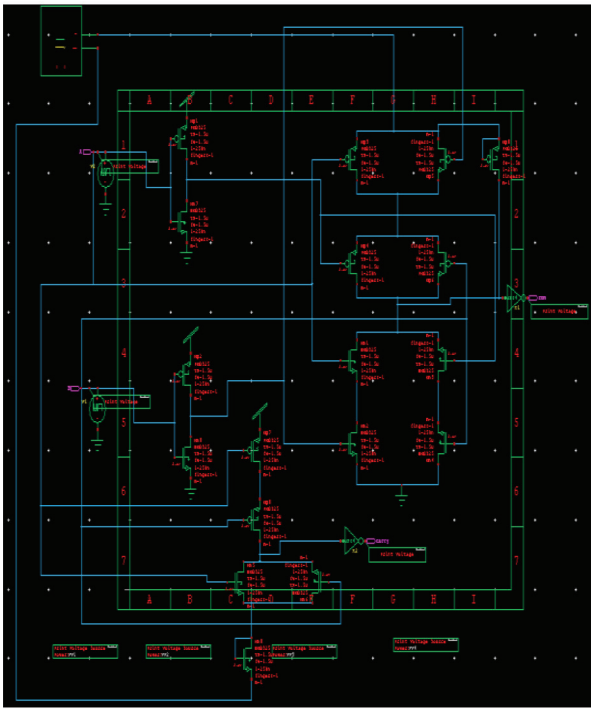

Fig. 10: Schematic of HALF ADDER using 2PASCL

Results

Table I shows the average power comparison that was obtained with and without the proposed technique for various circuits. The comparison chart of CMOS inverter, NOR Gate, D Flip Flop, and Half Adder using 2PASCL topology is shown Fig. 12. All the elements using 2PASCL topology consume less power as compared to those without 2PASCL topology.

Table 1: Average power consumption with and without 2PASCL

ELEMENTS	WITHOUT 2PASCL (mW)	WITH 2PASCL (mW)
CMOS INVERTER	6.066	0.955
NOR GATE	11.92	2.885
D FLIP FLOP	9.665	2.529
HALF ADDER	25.461	8.146

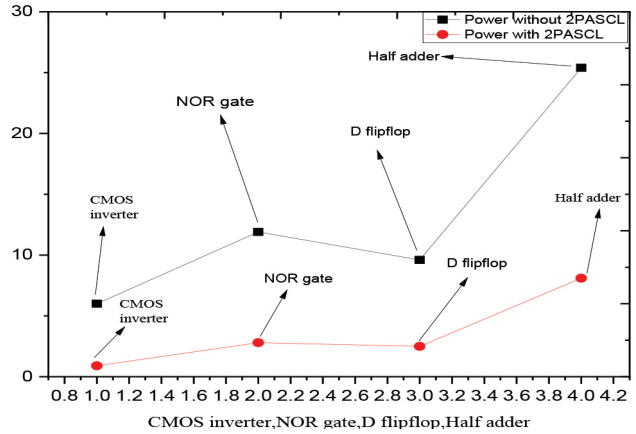

Fig. 11: Graph showing average power consumption of all the circuits with and without 2PASCL

Conclusion

The average power consumption of the "2PASCL" method is lowered by 70-80% when compared to the standard Complementary metal-oxide-semiconductor circuits, according to simulation data. The charging/discharging of the load capacitor is minimized when "2PASCL logic" is used because the capacitor is not charged or discharged in every clock cycle.

Conflict of Interest

The authors of this paper like to state that they have no conflicts of interest related to this work with other published works in similar domain as far best of their knowledge.

Author Contributions

The research work is original in nature and carried out solely by the first author under the guidance of Dr. Abhishek Bhattacharjee and relevant discussions and help from Dr. Tanmoy Majumder from time to time.

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