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Design and FPGA Realization of Energy Efficient Reversible Full Adder for Digital Computing Applications

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Abstract

Arithmetic primitives are necessary in order to conduct computations on large numbers in arithmetic circuit implementations including multiplications, additions, subtractions, and divisions. Because of the importance of computations in the central processing unit, effective design of arithmetic circuit has been part of the most important fields of research for design engineers. In order to create low-power and energy-efficient portable processors for image and digital signal processing, as well as cryptography applications, the switching activity factor and cell count must be reduced. This research focuses on the reversible digital full adder circuit, which is a key element in establishing the Energy Delay Product (EDP) for various computer applications. Here, a new reversible binary full adder is designed using the switching activity concept and the logic decomposition method. The internal blocks for reversible full adders such as Feynman Gate, Toffoli Gate, and New Gate are designed first, then a new reversible binary full adder is developed using the proposed method. In this paper, conventional and proposed reversible full adders are synthesized using the Xilinx Vivado design suite for the Zynq-7000 family of device configuration. According to the implementation results, the proposed reversible full adder circuit consumes less dynamic power dissipation than the existing method in comparison. Furthermore, a formulae-based evaluation is conducted on the implementation results to estimate the EDP of the design. The proposed reversible full adder design can achieve a 32.3% EDP improvement compared to the Proposed Full Adder.

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Introduction

Minimization of dynamic power dissipation is one of the primary objectives of digital logic design. A new innovative approach is explained in [1] to design low power full adder. In current days, reversible logic has attracted considerable interest to design logic circuits. Novel design of full adder using suitable reversible logic gates is presented in.[2] A FADE, which is novel 4×4 reversible gate logic is reported in.[3] Quantum logic circuits are therefore difficult to design without reversible logic concept. Reversible combinational logic synthesis is exponentially more difficult than conventional digital circuit synthesis since we're not enabled to use the concept of fan-out and feedback mechanism in a reversible logic circuit. In,[4] A survey of the design of logic circuits such as binary adder, binary subtractor, binary multiplier, and division has been conducted. In,[5] a 3×3 reversible universal and multifunctional gates using quantum-dot a cellular automaton is reported. High-performing processors that generate a lot of heat put a realistic limit about how far researchers can enhance the accuracy. Energy consumption efficiency will indeed gain through reversible computation. Gate count and other logical measures have been used to estimate the hardware quality of crypto-primitive algorithms is discussed in.[6] A novel design of reversible Full adder/subtractor with minimum number of cells has been distinguished in.[7] Reversible computation is needed

to enhance device accessible yet further. This will allow circuit component sizes to be minimized to microscopic proportions, enabling electronics more accessible. In,[8] An QCA based design provides an ultra-efficient full adder is designed using the concept of explicit interaction of cells is discussed. In,[9] conventional digital circuits using reversible logic are presented. Although the expense of embedded system in the coming days may be considerable, in today's digital revolution, dynamic power and tradeoffs are more crucial than circuit manufacturing costs, therefore the necessity for reversible processing cannot be neglected. The Design of full adder using reversible logic with minimum constant input and garbage output is reported in.[10]. The design of fault tolerant full adder using parity preserving logic is proposed in.[11] Due to the abrupt switching of input signals in recent VLSI circuit design, dynamic power consumption is exceptionally high. Conventional Combinatorial Circuits produce heat for each bit of binary data lost through execution. As a result, once data is missing, it cannot be restored in almost any method. In,[12] the design of combinational logic circuits using reversible logic with minimum quantum cost is discussed. In,[13] a reversible logic concept is introduced to design new full adder to minimize gate count and garbage outputs. When studying the manufacturing of reversible gates, we need circuits with a minimum number of gates and transistors. However, many Boolean expressions are irreversible. To minimize cell count, quantum cost and garbage outputs an attempt is made on combinational circuits, reported in.[14]. The dynamic power consumption due to circuit switching activity factor is discussed in.[15] We must first convert irreversible functions into reversible functions before fulfilling these functions. Every transformation technique that turns an irreversible expression of a reversible expression involves data bits that have been assumed to be zero. The design of an arithmetic logic unit (ALU) using reversible logic gates is reported to minimize power dissipation in.[16] The binary full adder design 1 and design 2 are reported in.[17] In the field of IC design, minimum power dissipation design has emerged as a promising research area. Low-power digital logic design techniques rely on choosing the best components to decelerate automation without affecting system features. In,[18] design of an ALU using two programmable reversible logic gates is presented. In,[19] design of multiplier using reversible logic gate is reported. Researchers should optimize diverse computations while keeping propagation latency and dynamic power dissipation low. It can display great power dissipation and speed, and it is evolving into more complex designs and styles. The detection of faults at output of logic circuits using parity preserving is proposed in.[20] The design of novel full adder using HNG gate is introduced in.[21]. Concerning this subject, researchers are working for years to improve designs and have presented a novel model based on reversible circuits to attain minimum delay and dynamic power dissipation. Energy consumption is still one of the main key aspects to concentrate on in modern technology. In,[22] fast reversible multiplier is proposed with less circuit complexity. The NXN reversible multiplier using TSG gate is presented in.[23]. The design of a ripple carry adder, BCD adder and carry look-ahead adder using TSG gate is reported in.[24] This study, which is a considerable extension of[1, 2], is organized as follows: The essential fundamentals demanded for the latest research initiatives are given in Section II. The introduction of reversible logic gates is covered in further depth in Section III. The design of reversible full adders is discussed in Section IV. IN Section V, the simulation and implementation results for reversible gates and full adders and then performance metrics assessment is described followed by the conclusion.

Preliminaries

Power dissipation: Static power dissipation of Metal Oxide Semiconductor (MOS) is proportional to the supply voltage (Vdd) and leakage currents flows in the transistor.

$$P_{static} = I_{leakage} \times V_{dd} P_{static} = I_{leakage} \times V_{dd} \quad (1)$$

Dynamic power dissipation of a MOS device is largely the result of the switching activity, capacitive loads, operating frequency and supply voltage (Vdd).

$$P_{dynamic} = \alpha \times C_L \times f \times V_{dd}^2 P_{dynamic} = \alpha \times C_L \times f \times V_{dd}^2 \quad (2)$$

In today's technology 80% of power dissipation occurs because of switching activity factor. In order to reduce power loss of MOS circuits, it is necessary to minimize the SA value of digital Very Large-Scale Integration (VLSI) circuits.

Switching Activity: The generalized expression to estimate the SA of any basic digital logic gate is expressed as

$$SA = \frac{2^n - 1}{2^{2n}} SA = \frac{2^n - 1}{2^{2n}} \quad (3)$$

Where, N indicates the number of inputs

For example, the SA value of single input NOT gate is 1/4, two input basic gates are having a SA value of 3/16, and three input basic gates SA value is 7/64. The single, two, and three input gates with their SA values are shown in the Fig.1.

Cell Count: In this paper, area occupied by digital circuit design is defined based on the number of cells require implementing any combinational circuit. The total cell count is defined as the summation of all individual NOT, AND, OR, and NAND gates used in the process of designing digital logic circuits.

Figure of Merit: The product of input to output propagation delay and the average power consumption has been used as FOM for digital circuits. FOM is used to measure and compare devices intended for linear circuit applications. FOM is used to determine the quality of a digital logic gate.

$$FOM = P_{avg} \times t_{pd} FOM = P_{avg} \times t_{pd} \quad (4)$$

Power Delay Product: The digital circuit designer goal is to minimize PDP; in order to get low power at frequency operated digital circuits. The PDP measures the energy consumption level of the gate. The PDP stands for the dynamic power consumed per switching event. The power delay product is amount of energy required to perform the computation. However, a digital logic design with minimal PDP may be very slow in performing its computation.

$$PDP = P_{dynamic} \times t_{pd} PDP = P_{dynamic} \times t_{pd} \quad (5)$$

Energy Delay Product: Therefore, energy delay product is estimated to get on the better performance of the digital logic circuit design. The energy delay product of any digital circuit design is described as the product of power delay product and input to output propagation delay.

$$EDP = PDP \times t_{pd} EDP = PDP \times t_{pd} \quad (6)$$

Reversible Logic Gates

A. Feynman Gate (FG)

The feynman gate [2] is a 2×2 reversible gate i.e., FG accepts two input signals and redirects to two output signals. Boolean equation representation of feynman gate is given below

$$F_{i,j}^2 \vdots Z_i = X_i F_{i,j}^2 \vdots Z_i = X_i \quad (7)$$

$$Z_j = X_i \oplus X_j Z_j = X_i \oplus X_j \quad (8)$$

The basic symbol of FG reversible gate and its functional table is shown in Fig.2. The internal logic diagram of FG

Reversible gate using conventional and proposed method is shown in Fig.3. In Fig.3, each and every gate represented with their switching activity value. The total SA value of FG reversible gate is obtained by adding all individual SA value of logic gates. From Fig.3, we observed that the SA value of Conventional FG (CFG) gate is 1.0625 and the total SA value of FG gate using the Proposed (PFG) method is 0.5625.

$$SA_{CFG} = 2 \times \frac{1}{4} + 3 \times \frac{3}{16} SA_{CFG} = 2 \times \frac{1}{4} + 3 \times \frac{3}{16} \quad (9)$$

$$SA_{PFG} = 3 \times \frac{3}{16} SA_{PFG} = 3 \times \frac{3}{16} \quad (10)$$

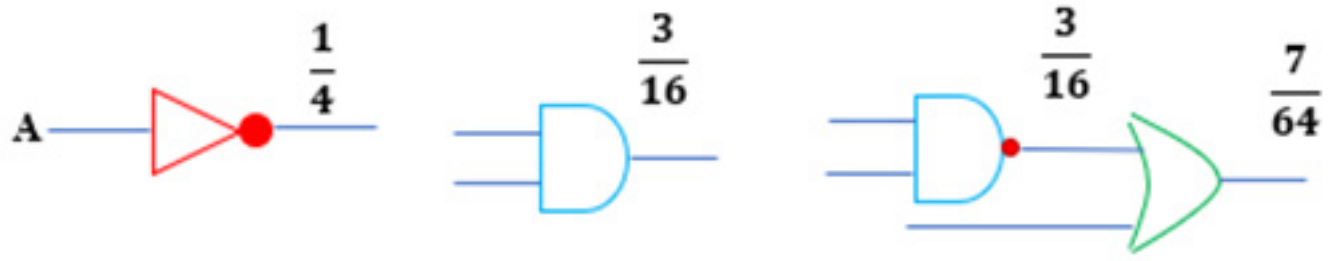
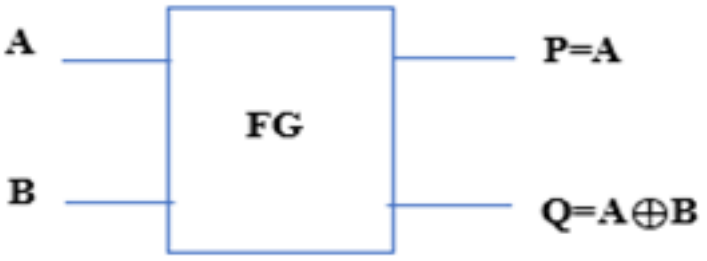


Fig. 1: SA values for one, two, and three input logic gates



(i)

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(ii)

Fig. 2: (i) Symbol of FG (ii) Functional table of FG

B. Toffoli Gate (TG)

The toffoli gate is a three-way reversible gate, which means it accepts three input signals and sends three output signals. The toffoli gate is represented by a Boolean equation as shown below.

$$T^3_{i,j,k} \vdots\ Z_i = X_i T^3_{i,j,k} \vdots\ Z_i = X_i \quad (11)$$

$$Z_j = X_j Z_j = X_j \quad (12)$$

$$Z_k = X_i X_j \oplus X_k Z_k = X_i X_j \oplus X_k \quad (13)$$

The basic symbol of TG [2] reversible gate and its functional table is shown in Fig.4. The Fig.5 and Fig.6 shows the internal logic diagram of the conventional and proposed TG reversible gate.

Each gate is illustrated in the Fig.5 and Fig.6 with its switching activity value. By summing all of the individual SA values of logic gates, the total SA value of the TG reversible gate is calculated. The SA value of a Conventional TG (CTG) gate is 1.0156, while the overall SA value of a TG gate employing the proposed technique is 0.5156, as shown in the Fig. 5 and Fig. 6.

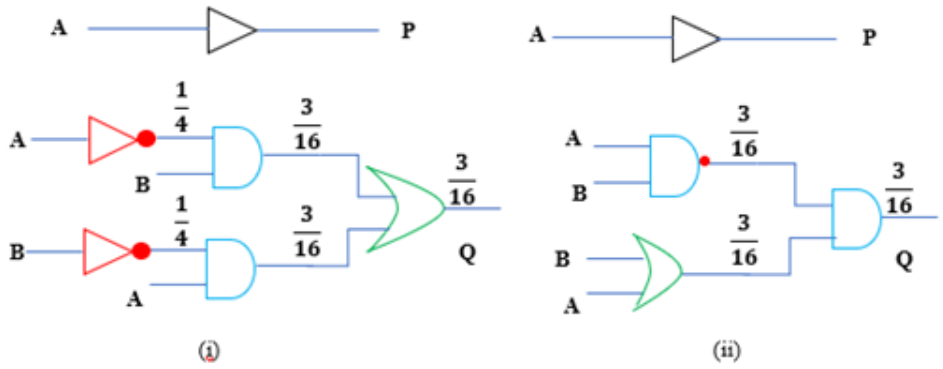
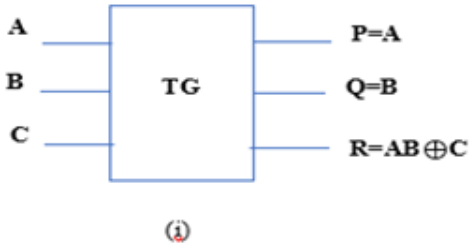


Fig. 3: (i) Logic diagram of Conventional FG gate (ii) Proposed FG gate



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

(ii)

Fig. 4: (i) Symbol of TG (ii) Functional table of TG

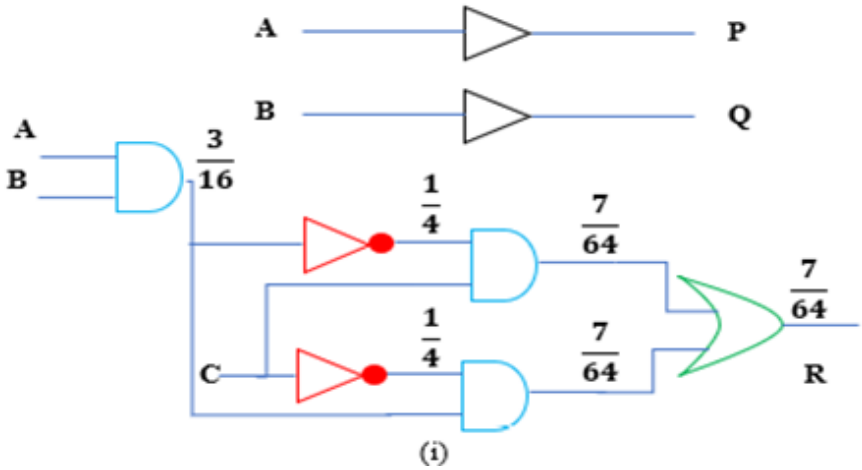


Fig. 5: Logic diagram of Conventional TG gate

$$SA_{CTG} = 2 \times \frac{1}{4} + \frac{3}{16} + 3 \times \frac{7}{64} \quad SA_{CTG} = 2 \times \frac{1}{7} + \frac{3}{16} + 3 \times \frac{7}{64} \tag{14}$$

$$SA_{PTG} = \frac{3}{16} + 3 \times \frac{7}{64} SA_{PTG} = \frac{3}{16} + 3 \times \frac{7}{64} \tag{15}$$

C. New Gate (NG) [2]

The new gate is a three-way reversible gate, indicating it accepts three input signals and produces three outputs. A Boolean equation is used to represent the new gate, as shown below.

$$N^3_{i,j,k} \vdots\ Z_i = X_i N^3_{i,j,k} \vdots\ Z_i = X_i \tag{16}$$

$$Z_j = X_i X_j \oplus X_k Z_j = X_i X_j \oplus X_k \tag{17}$$

$$Z_k = \overline{X_i}\ \overline{X_k} \oplus \overline{X_j}\ Z_k = \overline{X_i}\ \overline{X_k} \oplus \overline{X_j} \tag{18}$$

The basic symbol of NG reversible gate and its functional table is shown in Fig. 7. The internal logic diagram of the NG reversible gate using conventional and proposed method is illustrated in the Fig. 8 and Fig. 9. The switching activity value of each gate is shown in the Fig.8 and Fig.9. The overall SA value of the NG reversible gate is calculated by adding all of the individual SA values of logic gates. As indicated in the Fig.8 and Fig.9, the overall SA value of a Conventional NG (CNG) gate is 2.7812, while the overall SA value of a NG gate using the proposed technique is 1.0312.

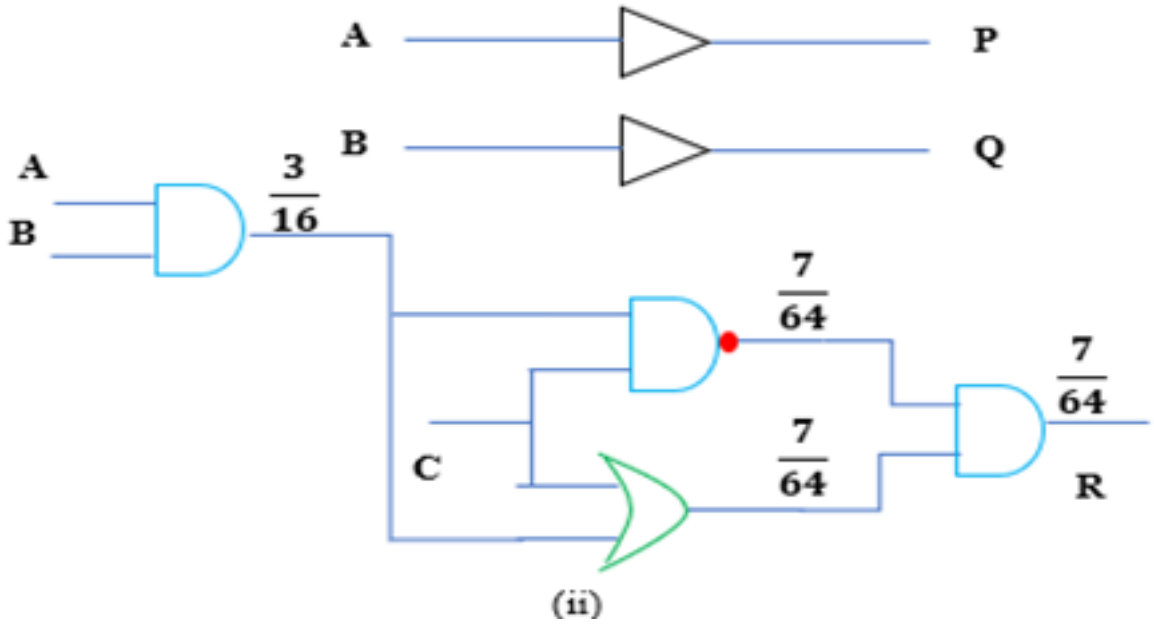
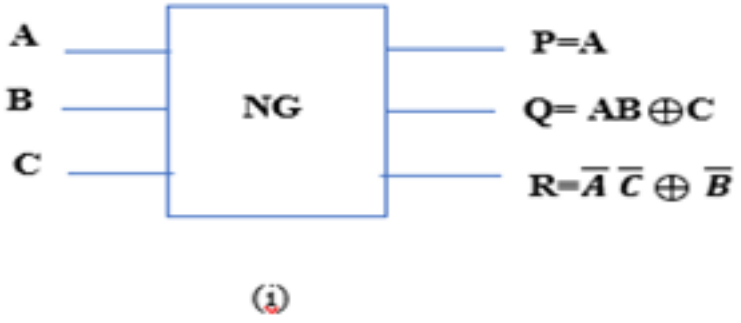


Fig. 6: Logic diagram of proposed TG gate



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

(ii)

Fig. 7: (i) Symbol of NG (ii) Functional table of NG

Table I: Comparison among reversible gates using conventional and proposed method

Name of the Gate	Conventional method				Proposed method			
	Number of NOT Gates	Number of 2-input Gates	Total Cell Count	SA Value	Number of NOT Gates	Number of 2-input Gates	Total Cell Count	SA Value
FG	2	3	5	1.0625	0	3	3	0.5625
TG	2	4	6	1.0156	0	4	4	0.5156
NG	7	8	15	2.7812	0	8	8	1.0312

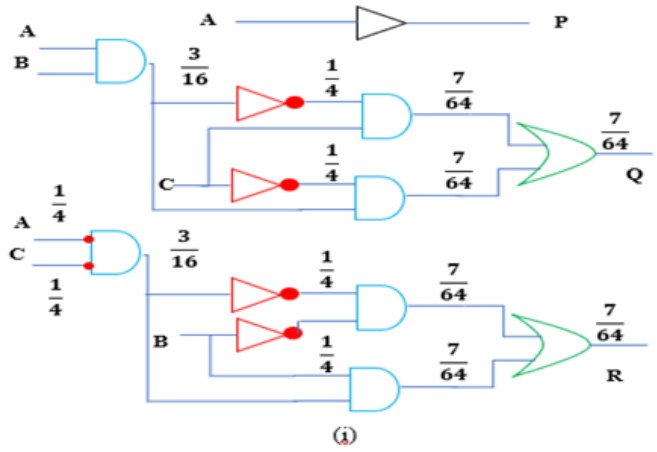


Fig. 8: Logic diagram of Conventional NG gate

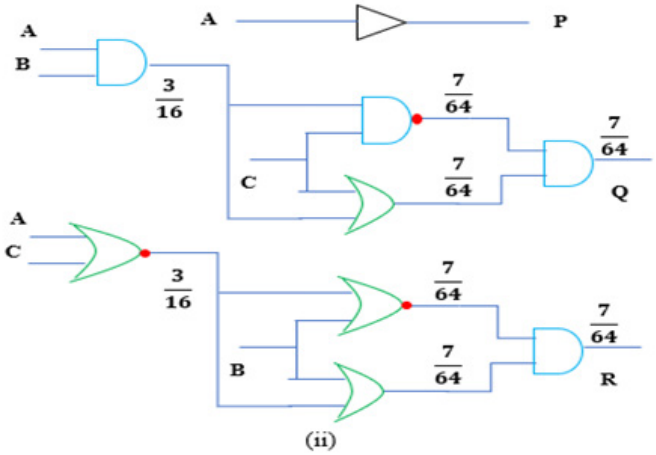


Fig. 9: Logic diagram of proposed NG gate

$$SA_{CNG} = 7 \times \frac{1}{4} + 2 \times \frac{3}{16} + 6 \times \frac{7}{64} \quad (19)$$

$$SA_{PNG} = 2 \times \frac{3}{16} + 6 \times \frac{7}{64} SA_{PNG} = 2 \times \frac{3}{16} + 6 \times \frac{7}{64} \quad (20)$$

The Design Of Reversible Full Adders

The design of full adder is composed of three reversible gates such as FG, TG, and NG. The two inputs A and B are passed through NG gate by making third input as zero. The first output of NF gate is considered as garbage bit, the other two outputs are passed as input to FG reversible gate with Cin bit. The first two outputs of TG reversible gate are passed as input to FG gate. The second output of FG reversible gate is sum output and the first output is considered as garbage output. The output carry bit is obtained from third output of TG gate. The block diagram of reversible full adder is illustrated in Fig.10.

A. The Proposed Reversible Full Adder (PRFA)

The logic diagram of proposed reversible binary full adder is designed for the use of proposed logic diagrams of NG, TG, and FG reversible gates. The total SA value proposed reversible full adder from Fig.3, Fig.6, and Fig.9 is calculated as follows

$$SA_{PRFA} = 2 \times \frac{3}{16} + 12 \times \frac{7}{64} SA_{PRFA} = 2 \times \frac{3}{16} + 12 \times \frac{7}{64} \quad (21)$$

According to theoretical analysis, the comparison among FG, TG, and NG reversible gates is presented in Table I. From the table1 we can find out the proposed method of FG, TG, and NG improved in every aspect such as NOT cell count and switching activity value.

B. Proposed Full Adder without reversible gates

The Proposed Full Adder [1] is designed based on the following Boolean expressions,

$$P = \overline{AB}\,(A + B) P = \overline{AB}\,(A + B) \quad (22)$$

$$S = \overline{PC}\,(P + C) S = \overline{PC}\,(P + C) \quad (23)$$

$$C_0 = PC_i + ABC_0 = PC_i + AB \quad (24)$$

The logic diagram of PFA [1] using equations23, 24, and 25 is shown in Fig.11. The total power dissipation consumed by PFA [1] is 211mW with a delay of 7.106nsec.

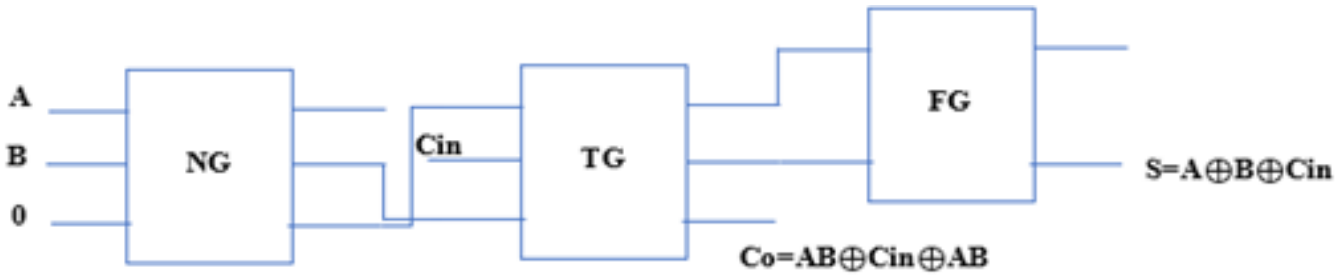


Fig. 10: Block diagram of full adder using reversible gates[2]

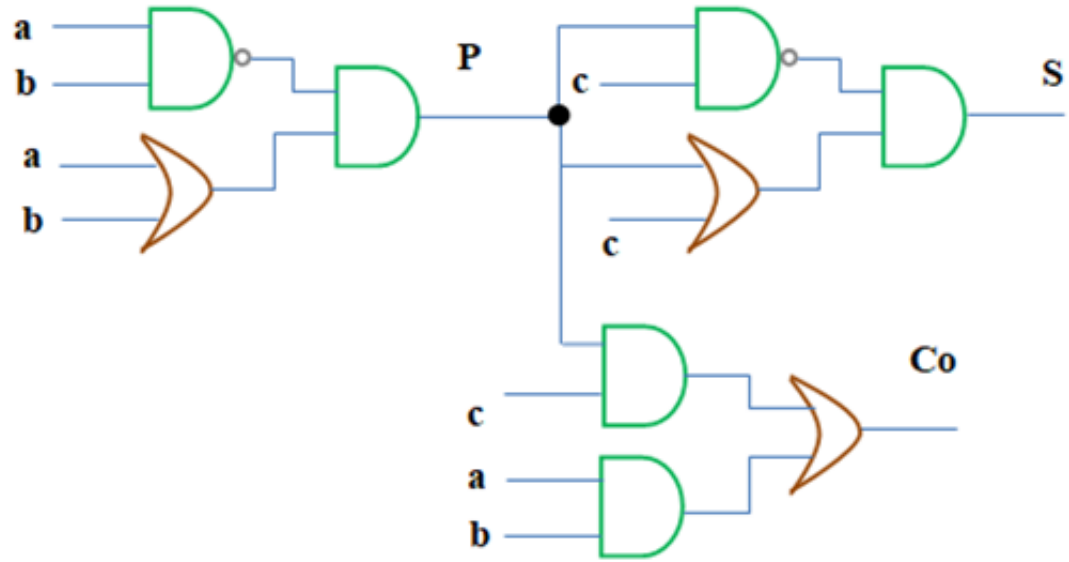


Fig. 11: Logic diagram of PFA [1]

Simulation Results

Functionality of reversible full adder is verified using Xilinx vivado behavioral simulation. Here, we are showing simulation results for two test vectors i.e., 110 and 100. For the above two input combinations, the output waveforms are shown in Fig.12. The simulation tool generated outputs are physically verified on FPGA ZYBOZ7. For this operation, the Verilog code is synthesized and implemented using Xilinx Vivado Zynq 7000 target device XC7Z020clg400 configuration.

The net list is generated after implementation step. This net list file is dumped into the FPGA board. Here, we considered input combination at 110; it means W13 switch is ON, P15 is ON and G15 is OFF are operated by the designer. According to the above input combination M15 LED is activated and M14 is not activated which means when input is 110, the sum output is logic 0 and carry out is logic 1 shown in Fig.13. The implementation result of conventional and proposed FG is shown in Fig.14. From Fig.14 the total power consumed by FG is 194mW, and 22mW using conventional and proposed method followed by delays of 6.486nsec. The implementation results of TG using conventional and proposed method are shown in Fig.15. From Fig.15 the total power dissipated by TG is 226mW, and 151mW using conventional and proposed method followed by delays of 7.027nsec.

The implementation result of conventional and proposed NG is shown in Fig.16. From Fig.16 the total power consumed by NG is 288mW, and 182mW using conventional and proposed method followed by delays of 7.357nsec. The comparison among conventional and proposed reversible logic gates is shown in Table II based on their implementation results. The comparison among conventional and proposed reversible logic gates is shown in Table III based on their performance metrics. The RTL diagram of proposed reversible full adder is shown in Fig.17. The implementation results of proposed reversible full adder are shown in Fig.18. From Fig.18 the total power dissipated by the proposed full adder is 189mW with a delay of 7.203nsec. The overall comparison among FG, TG, NG, and full adders in terms of static power, dynamic power and delay based on implementation results using conventional and proposed methods is shown in Table II and Table IV. After imposing the formula-based evaluation on implementation results, it becomes performance metrics

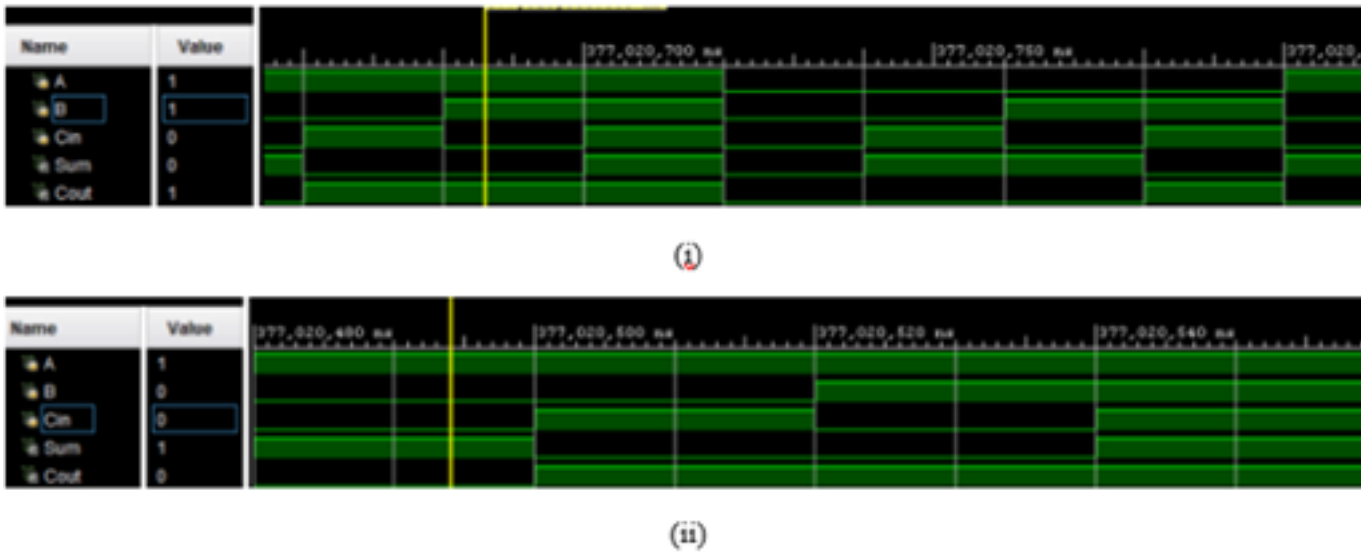


Fig. 12: Simulation results of reversible full adder (i) when input=110 (ii) when input=100

Table II: Comparison among conventional and proposed reversible gates based on implementation results

Name of the Gate	Conventional method			Proposed method		
	$P_{static}P_{static}$ (mW)	$P_{dynamic}$ $P_{dynamic}$(mW)	Delay (nsec)	$P_{static}P_{static}$ (mW)	$P_{dynamic}$ $P_{dynamic}$(mW)	Delay (nsec)
FG	121	73	6.486	120	22	6.486
TG	121	105	7.027	120	31	7.027
NG	122	166	7.359	121	61	7.359

TABLE III Comparison among conventional and proposed reversible gates based on performance metrics

Name of the Gate	Conventional method					Proposed method				
	P_{avg} P_{avg} (mW)	$P_{dynamic}$ $P_{dynamic}$ (mW)	FOM (nJ)	PDP (nJ)	EDP ($\times 10^{-21}$ $\times 10^{-21}$ J)	P_{avg} P_{avg} (mW)	$P_{dynamic}$ $P_{dynamic}$ (mW)	FOM (nJ)	PDP (nJ)	EDP ($\times 10^{-21}$ $\times 10^{-21}$ J)
FG	97	73	0.629	0.473	3.07	71	22	0.460	0.142	0.92
TG	113	105	0.794	0.737	5.18	75.5	31	0.530	0.217	1.52
NG	144	166	1.059	1.221	8.98	91	61	0.669	0.448	3.29

Table IV: Comparison between PFA [1] and PRFA based on implementation results

Name of FA	$P_{static}P_{static}$ (mW)	$P_{dynamic}$ $P_{dynamic}$ (mW)	Delay (nsec)
PFA [1]	121	90	7.106
PRFA	121	68	7.203

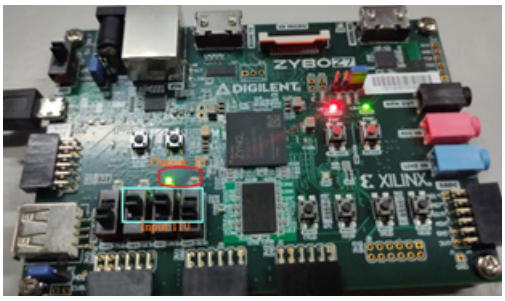


Fig. 13: Verification of Simulation results on FPGA board when input =110

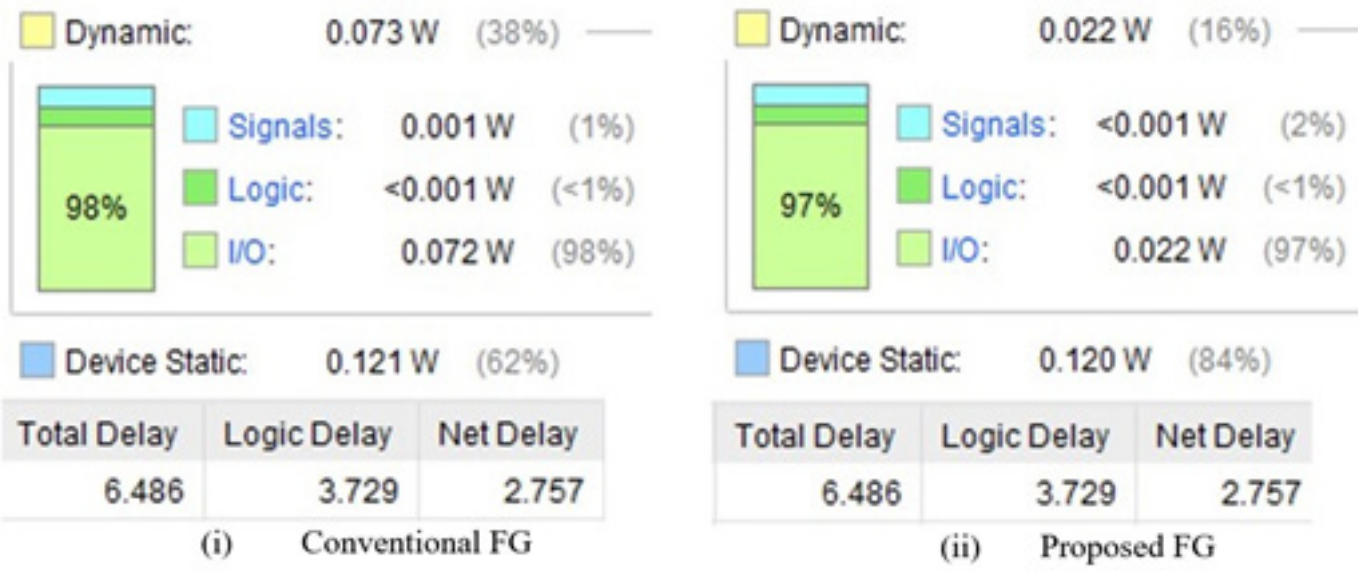


Fig. 14: Implementation Results of FG gate using Conventional and Proposed method

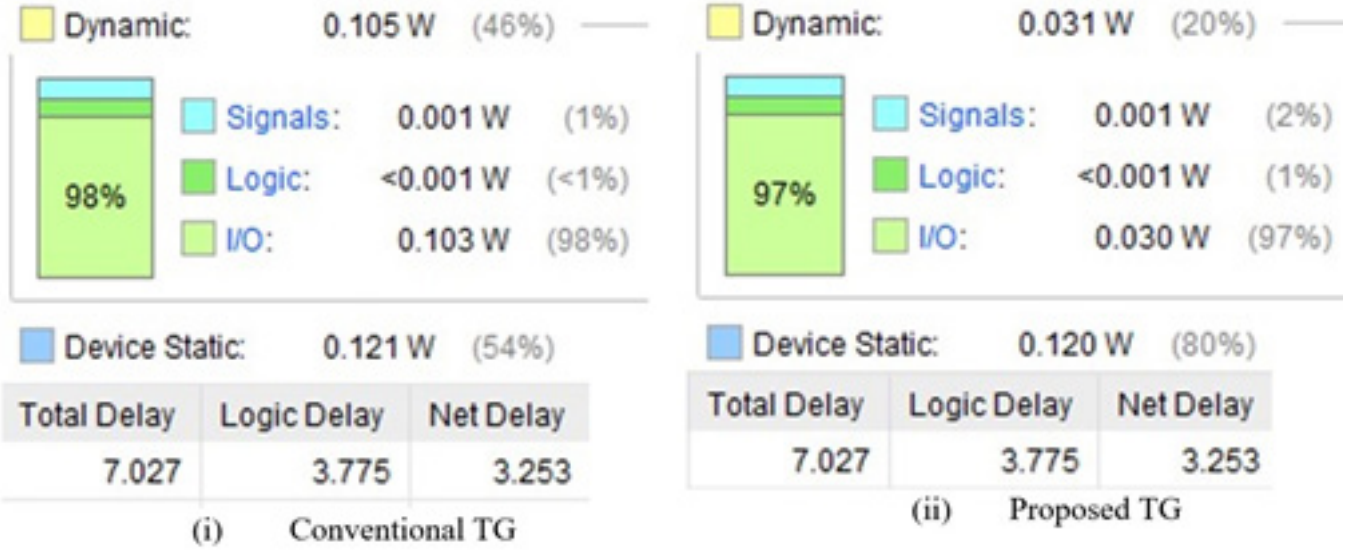


Fig. 15: Implementation Results of TG gate using Conventional and Proposed method

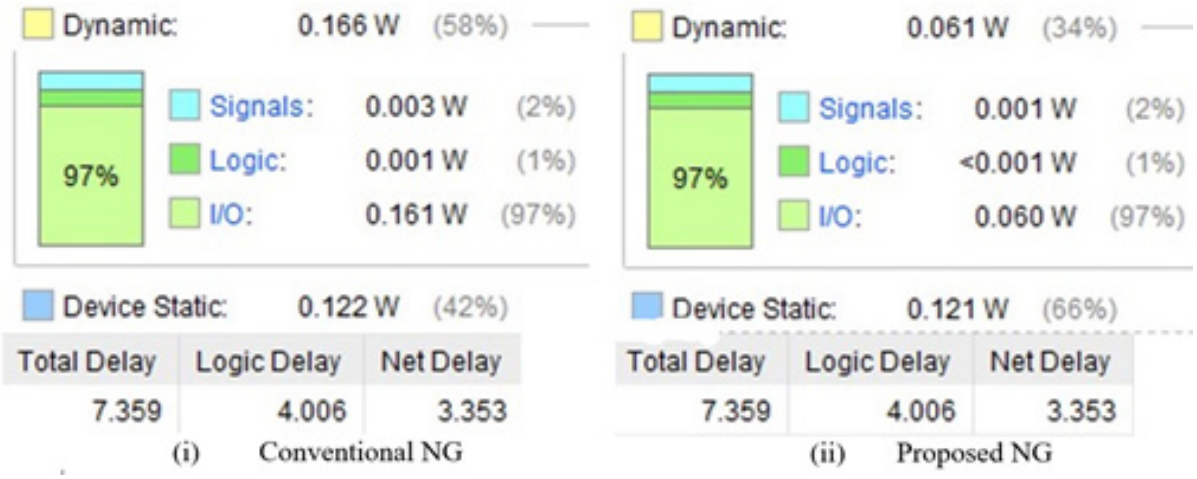


Fig. 16: Implementation Results of NG gate using Conventional and Proposed method

Table V: Comparison between PFA [1] and PRFA based on Performance metrics

Name of FA	P_{avg} P_{avg} (mW)	$P_{dynamic}P_{dynamic}$ (mW)	FOM (nJ)	PDP (nJ)	EDP ($\times 10^{-21}\times 10^{-21}$J)
PFA [1]	105.5	90	0.749	0.639	4.54
PRFA	94.5	68	0.671	0.483	3.43

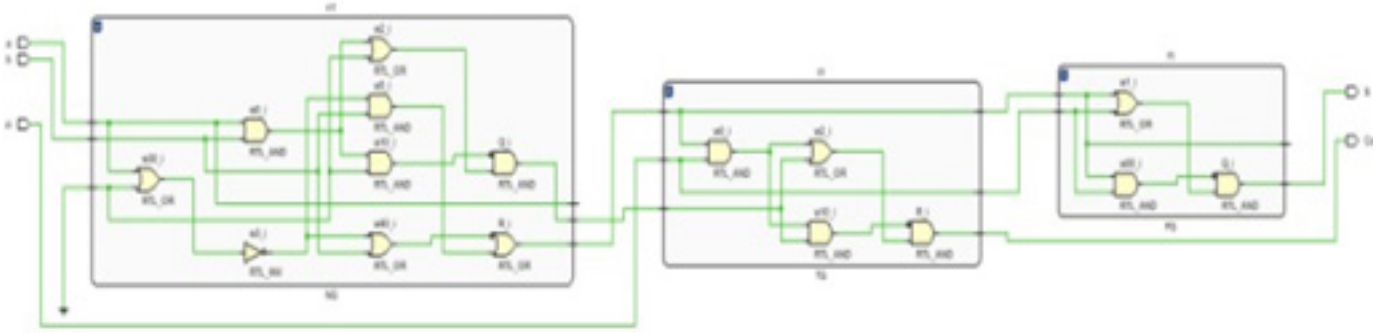


Fig. 17: RTL diagram of Proposed Reversible FA

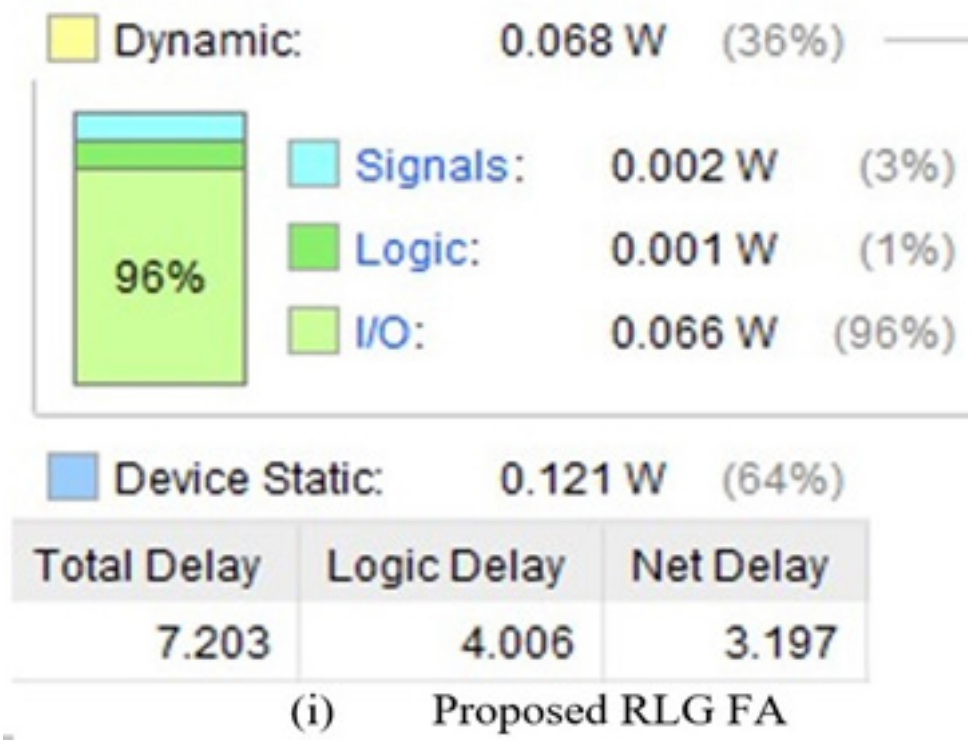


Fig. 18: Implementation results of Proposed RFA

of designed circuits. In this paper, we concentrated on the energy delay product of all designs. The energy delay product of FG, TG, NG, and reversible full adders is improved using the proposed method over the conventional method.

The performance metrics of all designs are presented in Table III and Table V. From the Table III and Table V, we found that the proposed method improved in terms of Figure of Merit, power delay product, and Energy delay product over the conventional method. The performance metrics of FG, TG, NG, and full adders are evaluated for conventional and proposed reversible gates. The graphical representation of comparison among improvement in performance metrics of reversible gates using conventional

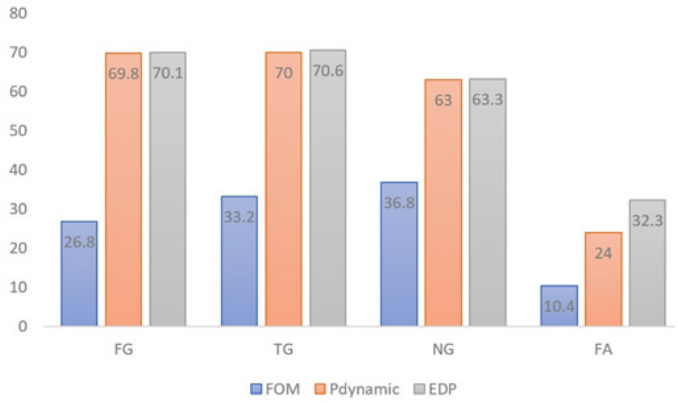


Fig. 19: Performance improvement among reversible gates and full adder

and proposed method is shown in Fig.19.The performance metrics of proposed reversible full adder are evaluated from equation 4, 5, and 6. The comparison between PRFA and PFA is shown in Table IV based on their implementation results. The comparison between PRFA and PFA is shown in Table V based on their performance metrics.

Conclusion

In this paper, conventional and proposed reversible gates and full adders are synthesized using the Xilinx Vivado design suite for the Zynq-7000 family of devices. We present a reversible FG, TG, NG gates with few cells and lower dynamic power dissipation than existing designs, as well as lower EDP. The switching activity idea has been implemented for a novel architectural level design that minimizes switching activity factors to reduce the dynamic power consumption and EDP of reversible full adders. The logic decomposition approach was created to further reduce the power consumption of the reversible binary full adder. According to FPGA implementation results, the proposed reversible full adder consumed 10.4% less FOM, and 32.3% less energy delay product than the PFA [1]. The simulation tool generated outputs are physically verified on FPGA ZYBOZ7 board. As a result, switching activity-based hybrid adders can be used in a variety of real- time applications, such as CPUs, crypto processors, and security systems. The proposed design is flexible enough to work together with a wide range of digit sizes and input bits. In this work, we only design the logic circuits of the proposed hybrid adder, allowing physical implementation and simulation to be discussed later.

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