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Fundamental Data Seperator using Threshold Logic at Low-Supply Voltages

Q. Hugh[1], Freddy Soria[2], C.C. Kingdon[3], Robert G. Luedke[4]

Robotics and Automation Laboratory Universidad Privada Boliviana Cochabamba, Bolivia

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Abstract

In digital terminology, a device that compares two numbers which are represented in binary format and determines whether one of the two inputs are lesser than or equal to or greater than the other input is called a comparator. Comparators are generally used in Central Processing units (CPUs) and microcontrollers. In this project, a 2-bit magnitude comparator is designed with 18nm FinFET technology. FinFET technology is used to overcome the drawbacks associated with CMOS technology like channel length, power consumption, delay and area of transistors, etc. The proposing magnitude comparator is compared with the existing CMOS comparator in terms of power and delay. Schematic circuit diagrams of greater than, equal to and lesser than circuits have been simulated using the Cadence Virtuoso tool. Power and delay values are calculated and plotted for different values of supply voltage ranging from 0.1v-1.0v. LVT (Low Voltage) and HVT (High Voltage) analysis are performed separately. FinFET comparators can be used where a fast switching rate is required, to improve the efficiency of control devices and to make devices compact.

Author's e-mail: Hugh.q@upb.edu, soria.fred@upb.edu, kingdon.cc@upb.edu, robert.g.lu@upb.edu

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Introduction

Most of the arithmetic components in digital systems use comparator as a basic element or component. Not only in digital systems, comparators are also used in many hardware components for various applications due it its efficient performance, packed component, and cost factor, thus playing a major role in various components and circuits. These comparator components can be utilized individually when the main purpose is for comparing or these components can be integrated into various circuits where comparison is a small part of any application. Comparators are mainly used in governing and inspecting processes and these analyses are used according to the requirement.[1-7] They are widely used in limit setting equipment like the maximum or minimum temperature that something can withstand, in other words, the tolerance of a component. This means, the range can be established through comparator. Various control systems mainly use comparator as the basic element. Comparators are also used in quality assurance of products. Quantity measurements like weighing machines make use of comparators. It is also used in image processing and signal processing. The applications of comparator are many thus; they are used in daily life. They are also used in operating motors like Brushless Direct Current motors. Comparators are used for efficiency checking of components in less time. Analog to digital conversions digital communication receivers and dc-dc converters also use comparators.[8-12] Comparators are also used in different generators: zero-crossing detector, window generator, time marker generator and phase detector. Applications of comparator are many. The operation of comparator also deals with only three outputs viz. greater than, lesser than or equal. At no case, all the three outputs become true, in other words, if one output is true among the three outputs, the remaining two outputs must and should become false.[13]

Power and delay are the two major concerns when it comes to analyzing the performance of a comparator. Various methods have been proposed to enhance the performance statistics of comparators.

The existing models were fabricated using different logics of MOSFET technology .[14-17] These logics include CMOS with domino logic, coupler logic etc. Different logics are incorporated with the same technology MOSFET to decrease the power consumption, increase the speed of operation and reduce the area of transistors. In VLSI, reducing all the factors is not possible, that is, we can only reduce one parameter at a time. Based on the application or the requirement, the associated factors can be reduced. CNTFET is also an existing technology. It stands for Carbon Nano Tube Field Effect Transistor. It uses single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon as used in MOSFET structure. This technology is more advantageous when compared to CMOS technology as they are reliable and can withstand high temperatures. There are few common drawbacks that are associated with the existing technologies. Channel length is more, thereby increasing the area of the chip. Due to increased area, the delay will also be more which considerably decreases the speed. The drive current is also less in the existing technologies.[18,19]

Due to the drawbacks of the existing technology, this project is aimed to overcome the drawbacks with the help of new technology known as FinFET. FinFET stands for Fin Field Effect Transistor. In other words, FinFET is a multi-gate transistor. 18nm is the channel length between source and drain. FinFET technology has many advantages when compared with the existing technologies. Many types of FinFET are available. Drive current is high. Channel length is very less. Delay will be less, thereby increasing the speed of operation. Suppressed short channel effect is present. As the channel length is very less, a greater number of FinFETs can be embedded on a given area. For Very Large-Scale Integrated Circuit designs (VLSI), we generally use Cadence Virtuoso tools for simulation and results. It is designed to help the users in creating and manufacturing robust designs to explore, analyze, and verify a design against design goals so that one can maintain design intent throughout the design cycle. SoC design engineers mainly use cadence products to move a design into packaged silicon or emulation hardware or for FPGA prototyping. In Cadence, we use FinFET libraries and associated transistors to implement analyze the design of comparator.[20-22]

This paper deals with the introduction of comparators and their uses. The existing technologies like MOSFET and CNTFET are compared. It also describes about the drawbacks of the existing technology which can be dealt with the new technology FinFET. The advantages of FinFET play a major role in the enhancement of VLSI. The detailed explanation about the structure of FinFET is explained. This literature survey forms a basis for the methodology to be implemented and for analyzing the results obtained through simulation. The block diagram and the functionality of comparator are explained through truth table. The 2-bit magnitude comparator using n-channel transistor logic is explained by considering different cases like greater than, lesser than and equal to as a part of methodology. The 2-bit magnitude comparator circuits are simulated to obtain transient response. Power and delay values are obtained for lesser than, greater than and equal to circuits. The behavior of power and delay are noted and plotted by varying the supply voltage from 0V to 1V for both LVT and HVT configured transistors in FinFET technology. In the end, the conclusions and future scope of this project is obtained through simulation results. It also explains about the drawbacks of FinFET which can be studied further. References and supporting materials to carry out the project are added at the end of the paper.

FinFET Characteristics and Modeling

FinFET stands for Fin Field Effect Transistor. It is also called as multi-gate MOS transistors. In FinFET, the conducting channel is wrapped by silicon wafer which forms the substrate for the transistor. The channel length is determined by the thickness of the device. It is a non-planar transistor. It generally consists of 2 gates. This double gate transistor is either based on silicon wafers or SoI (Silicon on Insulator). The base in which it gets fabricated determines the type of FinFET. To suppress or reduce the off-state leakage current and to allow good amount of current in drive state or ON state we use multi gates in FinFET. These multi gates also help to control the channel electrically. The performance issues on planar transistors can be overcome through FinFET technology. FinFET plays a major role in ULSI (Ultra Large Scale Integrated Circuits) products.[12, 13]

There are mainly two types of classification in FinFET: 1.Short Gate (SG) which are also called as 3T (three terminal) FinFETs. 2. Independent Gate (IG) which are also called as 4T (four terminal) FinFETs. The single gate transistor is classified in two types: 1. Bulk FinFET 2. SoI FinFET.

FinFET is the latest technology in VLSI domain. Because of its multi gate structure, it finds the following advantages: Drive current is more, Channel length is short implies that the design will be compact; Power

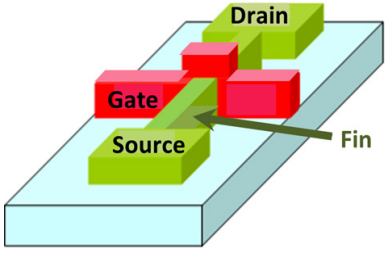


Fig. 1: Structure of FinFET

consumption is less; Better performance; High speed. It is used in the processors due to its compactness as many FinFET transistors can be used within a specified area. Samsung Galaxy S6 uses FinFET technology in its processors. In future, the channel length will be decreased even more to FinFET 10nm. The given table represents the symbols, parameters and values associated with double gate FinFET.[15, 20]

Proposed Comparator Block Using FinFET Models

In the block diagram Fig. 2, A and B are 1-bit binary inputs and L (less than), E (equal to) and G (greater than) are three outputs based on the combination of inputs given.

G1 = A' *G2 = B'*
G3 = A'B *G4 = AB'*
G5 = (A'B + AB')'

The logic gate representation of magnitude comparator can be better represented and implemented using transistor level models. CMOS transistor which is a combination of both P-FINFET and N-FINFET is used to implement logic gates. We can also have only P-FINFET logic or only N-FINFET logic based on the requirement and input-output conditions. Transistor level implementation is faster, suitable for larger designs and can handle longer simulation. In this project, FinFET technology is used for transistors. 2-bit magnitude comparator with inputs A0, A1, B0, B1 where A1, B1 represent MSB bit and A0, B0 represent LSB bit for the two numbers A and B are considered.

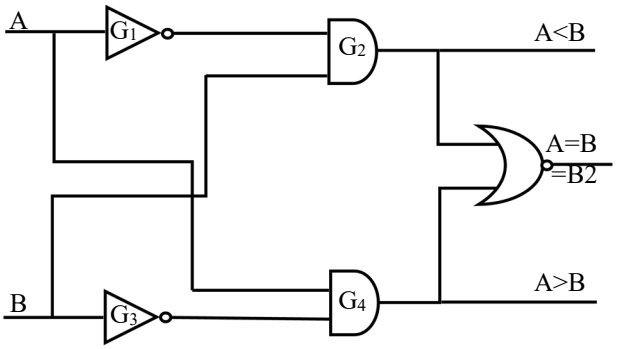


Fig. 2: Block diagram of 1-bit magnitude comparator

Lesser than functional circuit

Lesser than functional implementation for 2-bit magnitude comparator as shown in Fig. 3 is represented in N-FINFET logic to represent A<B.

Equal to functional implementation for 2-bit magnitude comparator as shown in Fig. 4 is represented in N-FINFET logic to represent A=B.

Greater than functional implementation for 2-bit magnitude comparator as shown in Fig. 5 is represented in N-FINFET logic to represent A=B.

Consider A and B are 2-bit binary inputs with A1, B1 as MSB bits and A0, B0 as LSB bits. The following expressions are:

L = A1'B1 + A0'B0B1 + A1'A0'B0

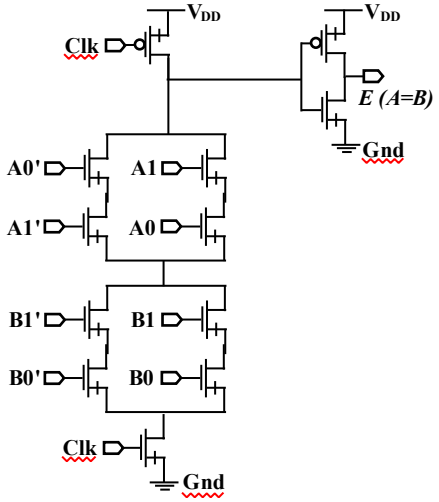


Fig. 4: Equal to functional circuit of 2-bit magnitude comparator

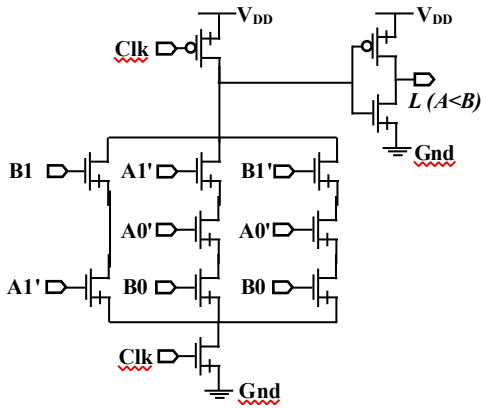


Fig. 3: Lesser than functional circuit of 2-bit magnitude comparator

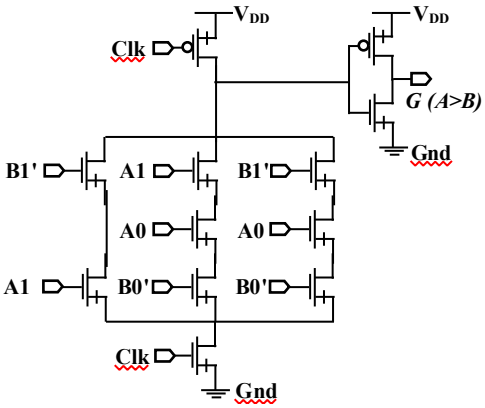


Fig. 5: Greater than functional circuit of 2-bit magnitude comparator

E = (A0B0 + A0'B0') (A1B1+A1'B1')
G = A1B1' + A0B1'B0' + A1A0B0'

Simulation Results and Experimental Findings of the Proposed Work

Lesser than circuit design

Figure 6 represents schematic diagram of 2-bit lesser than circuit with LVT configured FinFET transistors. We can replace LVT transistors with HVT or NVT for comparison purposes. Inverter is a symbol created for another schematic diagram which is a pair n-LVT and p-LVT to inv

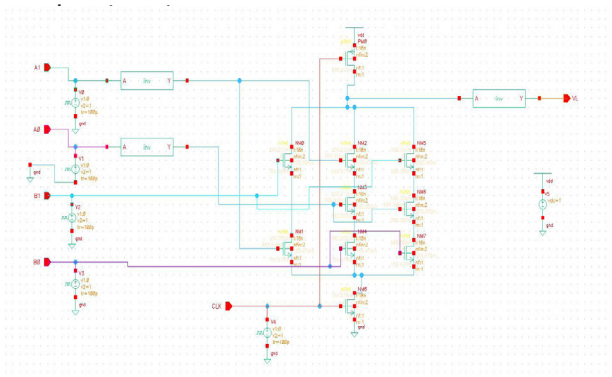


Fig. 6: Schematic diagram of 2-bit lesser than circuit

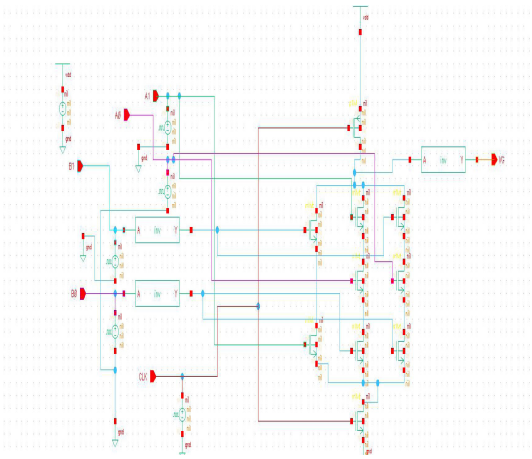


Fig. 8: Schematic diagram of 2-bit greater than circuit

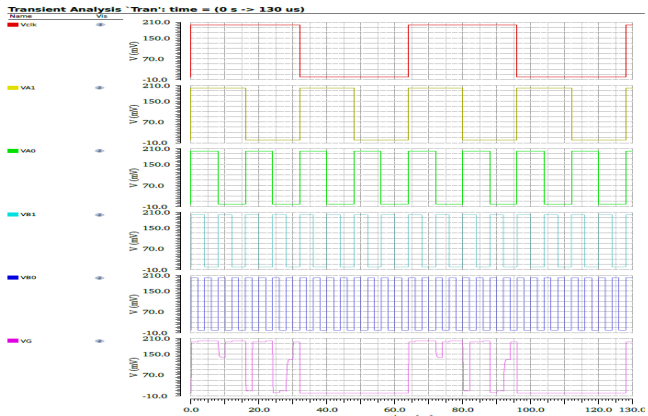


Fig. 10: Transient response of 2-bit equal to circuit

Equal than circuit design

Figure 7 represents schematic diagram of 2-bit equal to circuit with LVT configured FinFET transistors. We can replace LVT transistors with HVT or NVT for comparison purposes. Inverter is a symbol created for another schematic diagram which is a pair n-LVT and p-LVT in to invert the given input.

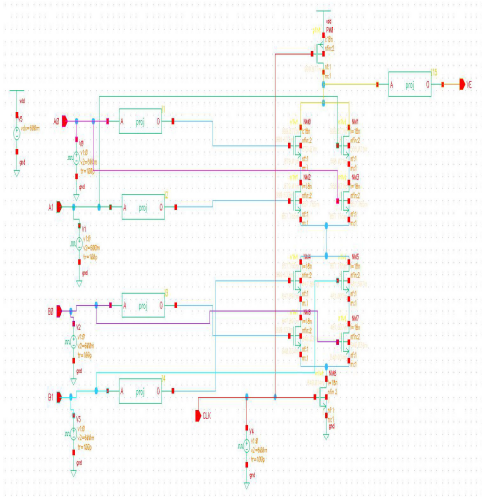


Fig. 7: Schematic diagram of 2-bit equal to circuit

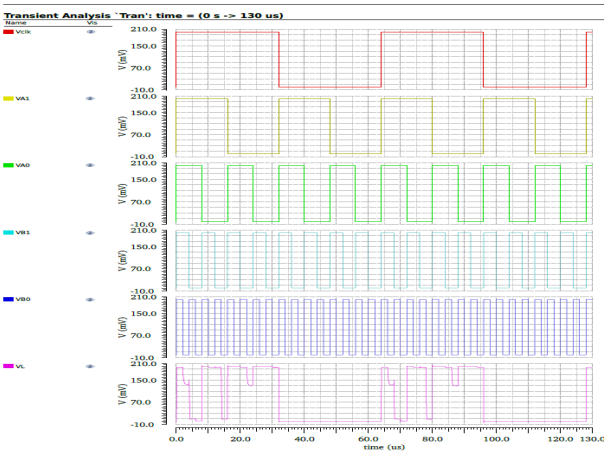


Fig. 9: Transient response of 2-bit lesser than circuit

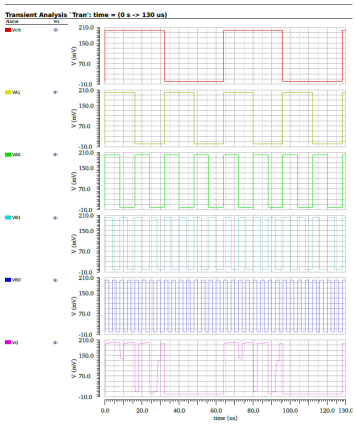
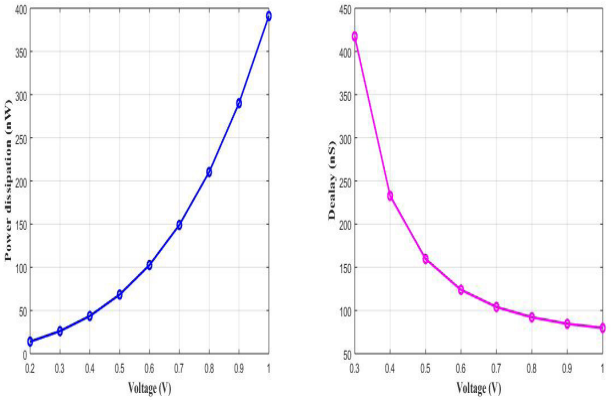


Fig. 11: Transient response of 2-bit greater than circuit

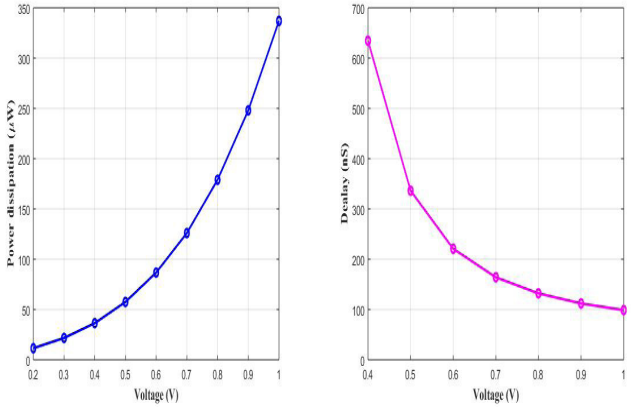
Greater than circuit design

Figure 8 represents schematic diagram of 2-bit greater than circuit with LVT configured FinFET transistors. We can replace LVT transistors with HVT or NVT for comparison purposes. Inverter is a symbol created for another schematic diagram which is a pair n-LVT and p-LVT to invert the given input.



(a) (b)

Fig. 12: Equal to circuit at LVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot



(a) (b)

Fig. 13: Equal to circuit at HVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot

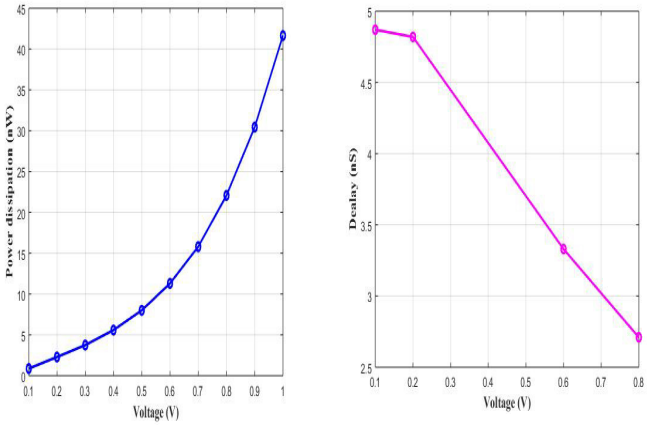
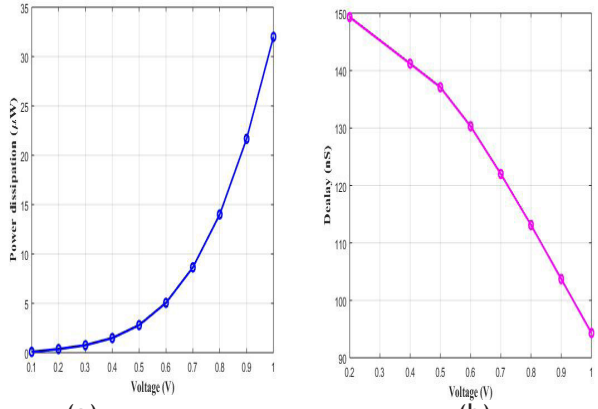
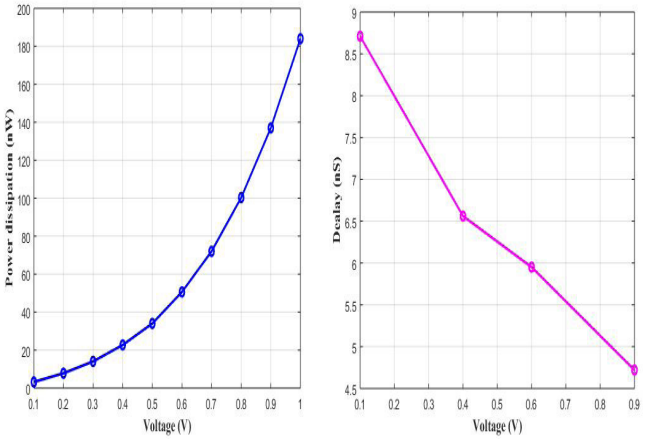


Fig. 14: Lesser than circuit at LVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot



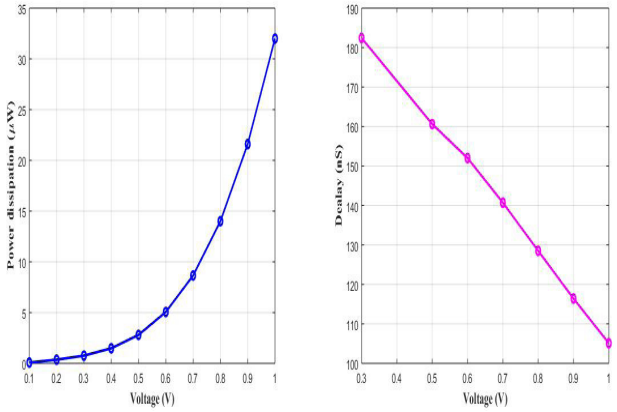
(a) (b)

Fig. 15: Lesser than circuit at HVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot



(a) (b)

Fig. 16: Greater than circuit at LVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot



(a) (b)

Fig. 17: Greater than circuit at LVT (a) Power vs Voltage plot (b) Delay vs Voltage Plot

Transient response plot of lesser than circuit

Figure 9, Figure 10 and Figure 11 are the simulation results obtained using spectre models for FinFET 18nm technology. The above transient response represents the overall functionality of comparator.

Experimental Findings of the Proposed Work

Power and Delay plots

From the figures: Figure 12, Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17: As the voltage increases, the power increases and as the voltage increases, the delay decreases for both LVT and HVT configurations. We can also infer that the delay for LVT is less when compared to HVT and the power consumption for LVT is more when compared to HVT.

Conclusion

In this paper, a 2-bit magnitude comparator is designed with 18nm FinFET technology. FinFET technology is used to overcome the drawbacks like channel length, power consumption, delay, and area of transistors, etc. The proposing magnitude comparator is compared with the existing CMOS comparator in terms of power and delay. Schematic circuit diagrams of greater than, equal to and lesser than circuits have been simulated using the Cadence Virtuoso tool and spectre models. Power and delay values are calculated and plotted for different values of supply voltage. LVT (Low Voltage) and HVT (High Voltage) analysis are performed separately. The power values for LVT and HVT are increasing as the voltage increases. The power consumption of LVT is more when compared to HVT. The delay decreases as we increase the voltage levels. Delay for LVT is less when compared to the delay of HVT. The power-delay product is efficient when compared to the existing technologies like MOSFET. The distortions obtained at the transient response can be reduced by using suitable capacitors and other combination of logics associated with FinFET. Different types of FinFET can be used to obtain more efficient results. Normal threshold voltage can also be analyzed for comparison purposes.

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