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Fundamental Code Converter Block Design using Novel CMOS Architectures

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Abstract

In this paper, a decoder is designed to convert the binary data to thermometer code. This paper involves a 4-bit decoder such that it consists of 4 inputs and 15 outputs. This decoder is designed in two different ways; IG-LP mode decoder and multiplexer based decoder. The IG-LP mode decoder is designed using the truth table of binary to thermometer decoder. This logic based decoder consists of 15 different logics, which are developed using the FinFET technology. The multiplexer based decoder is designed using 2:1 multiplexer circuits. These 2:1 multiplexers are also designed using FinFET technology. FinFET 18nm spectre models are used in cadence to design and simulations of proposed circuits. The performance validation has done with respect to power consumption, delay, PDP and EDP of both the designs.

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Introduction

Decoder is an electronic circuit that is used to convert the input binary data into another form of data. Every output data that is obtained through the decoder depends upon the unique input data. A decoder consists of multiple inputs and outputs, which makes their role crucial in ICs. There are many types of decoders, where each decoder has its application. In this paper, a decoder is designed in such a way that it converts the binary data to thermometer data.[1-9] A thermometer code relates the output produced by the thermometer. This decoder consists of x-bit binary data and 2x-1 thermometer data. This decoder design can be used in DAC, that it can be used in ASICs. Figure 1 shows the graphical representation of thermometer codes from values 0 to 7.[1-13]

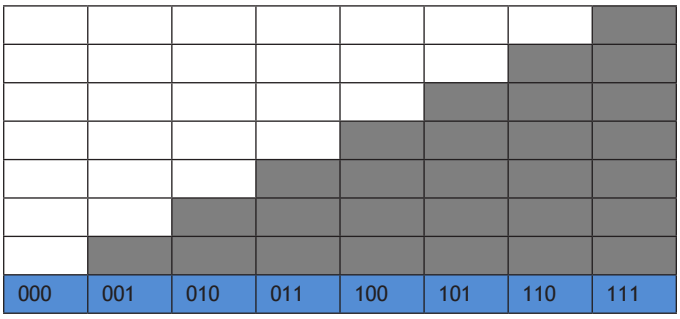


Fig. 1: Thermometer codes graphical representation

For example, an output 01101 is invalid in thermometer code Here with the help of truth table, a logic based binary to thermometer decoder can be designed. From the Fig. 1, as the binary value increases, the thermometer code changes from low to high, which resembles the function of a thermometer. Using this logic, a decoder is designed, such that it converts the binary data to the corresponding thermometer output data. Decoders are the combinational circuits that are used in analog to digital converters, seven-segment displays and memory address decoding.[14-24]

In the past few years, various decoder designs arrived, which has their own advantages and disadvantages. The binary decoders are the decoders that are used to convert the coded inputs to coded outputs. Some of the ICs developed using the binary decoders are, IC-74138 is a 3:8 line decoder, IC-74154 is a 4:16 decoder and IC-7442 is a BCD to decimal decoder. Also using reversible logic gates, decoders are developed. The decoder that converts the binary data to thermometer data is also designed previously using the binary decoding technique. Figure 2 represents conversions of the existing circuit of binary to thermometer decoder.[25-35]

Specifically, when the decoders are designed using the direct implementation of logic gates, the cost and the complexity of the design gets increased. Also using the direct implementation of logic gates consist large number of transistors at transistor level thereby increasing the power consumption of the circuit. To overcome these disadvantages, FinFET technology is used. As FinFETs have lower threshold voltage, they are operated at low voltages, which is an added advantage.[36-39]

This paper mainly deals with the decoder that converts the binary data to thermometer data, which can be used in the Digital-to-Analog converters. This decoder is designed in two ways to analyze its efficiency. One design involves the IG-LP mode and other design involves multiplexer. To make an efficient use of this decoder, it is designed using the FinFET technology. FinFET technology results in the reduction of leakage power, power consumption and delay. Here particularly the FinFET 18nm technology is used to reduce the chip area which plays a crucial role in integrated circuits. In the next section the working process, applications and advantages of FinFET technology are provided. Later the block diagram of the decoder is illustrated with all its internal circuit diagrams. In the results section, the transient response are included and analysis is carried out for power, delay, PDP, EDP for both the designs and are compared in terms of efficiency. The future works are demonstrated in conclusion section for further development.[17-21]

FinFET Characteristics and Modeling

A FinFET also called as the fin field-effect transistor is a multi-gate device that is used in the design of modern processors. Figure 3 represents the diagram of double gate FinFET device. There are two types of FinFETs. They are the SG mode and IG mode. In SG mode the gate terminals are shorted, thus it acts as a three terminal device. The terminals are not shorted in IG mode which is why they have four terminals. In this paper this IG-LP mode is used for designing the decoder. This IG-LP mode is particularly used to reduce the area and leakage power consumption. Using the equations obtained from the truth table of binary to thermometer decoder the IG-LP logics are developed. The design and analysis for binary to thermometer decoder in this technique are carried out using the Cadence virtuoso tool.[17,18]

This FinFET device came into existence due to the continual increase in integration. In this device, the thickness of the fin decides the effective channel length. To reduce the short channel effect, leakage current and threshold voltage, FinFET technology is evolved. The integrated circuits that are designed using the FinFET technology resulted in the low power consumption, low static leakage current and increase in operating speed. The working principle of a FinFET is very similar to a conventional MOSFET. The MOSFET can function in two modes, namely enhancement mode and depletion mode. When there is no

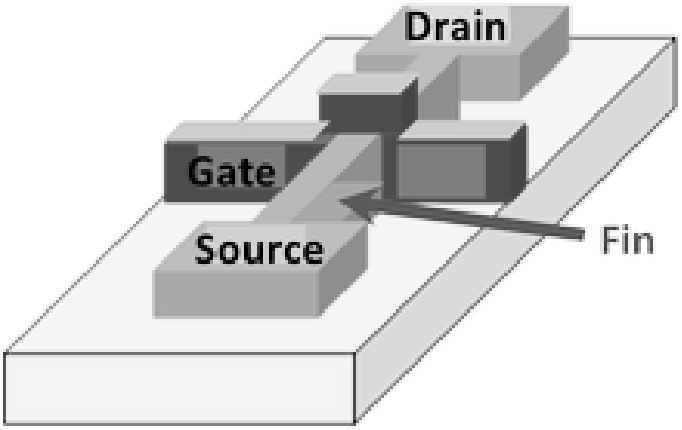


Fig. 3: Diagram of a Double Gate FinFET device

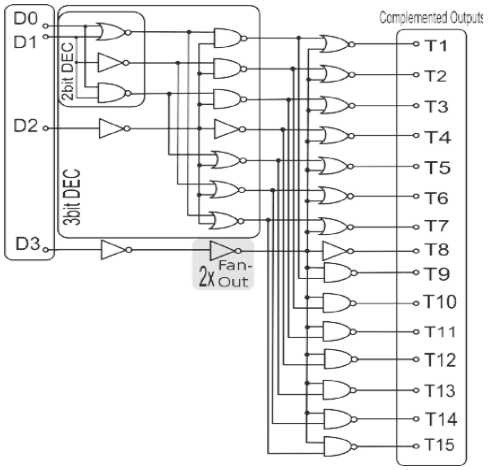


Fig. 2: Existing circuit of Binary to Thermometer decoder[5]

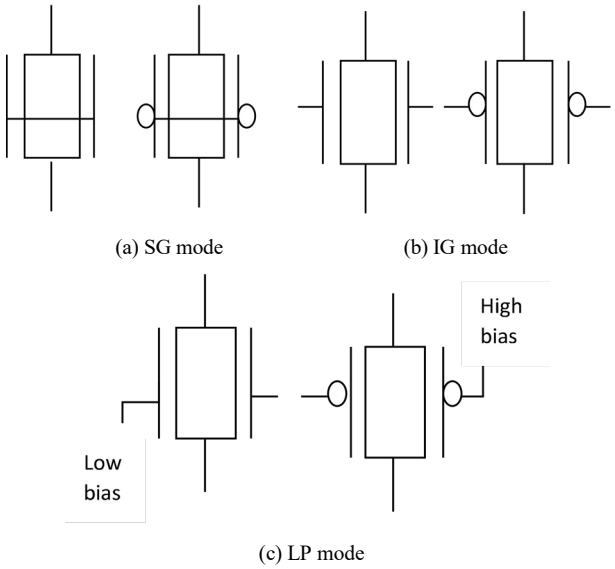


Fig. 4: Different modes in FinFET technology

voltage at the gate terminal, the channel exhibits maximum conductance. The conductivity of the channel reduces when the voltage changes from negative or positive. When the voltage at gate terminal is more, the device conducts more in enhancement mode than the depletion mode. There are various modes in FinFET technology. They are the IG mode, SG mode and LP mode. Figure 4 represents the different modes in FinFET technology.[15-21]

Figure 4(a) represents the SG mode, Fig. 4(b) represents LP mode and Fig. 4(c) represents IG mode. Each mode has its own advantages. In IG mode, the front and back gate are provided with two different input voltages, thus the transistor in this mode consists of four terminals. In IG mode the complexity of the circuit gets reduced but delay is more compared to CMOS. Using SG mode resulted in better drive strength, as two gates of the transistor are shorted making it more efficient. But the primary requirement of the VLSI technology is to reduce the power consumption and area of the circuit. In this case IG-LP mode is used to meet these requirements.

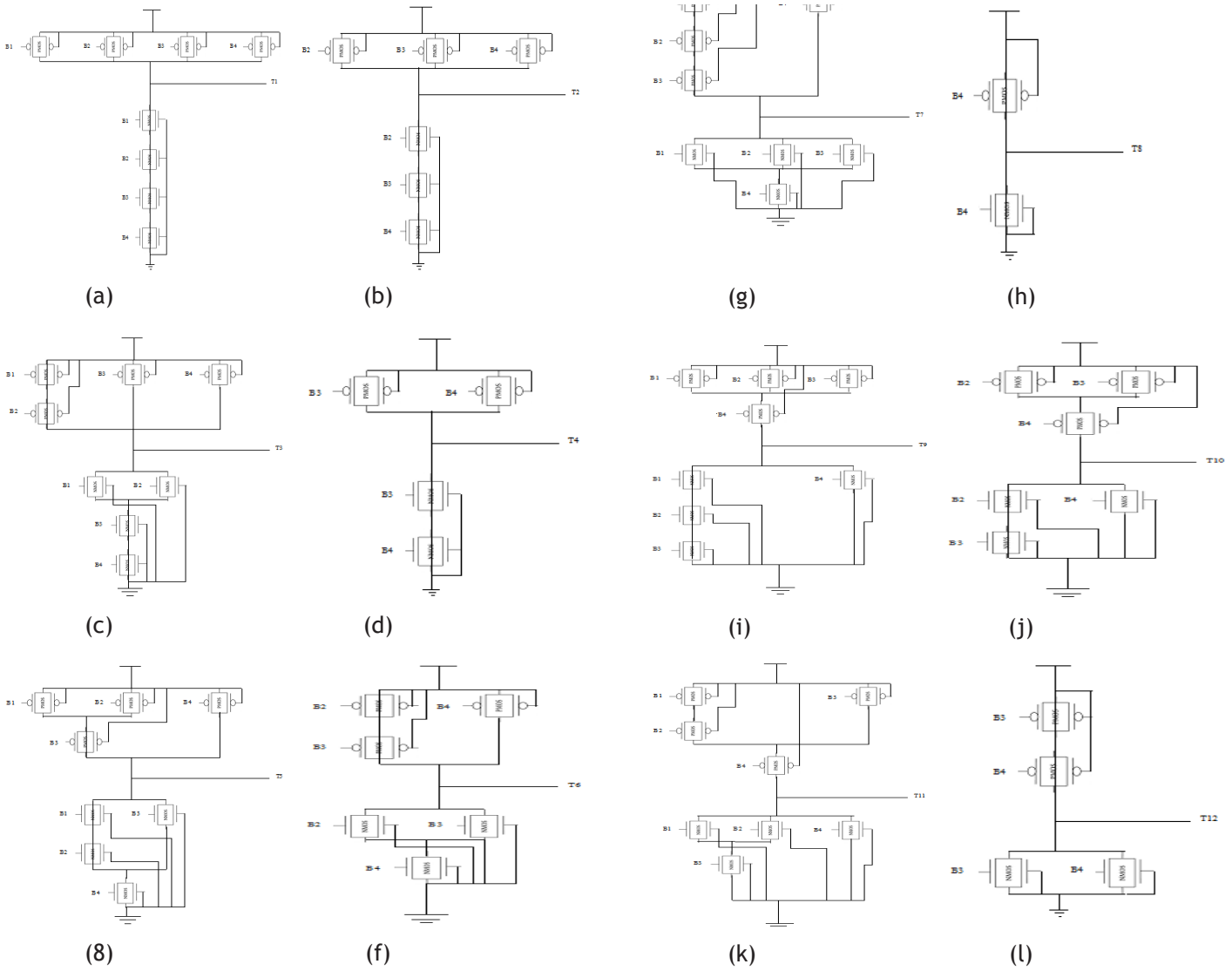
Proposed 4-Bit Decoder Block Using FinFET Models

In this section, the decoder design is illustrated in two methods. In the first method, the decoder is designed using the IG-LP mode logic. These design consists of 15 symbols, each comprise of its own logic. The circuit diagrams of 15 symbols are demonstrated below.

The Figure 5, 15 symbols are merged to form the decoder design. The block diagram of the decoder design using the IG-LP mode is demonstrated in Fig. 5..

In Fig. 6, all the 15 symbols are grouped into a single circuit, collectively forms the logic-based binary to thermometer decoder. Each symbol consists of its own logic that and is implemented using the truth table [39].

In figure 4, all the 15 symbol circuits that comprises of IG-LP mode are merged together and sufficient inputs are provided. The inputs provided here are the pulse voltages. The outputs of each symbol are plotted using the Cadence Virtuoso tool. The second method of decoder



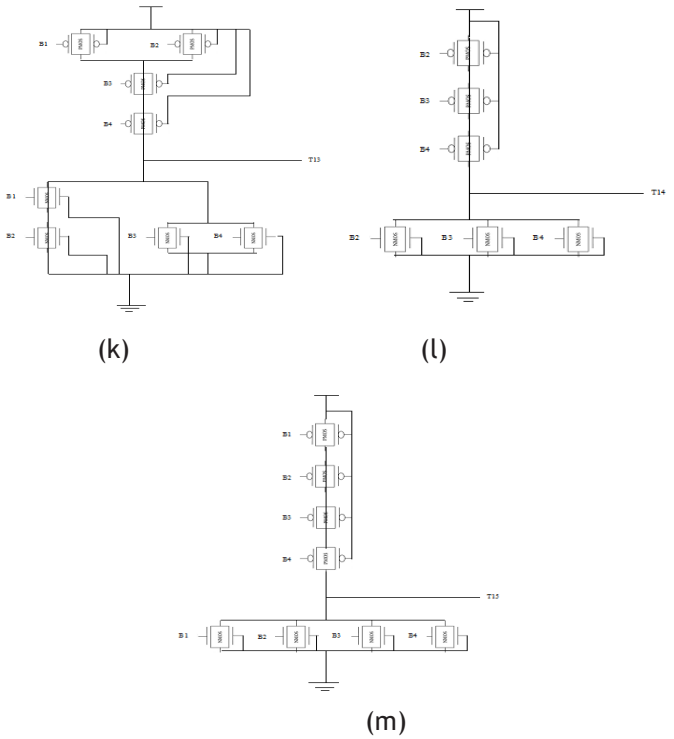


Fig. 5: Logic circuit for symbols of T1 to T15

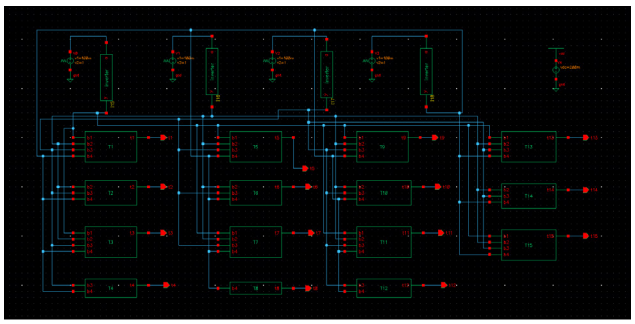


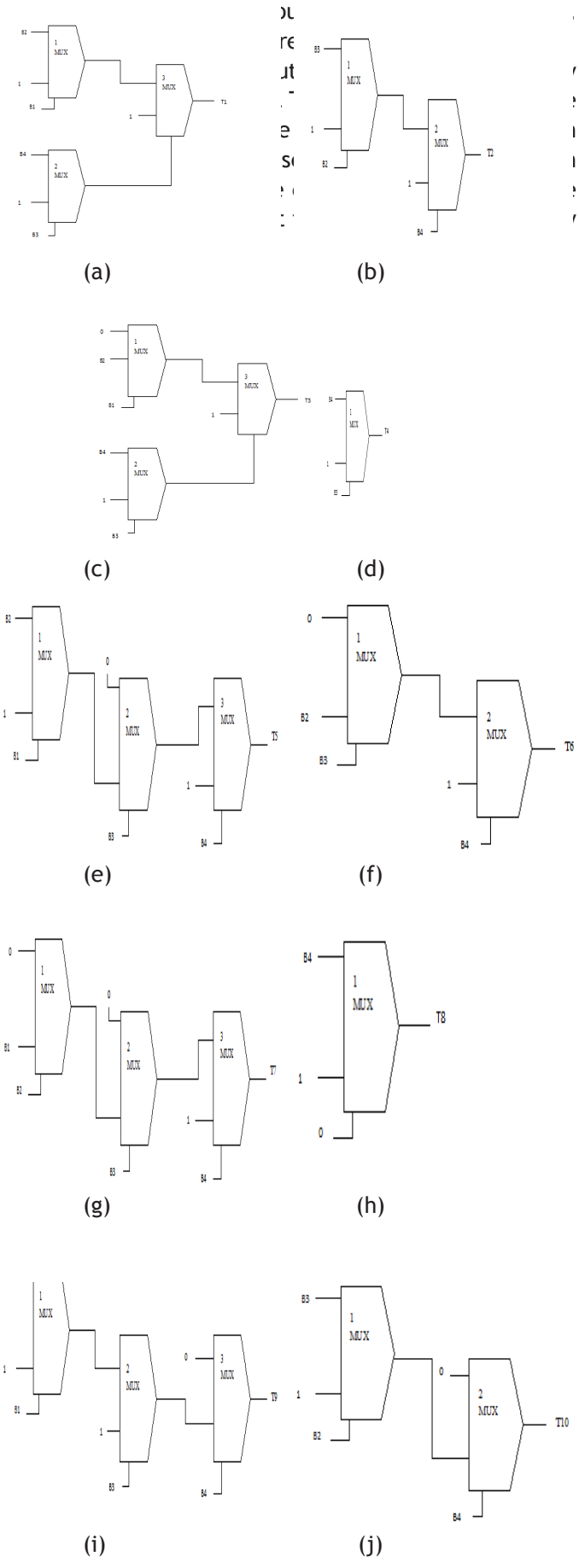
Fig. 6: Binary to Thermometer Decoder using IG-LP mode

design is based on the 2:1 multiplexer. All the 15 symbols are designed using 2:1 multiplexers. As this logic diagrams are developed using logic equations, 2:1 multiplexers are designed in such a way that they perform the logic OR and logic AND functions. These 2:1 multiplexers are used in circuit design of symbols. The circuit diagrams of all the 15 symbols are demonstrated in Fig. 7.

After the designing of these 15 symbols they are merged together to form the decoder design using multiplexer. The block diagram of decoder design is shown in Fig. 8..

In Fig. 8, all the 15 symbols are grouped into a single circuit, collectively forms the multiplexer-based binary to thermometer decoder. Each symbol consists of its own logic that and is implemented using the 2:1 multiplexers.

From truth table of Binary to Thermometer Decoder, using k-maps, the logics equations are simplified and these equations are turned into circuits using the FinFET IG-LP mode. The obtained logic equations after simplification are



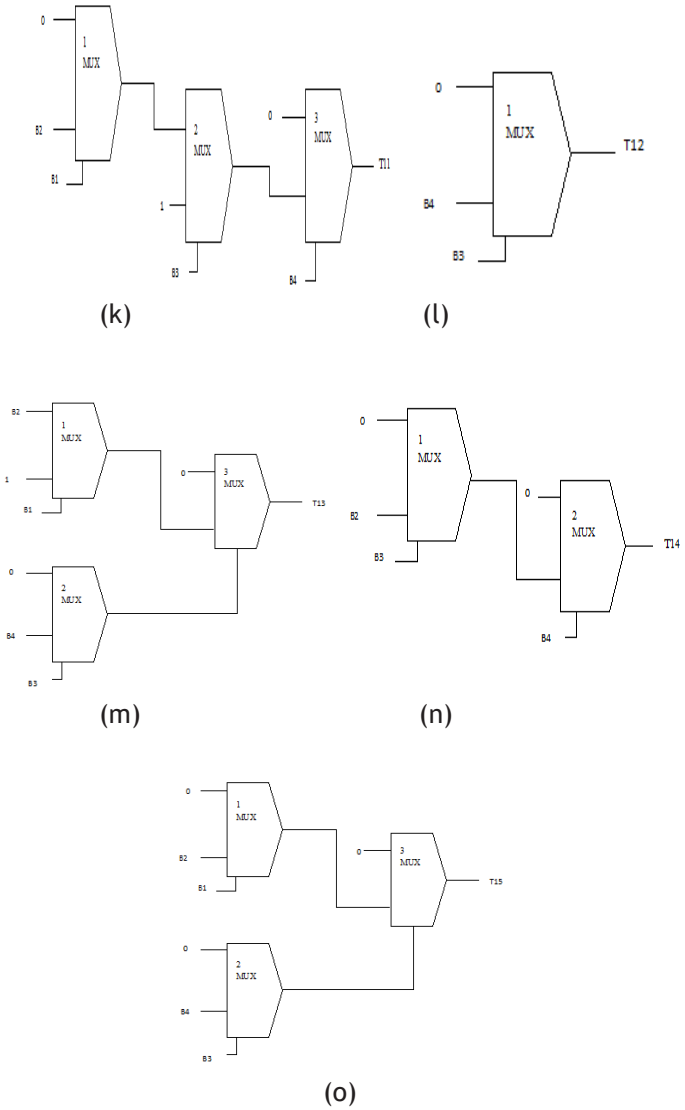


Fig. 7: Mux based Logic circuit symbols of T1 to T15

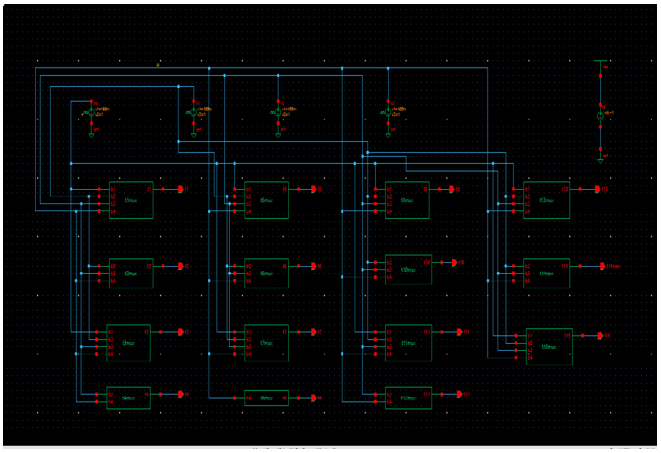


Fig. 8: Binary to Thermometer decoder design using 2:1 multiplexers

demonstrated below by considering binary input data as B4 to B1 and thermometer output data as from T_{15} to T_1.

$$T_1 = B_1 + B_2 + B_3 + B_4 \quad (1)$$
$$T_2 = B_2 + B_3 + B_4 \quad (2)$$
$$T_3 = B_1B_2 + B_3 + B_4 \quad (3)$$
$$T_4 = B_3 + B_4 \quad (4)$$
$$T_5 = B_3(B_1 + B_2) + B_4 \quad (5)$$
$$T_7 = B_1B_2B_3 + B_4 \quad (6)$$
$$T_8 = B_4(B_1 + B_2 + B_3) \quad (7)$$
$$T_9 = B_4(B_1 + B_2 + B_3) \quad (8)$$
$$T_{10} = B_4(B_2 + B_3) \quad (9)$$
$$T_{11} = B_4(B_1B_2 + B_3) \quad (10)$$
$$T_{12} = B_4(B_1B_2 + B_3) \quad (11)$$
$$T_{13} = B_4B_3(B_1 + B_2) \quad (12)$$
$$T_{14} = B_4B_3B_2 \quad (13)$$
$$T_{15} = B_4B_3B_2B_1 \quad (14)$$

Simulation Results and Experimental Findings of the Proposed Work

These circuits are designed using the Cadence Virtuoso tool. This tool is majorly used in the design of the circuits that are used in the modern processors. Before hardware implementation, the circuits are designed in this tool and are analyzed in various ways to understand the properties, advantages, and disadvantages.

Figure 9 displays the transient response obtained by IG-LP mode binary to thermometer decoder.

In the output waveform, it is observed that all the output remains low when the binary input is 0000. When the binary input is 0001, only t1 remains low and all other outputs are high. If the binary input is 0010, except T_1 and T_2 all other outputs remains high. Similarly, when the binary input is 1111, all the outputs are high. Thermometer decoder has some properties which need to be verified from the above output waveform. When a 0 occurs

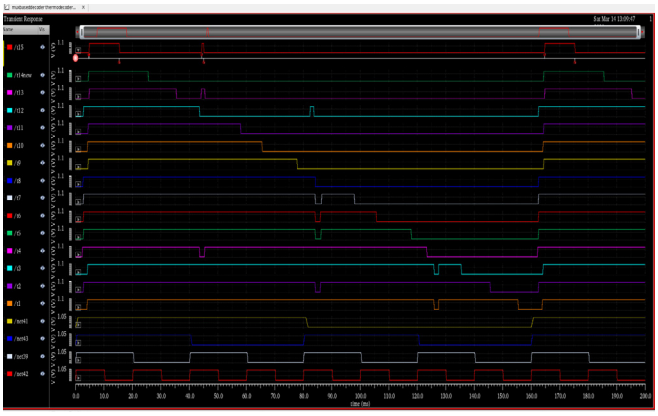


Fig. 9: Transient response of IG-LP mode Binary to Thermometer decoder

TABLE I. COMPARISON TABLE FOR POWER, DELAY, PDP, EDP FOR IG-LP MODE DECODER DESIGN

VDD	Power (μW)	Delay (μs)	PDP (x10-12J)	EDP (x10-12JS)
0.1	0.0183	278.7	5.10	0.0014
0.2	0.0193	332.4	6.41	0.0021
0.3	0.0854	377.8	32.2	0.012
0.4	0.482	533.8	257.2	0.137
0.5	1.653	576.4	952.7	0.549
0.6	3.322	624.9	2075.7	1.29
0.7	5.050	673.3	3400	2.28
0.8	6.799	719	4888.4	3.51
0.9	8.875	761.4	6757.4	5.14
1.0	11.36	6823.6	9356	7.7

values are 0.0183uW and 278.7us, respectively. Similarly, when V_{DD} is set to 0.2V the power and delay values are 0.0193uW and 332.4us, respectively. It is observed that, as the V_{DD} increases the power and delay of the circuit also increases.

Experimental Findings of the Proposed Work

Table 1 illustrates the comparison for delay, power delay product (PDP), energy delay product (EDP) for the IG-LP mode proposed design.

TABLE I.

From Table 1 it is observed that when V_{DD} is set to 0.1v, the power and delay are 1.83nw and 278.7μs. Here the PDP and EDP are also calculated. PDP is referred as the average energy consumed per switching event and EDP can deal with increased delay for lower energy. These two factors are very important in Nanoelectronics as the performance of any design can be calculated and later the drawbacks can be improved. When V_{DD} is set to 0.1V, EDP and PDP are 5.10pJ and 0.0014pJs. The power and delay at 0.5V is 1.653 micro watts and 576.4 micro seconds. In this condition, PDP and EDP are 952.7 Pico joules and 0.549pJs. There is a large variation in all the factors at V_{DD} at 0.5V. When V_{DD} is 0.6V and 0.7V, there is no large variation in EDP and PDP. But when the V_{DD} is set to 1V, there is a large variation in power and delay which gradually leads to higher values of EDP and PDP.

Conclusion

In this paper, the binary to thermometer decoder is designed in two methods. They are the logic-based decoder and multiplexer based decoder. In logic-based decoder, FinFET with 18nm technology in IG-LP mode is used. This IG-LP mode is particularly used to reduce the area and leakage power consumption of the circuit to make it more viable in application specific ICs. Nanoelectronics play a major role in the advanced technologies, where there is a requirement for low power consumption and high speed of operation. When the multiplexer-based decoder design is considered, only 2:1 multiplexers are used in this design process. This complexity to this design is less compared to the IG-LP mode. The entire operation of the decoder circuit is carried out using the functionality of 2:1 multiplexers. These two designs can be used in ADCs. In future, these designs can be modified in further development process in order to make use of these designs for various requirements. The IG-LP mode used in this design can be replaced with SG mode, if there is a need of enhancing the drive strength and a better control of the channel length. When there is a need of reducing the area of the circuit, IG mode is used. The speed of operation becomes slow when 2:1 multiplexers are used as the delay is added in switching the ports. If these 2:1 multiplexers are replaced with 4:1 multiplexers, there is a chance of enhancing the speed of operation and further reduces the cost and complexity of the circuit.

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