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ADC: Novel Methodology for Code Converter Application for Data Processing

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Abstract

An innovative "Multiplexer based Thermometer to Binary code encoder" is presented in this paper. This paper shows a relative decrease in the total count of multiplexers used which eventually reduces the no of transistors used when compared to traditional Architectures. The requirement for further more inverters is also eliminated in the proposed model. The input thermometer code is at first is converted to the respective gray code with the help of 2:1 multiplexer. Thereafter, using two-input XOR gates the conversion process of gray code to respective binary codes takes place. Outcomes of simulation reveal that there is an approximately 80% decrease in the power consumption which is a great reduction actually when differentiated with previously known and current encoder architectures with the delay being reduced from 0.472ps to 0.366 ps. This throws a light on modern power-saving encoder architectures and has a greater significance in the future. The proposed encoder gives a better application for future generation advanced ADC & related circuits.

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Introduction

One of the key operating unit in digital signal processing and system on chip applications is 'Analog to digital convertors' (ADC). For immense rapidity & applications on low resolution, the flash Analog to digital convertor is relatively used amidst various ADC design models.[1-4] Figure 1 displays the design model of flash ADC.[5-7]

Using thermometer to binary encoder, the outputs of comparator are converted to binary code. The ADC displayed in the image below has '2N -1' comparators for the 'N-bit resolution', in which reference voltage (V-ref) is being compared with the given input (analog signal) to provide the output as 'one' or 'zero'.[8-21]

There is necessity to construct ADC with greater rapidity, there by consuming fewer power, considering the fact that delay and power are the most significant elements in Integrated Circuit design. The traditional encoder designs present in "flash ADC" consumes more power and has a large delay.[22-31]

Therefore, an advanced model encoder is being proposed in the paper that actually uses/absorbs less amount of power and has very less delay when differentiated with existing and traditional and current encoder designs.[8-9]

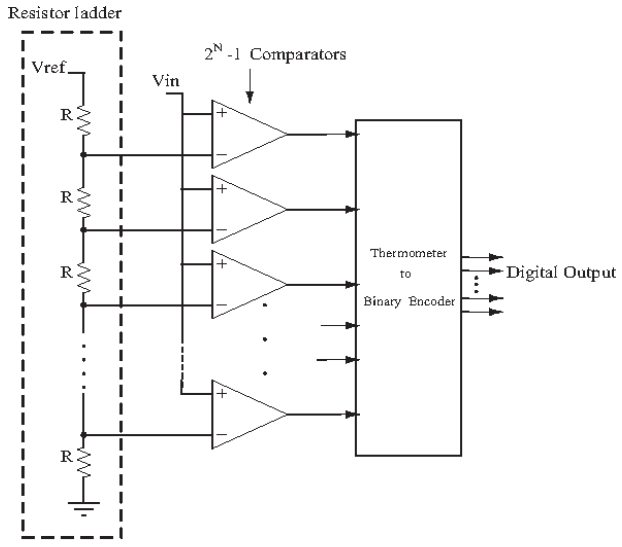


Fig. 1: N bit Flash ADC

Significant Drawbacks in the Existed Methods

In the existed methods the power consumption is more. This makes the circuit to draw or consume a lot of power. The existed model does not permit high integration levels. Due to their higher threshold voltage, previously known methods cannot be operated at low voltages.[32-39]

This tells us that the previously known and current known methodologies had a significant drawback which creates the need to invent new methodologies to make the circuit more efficient. It is also known that the static leakage current is also more in existing and previously known methodologies. There is high off-state current in MOSFET which is a major disadvantage. Existing models does not allow MOS technology to stay on track with Moore's law.

Proposed Design

The architecture or design model for the proposed design 4-bit encoder is displayed in the Figure 10 which is constructed based on 3-bit encoder design as shown in the fig 9. The basic blocks of the proposed model are "2:1 multiplexer" and "2-input XOR gate". After conversion process of thermometer code using "2:1 MUX" we get gray code as output as shown in Table 2 & the resultant binary code is acquired with the help of gray code from "2-input XOR gates" as displayed in the Figure 4.3. Here the input data one ('1') of a few of the multiplexers are linked or joined to ground node, to lessen the no of multiplexers & eliminate the requirement of extra inverters which when contrasted to the previously known models.

To achieve less power consumption, the "2:1 multiplexer" and "2-input XOR gates" are exercised using reliable methods of realizing through transmission logic gate [14]. Then the resulting binary code is acquired from gray code after successfully converting it with the help of XOR gates which is purposely done to increase the security and encrypting the information.

The implementation and methodologies used has a greater impact in the present generation advanced processors and enhanced security features when contrasted and differentiated with the existing or previously known models. The previously known models had a lot of drawbacks and disadvantages and hence we came up with a modern approach to implement new generation encoder designs which is actually more powerful and efficient than previously known models.

Paper Organization

Therefore, the main operation of 'Analog to digital convertors' is change or convert the given input (analog signal) to digital data. If suppose an input (analog) which is to be converted is sent to a machine (let it be a personal computer) then to process the analog information to the machine there must be an ADC which can carry out the task of converting. This task of converting or processing analog information and changing into Distortion-Less digital data is carried out by 'Analog to digital convertor'. So, from the above stated information we came to know that there is need for ADC.

FinFET Characteristics and Modeling

FinFET description and Operation

FinFET is called as "Fin Field Effect Transistor", a kind of "3D" transistor extensively used in modeling the advanced future generation processors. Generally, FinFET models make use of a sort of conducting channel which will rise more than the level/limit of the insulator, making a very skinny layer of 'Si' construct which resembles the shape of a fin, called as gate electrode. Multiple gates can be allowed to operate on a single transistor using fin shaped electrode. This process is actually an extension of Moore's law, there by letting semiconductor manufacturers to design memory blocks and CPUs that are smaller in size, enabling faster performance, and also consume less power.

The main structure/element of the device which is actually formed by encasing conducting channel by a very light layer of Si "fin", which actually forms, is one of the key characteristics of FinFET. The basic layout of a FinFET and operation modes of a FinFET will not vary from traditional FET. The FinFET device Schematic is shown in the figure 2.

To manage the current flow, one source, one drain and also a gate is present. When compared with "planar MOSFET", the channel present between drain & source is designed as "3D" bar on upper part of the "Si" substrate which is known as fin. The gate electrode is encased all over the channel.

So, many gate electrodes on each side is formed leading to decrease in the discharge of charge and an intensified drift charge/current which helps overcoming some other short-channel effects. When the device is in the 'off' state

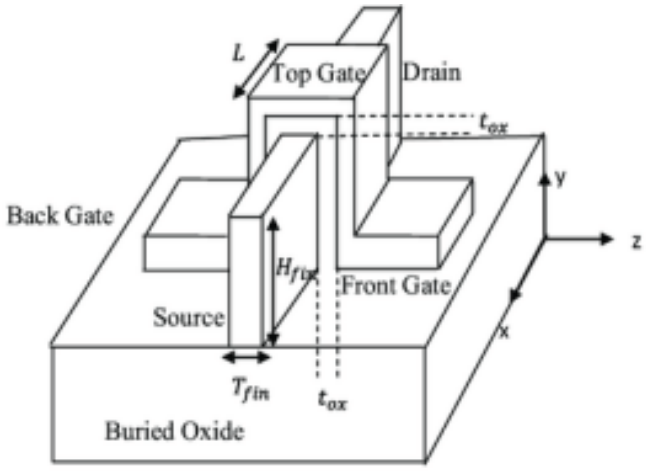


Fig. 2: FinFET Device Schematic

and when the channel is extended, there will be very small discharge of charge through the body. This will bring down threshold voltages and gives good performance and lower power consumption.

The figure 3 shows the comparison of construction between Planar MOSFET and FinFET

The figure 4 shows the comparison of construction between bulk and SOI FinFETs

Advantages of FinFET

In FinFET technology, the utilization of power is less. This makes the circuit to draw or consume less power. The FinFET technology permit high integration levels. Due to their lower threshold voltage, it can be operated at low voltages.

This tells us that the FinFET technology has a great advantage than previously known and current known methodologies which make the circuit more efficient. It is also known that the static current leakage is less when differentiated to existing and previously known methodologies. There is low off-state current in FinFET which is a major advantage. FinFET technology allows MOS technology to stay on track with Moore's law.

Applications of FinFET

As both gates can be conveniently controlled separately, it results in less power consumption. Threshold voltage of the device can be controlled by 2nd gate, which permits faster switching capabilities on one side and decreased current leakages when the circuit is unused. Finally, individual access to both gates can be used to develop a better simple logic gate. This would result in less power consumption, and also save area of the chip, leading to efficient & enhanced designs. In conclusion, we can understand that FinFET technology has more advantages than the previously known & currently used technology. This throws a light on designing future encoders using this technology which shows better performance.

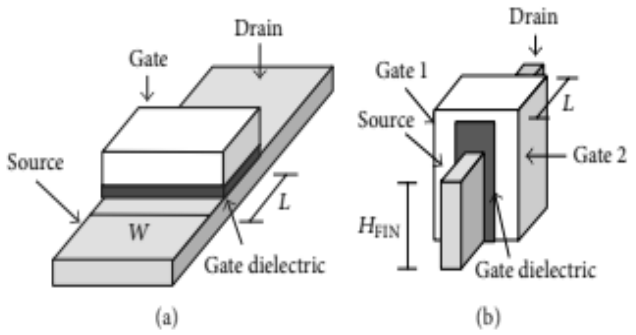


Fig. 3: Comparison of construction between (a) planar MOSFET & (b) FinFET

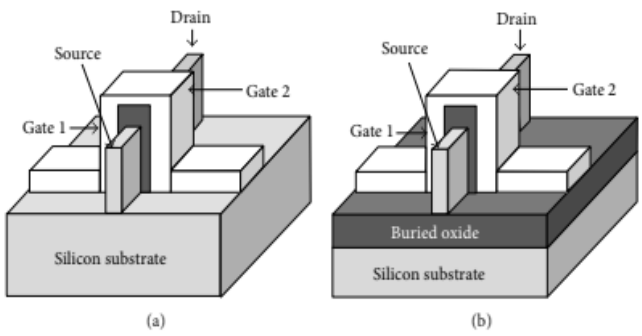


Fig. 4: Comparison of construction between (a) bulk and (b) SOI FinFETs

Proposed 4-Bit Encoder Block Using FinFET Models

Wallace Tree Encoder

It generally checks and calculates the number of ones in the thermometer code (input) at the first level & provides the output as 2-bit binary code. After this initial stage, in an effort to get a required regular structure, two-bit data of the adjacent cells 2 by 2 are added. The same process of structuring follows up on for 3rd level resulting 4-bit gray code outputs as shown in Figure 5 and Table 1. Hence, it is also called as "Ones counter" [10]. The counter mechanism can be chosen on the basis of the speed of ADC. As the framework is designed using full adder, which has many transistors, which results in increased power consumption. So, the structure consumes large power and the delay also increases which is a major drawback.

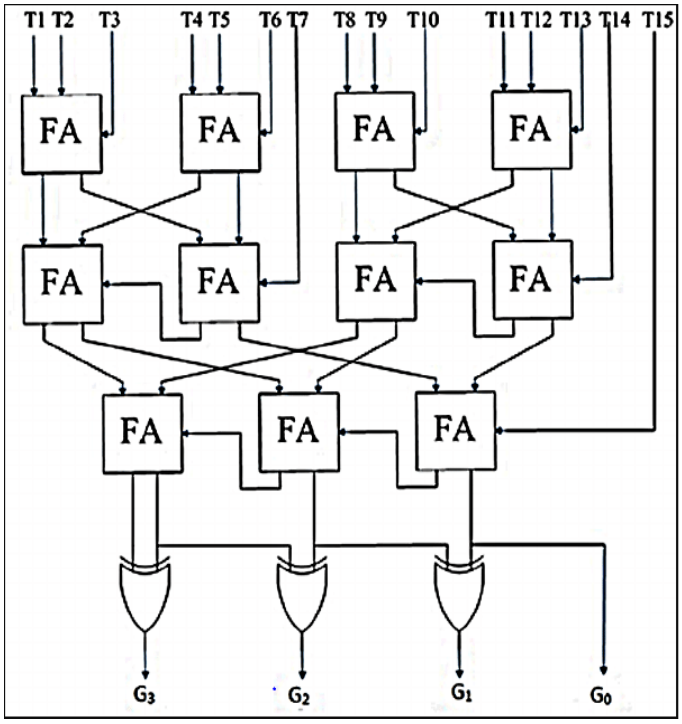


Fig. 5: Wallace Tree Encoder

Realization of XOR gate with the help of Transmission gate

The Figure 6 shows is multiplexer implemented using transmission gate.

Conventional Mux based Encoder description and operation

In this model 2:1 Multiplexer is used to attain less power consumption and less delay when differentiated with Wallace tree encoder. As it operates at greater speed and occupies small area of chip in comparison to above discussed architecture, this design model is generally used for designing flash ADCs. Figure 7 puts on view of the design of existing MUX based encoder.[11-12] The Self Re-configurable property[13] is a plus point for MUX based encoder in which

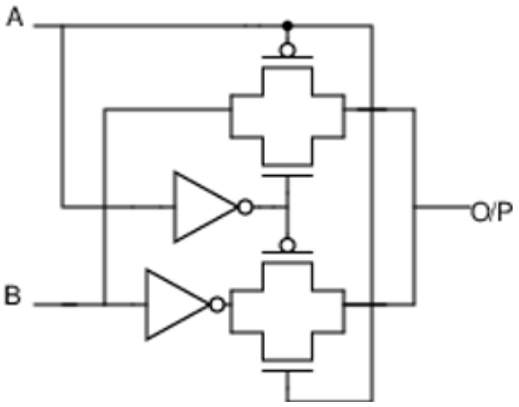


Fig. 6: Realization of XOR gate with the help of Transmission gate

similar encoder is used for several applications. This design has a drawback of large fan-out which has an increased view on the overall power consumption. The circuit shown below is existing MUX based encoder.

Realization of Multiplexer with the help of Transmission gate

The Figure 8 shown below is multiplexer implemented using transmission gate logic.

Mux Encoder using Thermometer code description and operation

The architecture or design model for the proposed design 4-bit encoder is displayed in the Figure 10 which is constructed based on 3-bit encoder design as shown in the Figure 9. and the truth table for 3-bit encoder is displayed in the table 1.2. The basic blocks of the proposed model are "2:1 multiplexer" and "2-input XOR gate". After conversion process of thermometer code using "2:1 MUX" we get gray code as output as shown in Table 1.1& the resultant binary code is acquired with the help of gray code from "2-input XOR gates".

3-bit Encoder

3-bit encoder taken as reference for constructing 4-bit encoder

$$G_3 = T_4$$
$$G_2 = T_2\overline{T_6}$$
$$G_1 = T_1\overline{T_3} + T_3\left(\overline{T_7}T_5\right)$$

Table 1: Truth table of 4: Bit Encoder (Thermometer to Gray) code conversion

Thermometer Code															*Gray Output*		
T15	*T14*	*T13*	*T12*	*T11*	*T10*	*T9*	*T8*	*T7*	*T6*	*T5*	*T4*	*T3*	*T2*	*T1*	*G4*	*G3*	*G2*	*G1*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

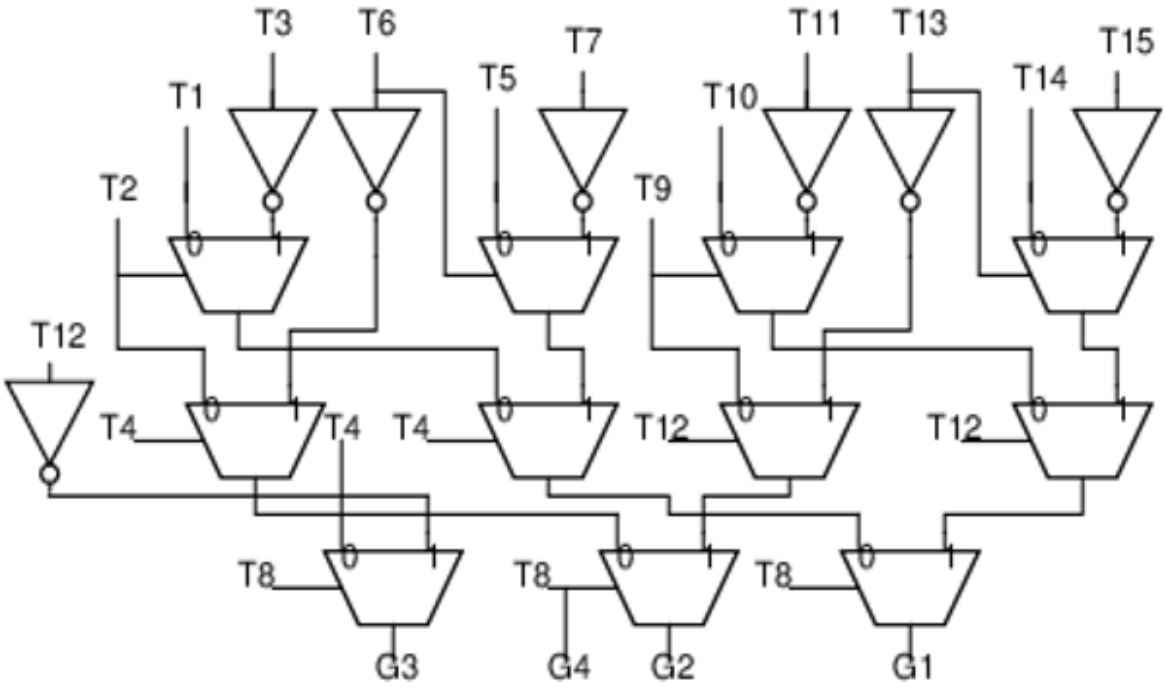


Fig. 7: Existing MUX Based Encoder

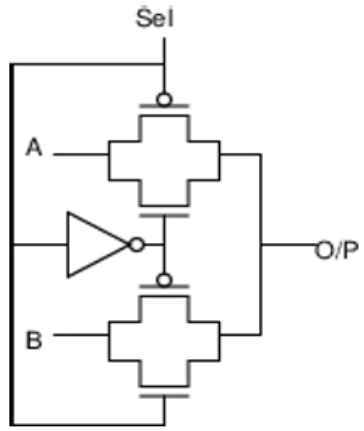


Fig. 8: Realization of Multiplexer with the help of Transmission gate

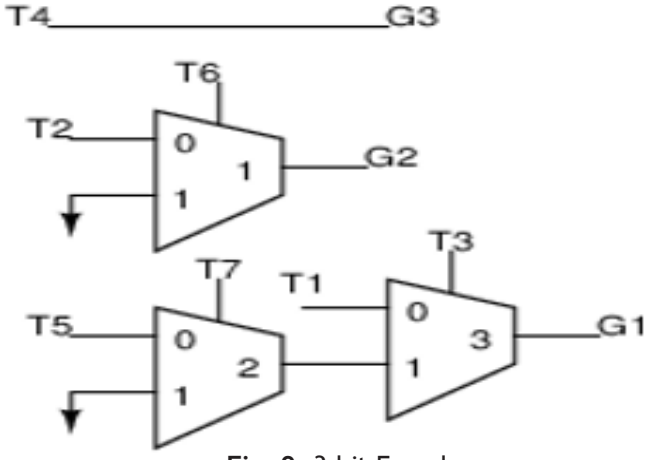


Fig. 9: 3-bit Encoder

Table 2: Truth Table For 3- Bit Encoder

Thermometer Code							*Gray Output*		
T7	*T6*	*T5*	*T4*	*T3*	*T2*	*T1*	*G3*	*G2*	*G1*
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	1
0	0	0	0	1	1	1	0	1	0
0	0	0	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	0	0

4-Bit Encoder

Expressions of conversion is written using Figure 10 Circuit Diagram of 4-bit Encoder

Gray to binary Conversion

Generally Gray to binary conversion as displayed in table 3 is done just to increase the security and encryption mechanism. The conversion is shown in the below Figure 11.

Here the input data one ('1') of a few of the multiplexers are linked or joined to ground node, to lessen the no of multiplexers & eliminate the requirement of extra inverters which when contrasted to the previously known models. To achieve less power consumption, the "2:1 multiplexer" and "2-input XOR gates" are exercised using reliable methods of realizing through transmission logic gate.[14]

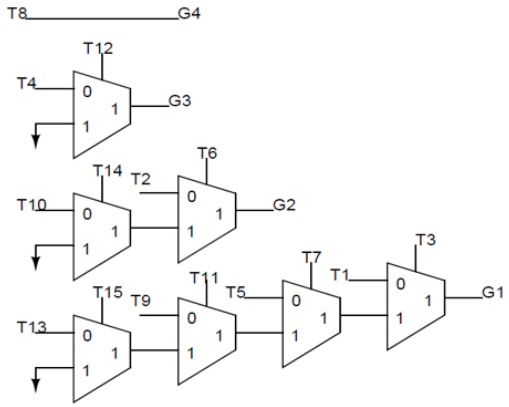


Fig. 10: 4-bit Encoder

Then the resulting binary code is acquired from gray code after successfully converting it with the help of XOR gates which is purposely done to increase the security and encrypting the information.

Simulation Results and Experimental Findings of the Proposed Work

Simulation Results of Wallace Tree Encoder

It generally checks and calculates the number of ones at the input at the first level and provides required output after processed through multiple levels. The below Figure 12 shown is Wallace tree encoder circuit. The waveform is displayed in figure 13.

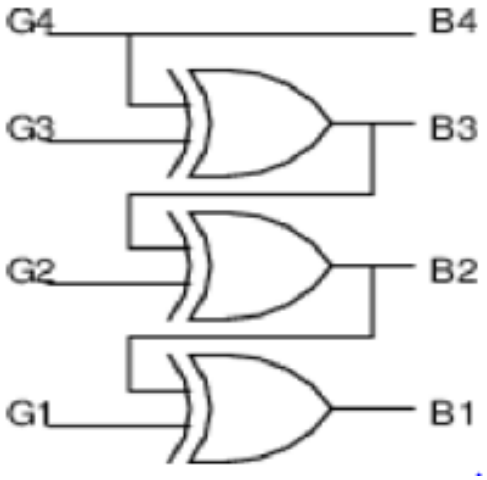


Fig. 11: Gray to binary conversion

Table 3: Truth Table for conversion (input gray code to output binary code)

Gray Code Input				*Binary Output*			
G3	*G2*	*G1*	*G0*	*B3*	*B2*	*B1*	*B0*
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

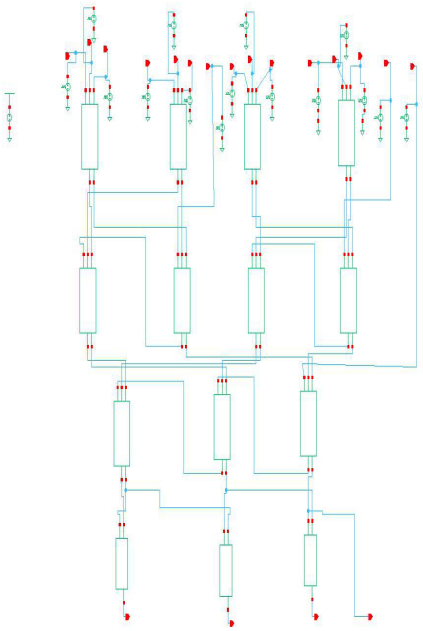
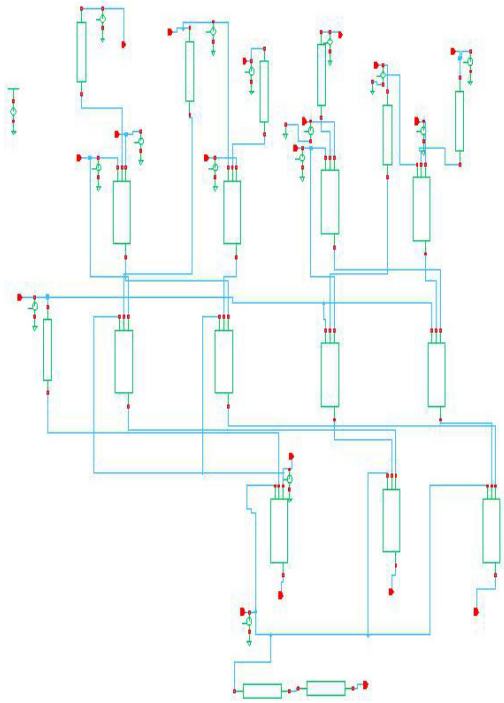


Fig. 12: Wallace Tree Encoder Circuit



ig. 14: Existing Mux Based Encoder Circuit

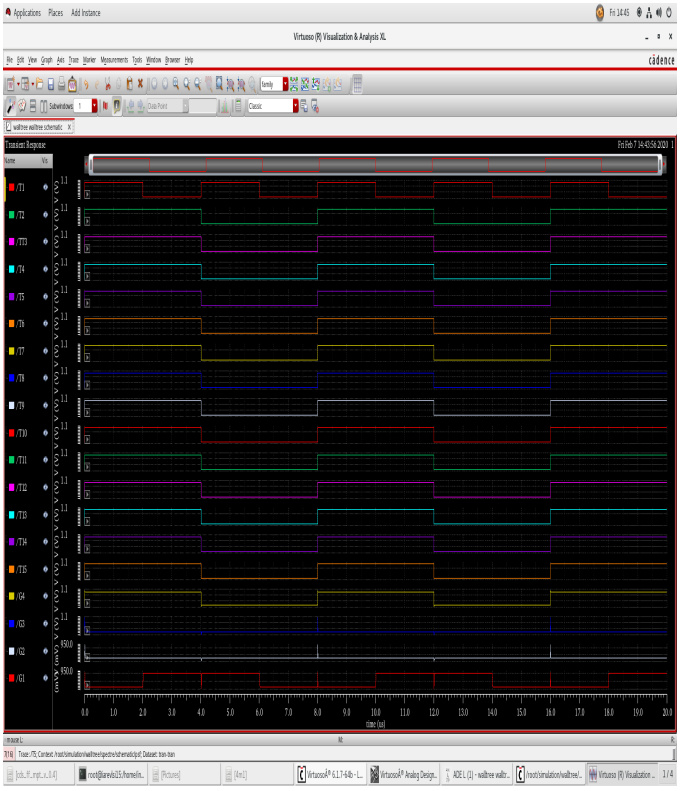


Fig. 15: Existing Mux Based Encoder Waveform

Simulation Results of Conventional Mux based Encoder

In this model as shown in Figure 14 “2:1 Multiplexer” is used to attain less power consumption and less delay when differentiated with “Wallace tree encoder”. The

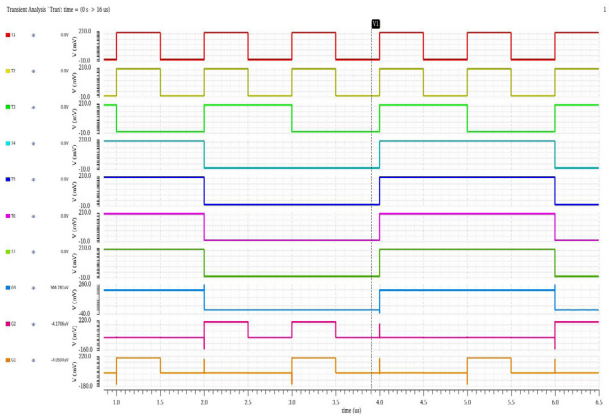


Fig. 16: 3-Bit Encoder Waveform

waveform of the circuit is shown in Figure 15. This design has a drawback of large fan-out which has an increased view on the overall power consumption.

Simulation Results of Mux Encoder using Thermometer code

4.3.1 3-Bit Encoder

The Figure 16 represents 3-bit encoder waveform

4-Bit Encoder (Thermometer coder)

The Figure 17 represents 4-bit encoder waveform

Gray to binary Conversion

The Figure 18 represents Gray to binary code conversion waveform

Table 4 shows us the comparison for delay, PDP, EDP for all three encoder circuits.

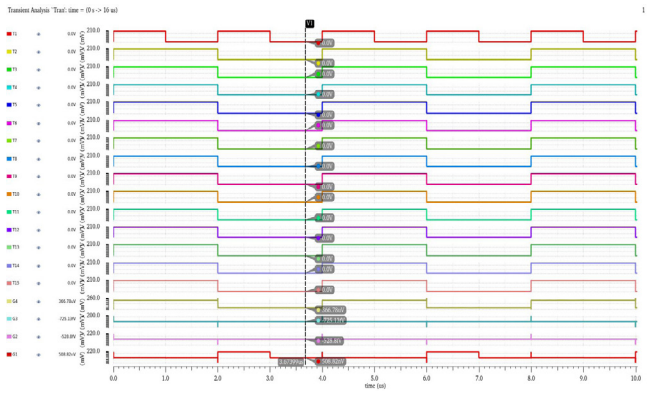


Fig. 17: 4-Bit Encoder Waveform

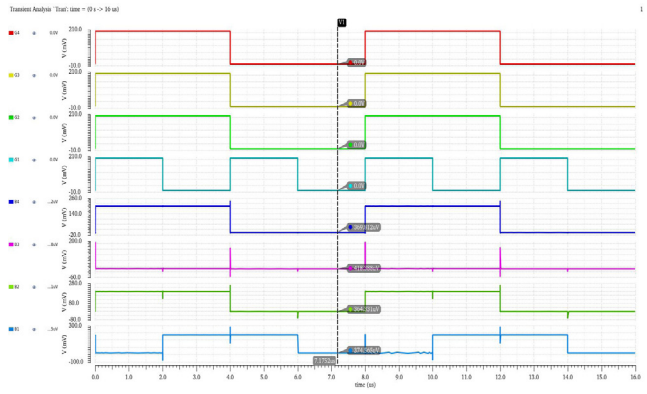


Fig. 18: Gray to binary conversion verification Waveform

Table 4: Comparison for delay, PDP, EDP for all three encoder circuits

Structure	*Power Consumption (mW)*	*Delay (ns)*	*Power Delay Product (PDP) (x10-24)J*	*Energy Delay Product (EDP) (x10-24)Js*
Wallace Tree Encoder	51.07	124	6.332	785.168
Existing MUX Encoder	2.45	0.472	0.0015	0.000708
Proposed MUX Encoder	0.698	0.366	0.00025	0.000091

Simulation results Analysis

All the three encoder architectures discussed in the above chapters and design models are simulated using "Cadence software Simulator" at 18nm advanced technology. The Table 4 brings us a comparison between different encoder designs and performance analysis. Outcomes of simulation reveal that there is approximately 80% decrease in the power consumption which is a great reduction actually when differentiated with previously known and current encoder architectures with delay being reduced from 0.472ps to 0.366ps which tells us that the circuit performs faster than ever before. This throws a light on modern power saving encoder architectures and has a greater significance in future.

Conclusion

In Conclusion, an innovative "Multiplexer based Thermometer to Binary code encoder" is presented in this paper. This paper shows a relative decrease in the total count of multiplexers used which eventually reduce the no of transistors used when compared to traditional Architectures. The requirement for further more inverters is also eliminated in the proposed model. The input thermometer code is at first is converted to the respective gray code with the help of 2:1 multiplexer. Thereafter, using two input XOR gates the conversion process of gray code to respective binary codes takes place. Outcomes of simulation reveal that there is approximately 80% decrease in the power consumption which is a great reduction actually when differentiated with previously known and current encoder architectures with delay being reduced from 0.472ps to 0.366 ps. This throws a light on modern power saving encoder architectures and has a greater significance in future. The proposed encoder gives a better application for future generation advanced ADC & related circuits.

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