Journal of VLSI circuits and systems

Journal of VLSI Circuits and Systems, ISSN: 2582-1458 Vol. 5, No. 1, 2023 (pp. 1-7)

RESEARCH ARTICLE

WWW.VLSIJOURNAL.COM

Fundamental Flip-Flop Design: Comparative Analysis

Kagaba J. Bosco[1], S. M Pavalam[2], L.J. Mpamije[3]

Information and Communications Technology, National Institute of Statistics of Rwanda, Kigali, Rwanda

KEYWORDS:
Clock;
D-Latch,
Delay,
FinFET,
Leakage current,
Power consumption.

ARTICLE HISTORY:
Received 14.07.2022
Accepted 10.08.2022
Published 23.09.2022

DOI:
https://doi.org/10.31838/jvcs/05.01.01

Abstract

A latch is used to store single bit information. It is a level triggered device. These are the building blocks for sequential circuits. The basic working of D-Latch is that input data will be transferred to the output node whenever the clock or enable signal is high. In this paper, various efficient designs of d-latch using 18nm FinFET technology are proposed. The designing of latches are very flexible when compared with flip flops. FinFET technology has many advantages over planar CMOS, such as lower leakage current and lower power consumption. The circuits are designed and simulated using FinFET spectre models in cadence virtuoso tool. The proposed latches using FinFET consumes less power and has low power delay product when compared to traditional D-Latch designs.

Author's e-mail: Bosco.je.kag@nur.ac.rw, pav.sm@nur.ac.rw, lj.mpam@nur.ac.rw

How to cite this article: Bosco KJ, Pavalam SM, Mpamije LJ. Fundamental Flip-Flop Design: Comparative Analysis. Journal of Complementary Research, Vol. 5, No. 1, 2023 (pp. 1-7).

Introduction

Nowadays, all the electronic circuits require low power consumption and an increase in the speed of operation. Many technologies have been used by the researchers to design circuits with less power consumption. A Low-Voltage CML (current mode logic) D-latch and CML based logic gates and Latches are designed in.[1,2] Process variations have been increasing with technology scaling. These process variations effect the temperature of the device. These effects are studied and discussed in.[3] The optimizations in the FinFET devices are discussed in[4] for low power and delay. FinFET circuits are designed at low power, and they are analyzed at multiple threshold voltages and supply voltages in.[5] The soft error masking latches have been designed to reduce the errors and obtain the efficient outputs in.[6] MCML D-Latch has been designed in.[7] A low-cost CMOS latch has been designed in.[8] A time redundant hardened latch has been designed for efficient outputs.[9] Transistor stacking technique has been implemented in many combinational circuits to reduce the leakage current.[10] A fault resistant D-Latch has been designed to reduce the transient faults that occurred from the previous circuits .[11] Different D-Latch topologies have been designed in 32nm CMOS technology based on transistor stacking effect in.[12] A ternary D-Latch has been designed using GNRFET's (Graphene Nano-ribbon Field Effect Transistor) as it gives reduced power consumption and a small area.[13] The brief explanation about the characteristics, working and types of FinFET are studied and discussed in.[14]

Commonly used methodologies are CMOS, FinFET, GNRFET, etc. FinFET is used in many electronic devices, and it serves as the basis for fabrication of nano semiconductor devices.[15, 16] So far, many researchers have preferred planar MOSFET's that are built on bulk silicon wafers. CMOS (Complementary MOSFET's) are mostly preferred to design various VLSI circuits and its applications.[17, 18]

MOSFET is widely used for amplifying the electronic signals and switching in electronic devices. However, the main drawback in MOSFET is the increase in short channel effects.[19] The short channel effects mainly arose due to electron shifts and the change in threshold voltage.[20] The main motive of most of the researchers is to reduce power consumption and enhance the speed of operation. To achieve these improvements we have to decrease the

channel length. Due to this decrease in channel length, drain potential will influence the electrons in the channel. Due to this, the gate loses its control over the channel. This problem leads to an increase in leakage current and short channel effects.[21] The Multiple-gate Field Effect Transistors (MGFET's) are the best alternative for MOSFET's to reduce the leakage currents and short channel effects.[22] Because if one gate loses control over the channel, the other gate takes control and reduces the leakage current, thereby reducing the short channel effects. This is the main advantage of MGFET's.[23] The most commonly used MGFET's are FinFETs and Tri-gate FET's. The fully depleted SOI (silicon-on-insulator) MOSFET's reduces the leakage current to some extent. The MGFET's reduces the leakage current and offer better performance when compared with planar MOSFET's.[24, 25].

The existing circuits are designed using CMOS technology. To obtain better results of power and delay FinFET technology has been evolved. As FinFET has many advantages than CMOS technology, the proposed circuits are designed using FinFET technology. The proposed D-Latches are designed in 18nm FinFET technology for low power memory applications. Different D-Latches have been designed and simulated using cadence virtuoso tool.[26]-[31]

The characteristics and working of FinFET are discussed in the second section. There are two types of FinFET. Shorted-gate FinFET and Independent-gate FinFET. The brief description of the types of FinFET and its advantages and applications are discussed in the next section. The proposed design and its circuit diagrams, along with its truth tables are discussed in the third section. The simulations are performed using cadence virtuoso tool. These results are shown in the fourth section. The experimental results are also performed. The power delay calculations and comparisons are tabulated in the fifth section. The final results obtained and conclusions are discussed in the last section. Advantages of the designed circuits and their applications are also discussed.

FinFET Characteristics and Modeling

The MGFET's can reduce the leakage current and offer better performance when compared with planar MOSFET's. Among all the MGFET's, FinFETs and Tri-gate FET's are mostly preferred because they are simple to fabricate. FinFET having thick oxide on the top of the fin is called as Double gate FinFET. FinFET having thin oxide on the top of the fin and the sides is called as Tri-gate FinFET.[26] The structures for FinFET and Tri-gate FET's are shown in Figure 2. Tri-gate FET's have an additional gate on top of the fin so that its process becomes complex. However, the fringe capacitances will be reduced by using the Tri-gate FET's. But FinFET is mostly preferred by most of the researchers. The working principle of FinFET is similar to MOSFET. But the main difference is CMOS is a planar transistor and FinFET is a non-planar transistor with two gates.[27-35]

FinFET was developed by Chenming Hu and by his colleagues at the University of California, Berkeley. FinFET is a non-planar transistor. It is a multi-gate device. It is a MOSFET with channel elevated so that the gate surrounds the channel on three sides. Due to this gate that surrounds the channel, leakage current decreases, and the obtained results will be useful. The technology has been named as FinFET because the structure looks like a set of fins. The basic working of FinFET is same as standard CMOS. FinFET also has source, drain and a gate to control the flow of current. But the only difference is that the channel is built in three dimensional between the source and drain. The gate surrounds the channel so that leakage current reduces. The width of the FinFET is nothing but the height of the channel. FinFETs are built on both bulk and silicon-on-insulator wafers. Most of the researchers prefer FinFET built on SOI wafers. Bulk FinFETs are also used by some of the companies.[32-39]

Proposed D-Latch Module Using FinFET Models

In this paper, the proposed circuits are designed using FinFET technology. Latches can be easily designed when compared to flip-flops. These are used in sequential circuits like shift registers, adders, etc. The proposed circuits show better performance by reducing power consumption and power delay product when compared to existing D-Latch.

A latch is used for storing single bit information. Every sequential circuit is built with latches. So these are the

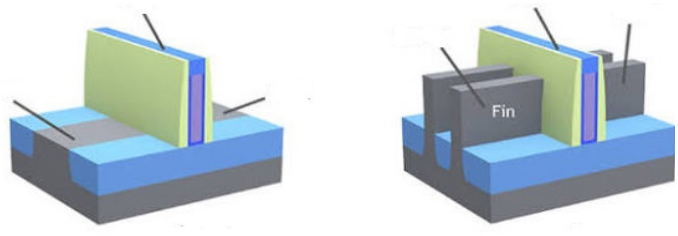


Fig. 1: Structure of (a) planar MOSFET (b) FinFET

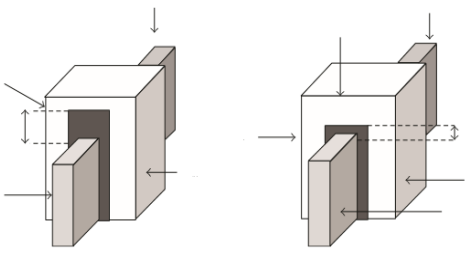


Fig. 2: Structures for (a) FinFET (b) Tri-gate FET

building blocks for sequential circuits. When CLK is high, the output will be the same as D. When CLK is low output will remain in its previous state. The working of D-Latch has validated from the circuit of basic D-Latch shown in Figure 3.

Design 1

From Figure 3, when clk is high the transistors T1 and T2 becomes on and passes the data D. This data gets inverted by transistors T3 and T4 and again inverted by T9 and T10. At this instant, the data inverted by T3 and T4 gets stored and latched by transistors T5, T6, T7 and T8. When CLK becomes low T1 and T2 becomes off and T5, T6 becomes on. So the data D will not be passed through transistors T1 and T2. Therefore, the previous data which was stored by T7 and T8 will be passed through T5 and T6. This data gets inverted two times by the transistors T3, T4, T9 and T10. Finally, the output will remain in the previous state. Assuming that the previous state is logic '1' the truth table for deisgn1 is shown in table 2.

Design 2

From Fig. 4, when CLK is high, the transistors T1 and T2 become on. So the data D passes through T1 and T2. The data D will be directly sent to the output node. At this instant, the output will be stored by the transistors T9, T10, T11 and T12. Now if the CLK is off the transistors, T1 and T2 become off. So the data D will not be sent to the output node. The previous data which was stored by the transistors T9, T10, T11 and T12 will be sent to remaining transistors. So the output will remain in the previous state. The table 3 shows the truth table for Design2 assuming the previous state as logic '1'.

Design 3

From Fig. 5, when CLK is high, the transistors T2 and T3 become on. If D=1, then transistor T4 becomes on and T1 becomes off. So logic '0' will be sent to the next node. This gets inverted by the inverter, and then logic '1' will be sent to the output. At this instant, this output data will be stored by the transistors T7 and T8. The same process goes on for D=0. Now if CLK becomes low, transistors T2 and T3 become off. So no data will be sent to the next node. Transistors T8 and T9 become on. As the previous output is '1' transistor, T7 becomes off, and T10 becomes on. So logic '0' will be sent to the next node. This gets inverted, and logic '1' will be sent to the output. From this, it is evident that whenever CLK is low output remains in the previous state. The truth table for this design is shown in table 4, assuming the previous state as logic '1'.

Design 4

Figure 6 shows ternary D-Latch design. The existing circuit is designed using GNRFET. The proposed circuit is designed using FinFET. The circuit diagrams for NTI (Negative ternary inverter), STI (Standard Ternary Inverter) and NAND gates are shown in figure 7. NTI and STI work similarly to the basic inverter. These are designed to generate three levels in the output. But the designed circuit is simulated using cadence virtuoso tool. So the output consists of

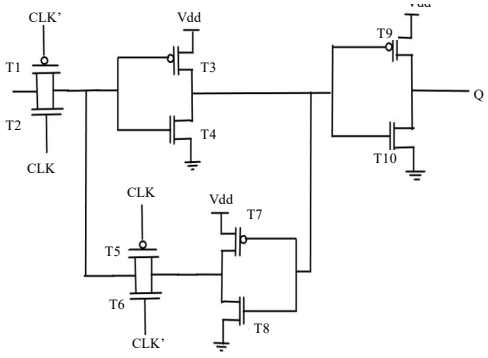


Fig. 3: D-Latch design1

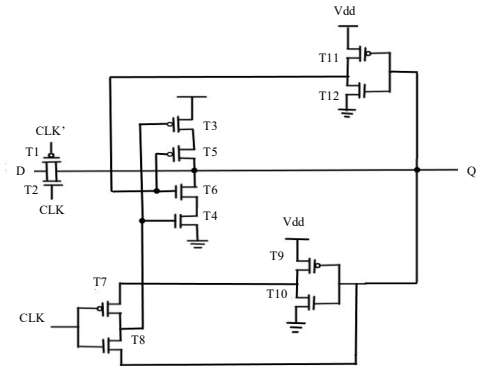


Fig. 4: D-Latch design 2

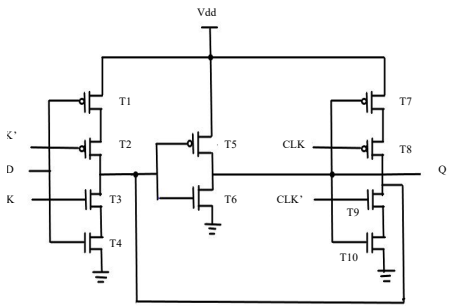


Fig. 5: D-Latch design 3

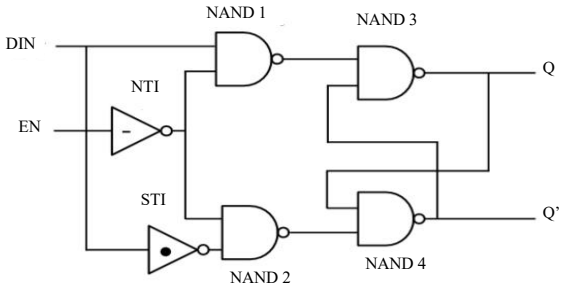


Fig. 6: D-Latch design 4

only two levels. Ternary NAND gate also works similar to a binary NAND gate.

From figure 6, whenever the EN is low, the output Q will be the same as the data D. when the EN is high output will remain in the previous state. This is the operation of the above D-Latch. The truth tables for the inverters, NAND gate and the designed circuits are shown in the following tables.

Figure 9 shows the circuits for STI and NTI. The above circuits are designed using ternary logic. The working of these circuits is similar to that of CMOS inverter and NAND gates. The truth table for these circuits is shown in Table I and Table II.

Experimental Findings of the Proposed Work

The schematics are designed and simulated using 18nm FinFET library in cadence virtuoso tool. The circuits are simulated with a power supply of 1V at a frequency of 1GHz. Power and Delay values are also obtained from the resultant waveforms. The power and delay calculations are performed for both LVT and HVT FinFETs. The outputs for all the designed circuits are shown in figure 8, 9, 10 and 11.

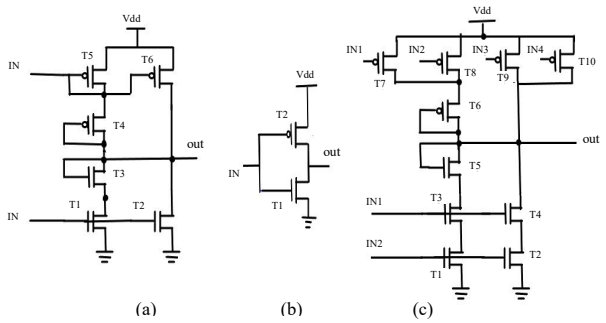


Fig. 7: Schematics for (a) STI (b) NTI (c) NAND

Table 1: Truth table for STI and NTI

Input	STI o/p	*NTI o/p*
0	2	2
1	1	0
2	0	0

Table 2: Truth table for STI and NTI

Input IN1	Input IN2	NAND output
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

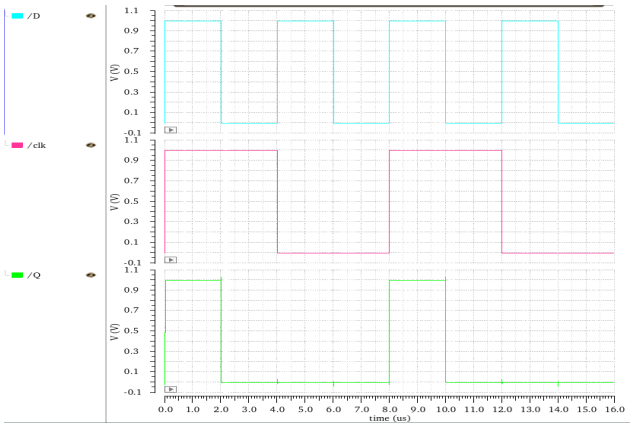


Fig. 8: Output for Design1

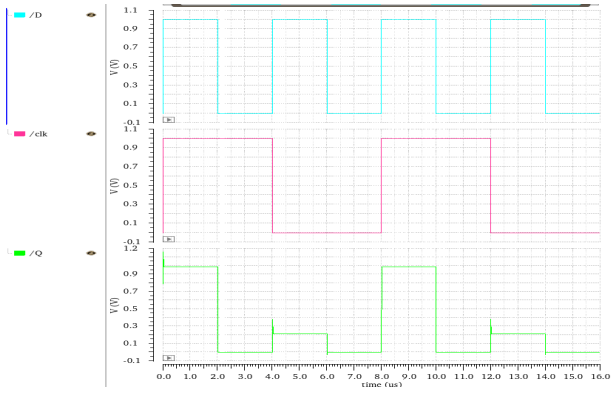


Fig. 9: Output for Design2

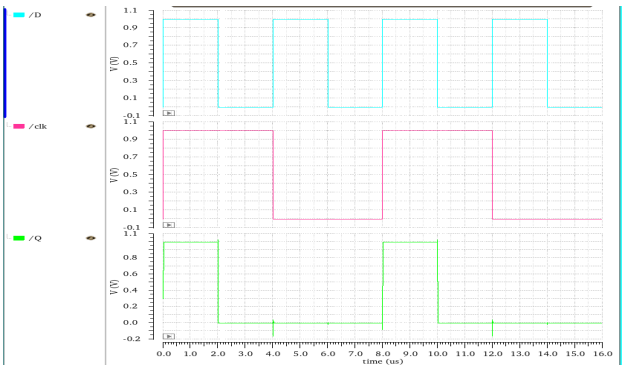


Fig. 10: Output for Design3

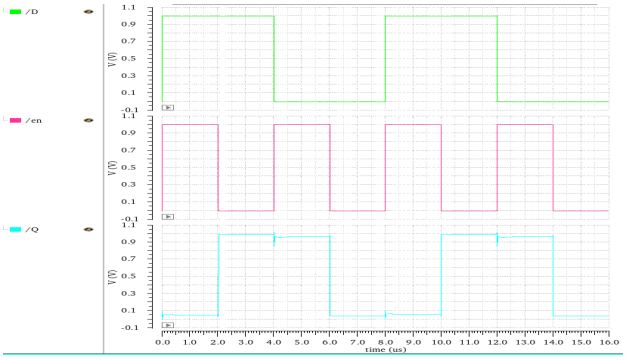
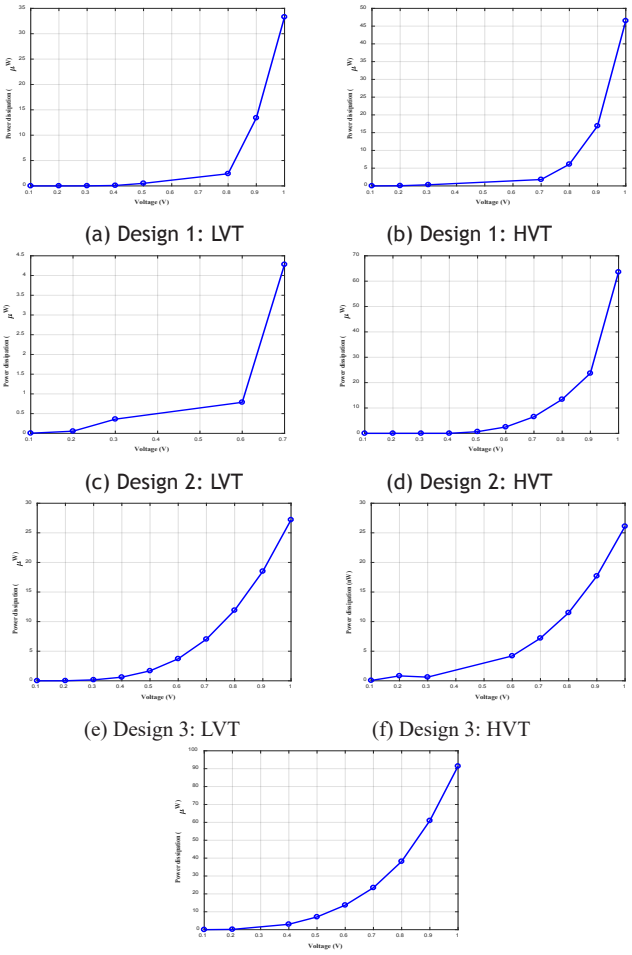


Fig. 11: Output for Design4

Table 3: Power and delay comparisons

	LVT		*HVT*	
Design	*Power*	*Delay*	*Power*	*Delay*
Design 2	0.1 mw	8 us	63.5 uw	8 us
Design 4	91.4 uw	2.00 us	83.6 uw	2.00 us
Design 1	46.5 uw	39.6 ps	33.3 uw	55.5 ps
Design 3	27.2 uw	0.336 ps	26.1 nw	44.2 ps



(a) Design 1: LVT (b) Design 1: HVT

(c) Design 2: LVT (d) Design 2: HVT

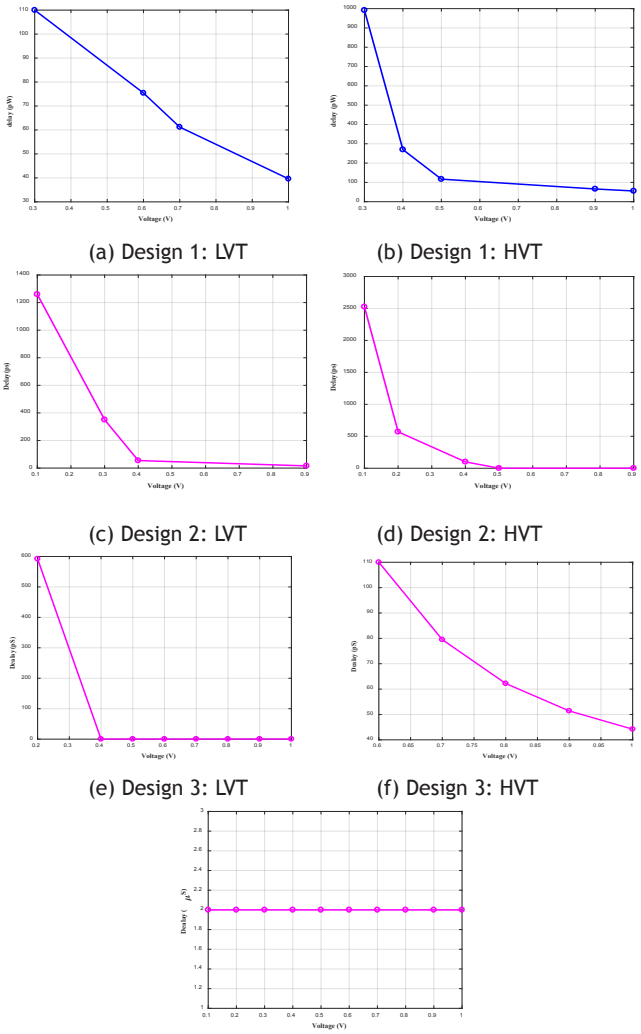
(e) Design 3: LVT (f) Design 3: HVT

(g) Design 4: LVT

Fig. 12: Power consumption Vs V_{DD}

Table 3 shows the Comparisons of Power and Delay for all the four designs. From the obtained results, it has been observed that the values of power and delay are more efficient in HVT than in LVT. Among all the four designed circuits Design3 consumes less power.

The Power and Delay values are calculated at a different range of voltages. The values are calculated with a power supply of 0.1 to 1V. These values are calculated for LVT FinFET and HVT FinFET. Based on the obtained values, power Vs Vdd and Delay Vs Vdd waveforms are plotted. Waveforms for Power Vs Vdd are shown in figure 12. Waveforms for Delay Vs Vdd are shown in figure 13.



(a) Design 1: LVT (b) Design 1: HVT

(c) Design 2: LVT (d) Design 2: HVT

(e) Design 3: LVT (f) Design 3: HVT

(g) Design 4: LVT

Fig. 13: Delay Vs VDD

Conclusion

We have presented the different approaches to designing D-Latch that consumes low power. The designed D-Latches consume less power when compared to existing latches. The circuits are designed using 18nm FinFET technology in cadence virtuoso tool. Many researchers have used CMOS technology. But FinFET has many advantages over CMOS technology. The main disadvantage of CMOS is short channel effects. These can be reduced by using FinFET because it is a multi-gate device. From the obtained results, the power and delay are reduced than the existing circuits. Among all the four designed D-Latches, design3 consumes less power when compared to others. The circuits are simulated at a supply voltage of 1V. Power and Delay values are calculated at different supply voltages. Power and Delay waveforms are plotted using the obtained values. The proposed latches can be used in power gating circuits, adders, shift registers, etc. These circuits are specifically used for low power memory applications.

References

[1] M. Alioto, R. Mita, G. Palurnbo, "Analysis and Comparison of Low-Voltage by CML D- Latch," 9th International Conference on Electronics, Circuits and Systems, Dubrovnik, Croatia, September 15-18, 2002, pp. 737-740.

[2] Jujavarapu Sravana, S.K. Hima Bindhu, K. Sharvani, P. Sai Preethi, Saptarshi Sanyal, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Implementation of Spurious Power Suppression based Radix-4 Booth Multiplier using Parallel Prefix Adders," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-6.

[3] Chandra Shaker Pittala, Vallabhuni Vijay, A. Usha Rani, R. Kameshwari, A. Manjula, D.Haritha, Rajeev Ratna Vallabhuni, "Design Structures Using Cell Interaction Based XOR in Quantum Dot Cellular Automata," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[4] S. China Venkateshwarlu, Mohammad khadir, V. Vijay, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "Optimized Design of Power Efficient FIR Filter Using Modified Booth Multiplier," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[5] G. Naveen, V.R Seshagiri Rao, Nirmala. N, Pavan kalyan. L, Vallabhuni Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, "Design of High-Performance Full Adder Using 20nm CNTFET Technology," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[6] Mohammad khadir, S. Shakthi, S. Lakshmanachari, Vallabhuni Vijay, S. China Venkateswarlu, P. Saritha, Rajeev Ratna Vallabhuni, "QCA Based Optimized Arithmetic Models," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[7] P. Ashok Babu, P. Sridhar, and Rajeev Ratna Vallabhuni, "Fake Currency Recognition System Using Edge Detection," 2022 Interdisciplinary Research in Technology and Management (IRTM), Kolkata, India, February 24-26, 2022, pp. 1-5.

[8] Koteshwaramma, K. C., Vallabhuni Vijay, V. Bindusree, Sri Indrani Kotamraju, Yasala Spandhana, B. Vasu D. Reddy, Ashala S. Charan, Chandra S. Pittala, and Rajeev R. Vallabhuni, "ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 5-13.

[9] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[10] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[11] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[12] Gollamandala Udaykiran Bhargava, Vasujadevi Midasala, and Vallabhuni Rajeev Ratna, "FPGA implementation of hybrid recursive reversable box filter-based fast adaptive bilateral filter for image denoising," Microprocessors and Microsystems, vol. 90, 2022, 104520.

[13] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[14] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[15] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[16] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[17] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[18] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[19] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," National conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.s

[20] Ratna, Vallabhuni Rajeev, and Ramya Mariserla. "Design and Implementation of Low Power 32-bit Comparator." (2021).

[21] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, "Design of Optimum Multiplexer In Quantum-Dot Cellular Automata," International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[22] J. Sravana, K.S. Indrani, Sankeerth Mahurkar, M. Pranathi, D. Rakesh Reddy, and Vijay Vallabhuni, "Optimised VLSI

Design of Squaring Multiplier using Yavadunam Sutra through Deficiency Bits Reduction," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[23] L. Babitha, U. Somanaidu, CH. Poojitha, K. Niharika, V. Mahesh, and Vallabhuni Vijay, "An Efficient Implementation of Programmable IIR Filter for FPGA," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[24] K. C. Koteswaramma, Ande Shreya, N. Harsha Vardhan, Kantem Tarun, S. China Venkateswarlu, and Vallabhuni Vijay, "ASIC Implementation of division circuit using reversible logic gates applicable in ALUs," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[25] S. Sushma, S. Swathi, V. Bindusree, Sri Indrani Kotamraju, A. Ashish Kumar, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "QCA Based Universal Shift Register using 2 to 1 Mux and D flip-flop," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[26] M. Sreevani, S. Lakshmanachari, B. Manvitha, Y.J.N. Pravalika, T.Praveen,V.Vijay, Rajeev Ratna Vallabhuni, "Design of Carry Select Adder Using Logic Optimization Technique," IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3'21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[27] M. Saritha, Chelle Radhika, M. Narendra Reddy, M. lavanya, A. Karthik, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Pipelined Distributive Arithmetic-based FIR Filter Using Carry Save and Ripple Carry Adder," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[28] S. Swathi, S. Sushma, V. Bindusree, L Babitha, Sukesh Goud. K, S. Chinavenkateswarlu, V. Vijay, Rajeev Ratna Vallabhuni, "Implementation of An Energy-Efficient Binary Square Rooter Using Reversible Logic By Applying The Non-Restoring Algorithm," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[29] Kiran, K. Uday, Gowtham Mamidisetti, Chandra shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, "A PCCN-Based Centered Deep Learning Process for Segmentation of Spine and Heart: Image Deep Learning," In Handbook of Research on Technologies and Systems for E-Collaboration During Global Crises, pp. 15-26. IGI Global, 2022.

[30] Vallabhuni Vijay, V.R. Seshagiri Rao, Kancharapu Chaitanya, S. China Venkateshwarlu, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, "High-Performance IIR Filter Implementation Using FPGA," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[31] S. Swathi, S. Sushma, C. Devi Supraja, V. Bindusree, L. Babitha and Vallabhuni Vijay, "A Hierarchical Image Matting Model for Blood Vessel Segmentation in Retinal Images," International journal of system assurance engineering and management, vol. 13, iss. 3, 2022, pp. 1093-1101.

[32] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[33] M. Lavanya, Malla Jyothsna Priya, Ponukumatla Janet, Kavuluri Pavan Kalyan, and Vijay Vallabhuni, "Advanced 18nm FinFET Node Based Energy Efficient and High-Speed Data Comparator using SR Latch," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[34] Vallabhuni Vijay, J. Sravana, K.S. Indrani, G. Ajitha, A. Prashanth, K. Nagaraja, K.C. Koteswaramma, C. Radhika, M. Hima Bindu, N. Manjula, "A SYSTEM FOR CONTROLLING POSITIONING ACCORDING TO MOVEMENT OF TERMINAL IN WIRELESS COMMUNICATION BASED ON AI INTERFACE," The Patent Office Journal No. 50/2021, India. Application No. 202141055995 A.

[35] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthilaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, "Garbage Collector with Smart Segregation and Method of Segregation Thereof," The Patent Office Journal No. 04/2022, India. Application No. 202141062270 A.

[36] Sravana, J., K. S. Indrani, M. Saranya, P. Sai Kiran, C. Reshma, and Vallabhuni Vijay, "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 14-21.

[37] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[38] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[39] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.