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Data Conversion: Realization of Code converter using Shift Register Modules

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Abstract

Barrel shifter architecture is well known for bit manipulation in a single clock cycle. Due to its various operations and advantages, it is most likely used in the Arithmetic logic unit of every processor. Gray code is also known as reflective code which is widely used in digital communication for the purpose of error correction and error detection. In this project, an 8 x 4 barrel shifter is designed which is further connected to 4-bit binary to gray code converter. The barrel shifter is cascaded with binary to gray code converter so that this combination can be useful for the application of encryption of binary data in digital communications. It is designed in cadence virtuoso tool using FinFET technology at 18 nm node. The simulation results proves that the power consumed by the proposed design with FinFET technology is 11.92% less when compared with the conventional design with MOS transistors. Hence, this design can be used in application of low power digital communications. The functionality testing and verification is done using cadence virtuoso tool.

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Introduction

An Arithmetic logic unit in a processor performs various arithmetic operations like addition, subtraction, multiplication and logical operations like AND, OR etc. Most of the operations require only operands, but few operations require sub-modules along with operands. For example, multiplication operation is done by multiplying of data using AND gate and addition of partial products using full adders or half adders. It also requires a shifter to shift partial products so that they can be added in correct format. Hence these modules play an important role in characterizing the performance of processors.[1-15]

Different types of shifters available in digital electronics. They are basically sequential shifter such as serial shifters, parallel shifters which shifts or rotates data based on clock cycle of the processor. They require n clock cycles to shift n-data bits which are not beneficial in terms of performance of the processor. To overcome this problem, ALU's are embedded with a module called Barrel shifter. A Barrel shifter as name suggests shits data either left or right based on the control shift bits configuration. It is usually consists of multiplexers connected parallel to each other. It works completely on combinational logic and shifts data in a single clock cycle. Due to its advantage, RISC processors use these barrel shifters embedded in ALU.[1] Then again, a gray code converter is used to generate gray codes for a respective binary code. The Gray code is a non-weighted binary code that has a special property that there is only a single bit difference between two sequential numbers.[3] Due to this property, it is popularly used for data error correction and detection in digital communication.[16-21]

We know that the barrel shifter block plays a vital role in performance of the device from last chapter. Due to its importance, several studies were made by researchers to improve its performance for increasing its applications. A Convention barrel shifter is built using multiplexers. Higher the order of multiplexer, higher the number of bits will be shifted or rotated in barrel shifter.[7] Different logic styles of multiplexer implementation helps in improving the performance of barrel shifter.[4] There are numerous ways to design a barrel shifter proposed by various authors using adiabatic logic.[2] Adiabatic techniques were proposed to

design architectures for reducing power consumption of multiplexers.[6] Figure 1 shows the example of Mux based 8-bit barrel shifter.[22-29]

Through adiabatic techniques, power consumption is reduced for a minimal amount, but even the architecture with numerous multiplexers occupies large area which in turn increases path delay affecting the speed of the design. It is clear that there is a need to develop a suitable transistor level design for shifting operation. Hence, it is proposed to perform a detailed study on barrel shifter design with various logic styles and to suggest suitable logic of barrel shifter for low power digital applications. Later, studies were made to reduce power consumption by changing technology from CMOS to FinFET at 18nm node.[10] This technique only allows to reduce power consumption but does not give any solution to how to reduce transistors count in barrel shifter. Another novel architecture of 8 x 4 barrel shifter is designed successfully which meets the requirements of both low power consumption and better delay performance.[11] To improve this architecture, its analysis is carried out using FinFET technology through this paper.[30-39]

FinFET Characteristics and Modelling

FinFET, also known as Fin Field Effect Transistor, is a sort of non-planar or "3D" transistor used in the architecture of modern processors. A FinFET was earliest fabricated in 1998 and tested by researchers from U. C. Berkeley. Since then, lot of work has been done during the next few years on FinFET. This led to the commercialization of FinFET devices in 2012.[12] Intel launched their first 22 nm FinFET (Tri-Gate) processor in 2012. Figure 2 shows constructional difference between a conventional MOSFET and FinFET.

The working of FinFET is similar to MOSFET, the only difference FinFET has is its sophisticated construction. FinFET is dividing into two types namely

1. Bulk FinFET
2. Silicon-On-Insulator (SOI) FinFET

The various types of FinFET are classified on the 'base' onto which it is fabricated. This implies FinFET can be made either on Silicon-On-Insulator (SOI) wafers or normal silicon wafers. Contrasted with the more regular planar technology, FinFET transistor technology offers some critical favorable circumstances in the IC structure. Advantages include reduce in short channel effects and higher gain, excellent mobility, scalability, trans- conductance.[13] In digital electronic circuits, the major advantage of Field-Effect Transistors (FET) is to act as a logic switch, in which the current flowing through drain (ID) is controlled by the gate to source voltage (VGS). Faster switches can be designed with smaller devices which improves response time. In 1965, Moore's law predicted that the transistor density in an IC will increase exponentially for every four years. Since, the feature size of the transistors started to be lesser than 1µm, the Moore's law became difficult to be accomplished and some undesirable effects started to effect the transistor behavior. It happens because the source and drain terminals of the MOSFET become to be closer.[14-21]

As a result of that, the gate terminal of the MOSFET starts to lose the control of the channel. Those undesirable effects which causes negative behaviour of transistor are called "short-channel effects" (SCE).[22-25]. Usually, short-channel effects are seen when the controllability of the channel region by the gate that is affected by transistor minimization.[26] There are five types of short channel effects such as drain-induced barrier lowering, surface scattering, velocity saturation, impact ionization and hot electron effect. Due to these effects, it became impossible to reduce channel length in CMOS technology which internally uses NMOSFET and PMOSFET.

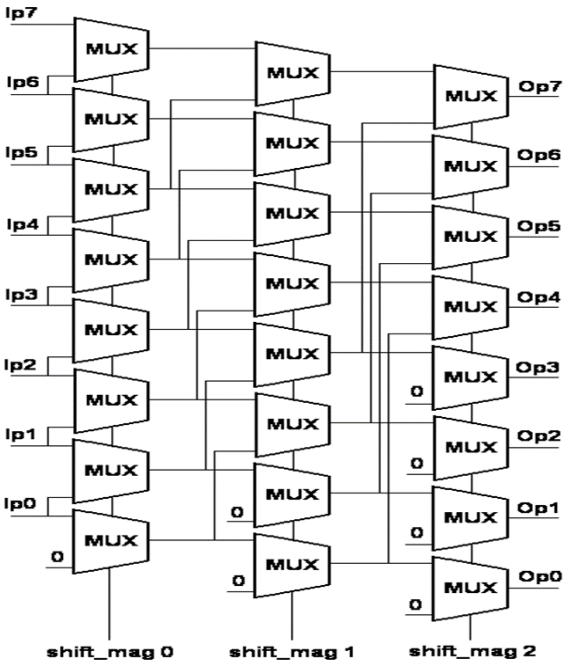

Fig. 1: MUX based Barrel shifter

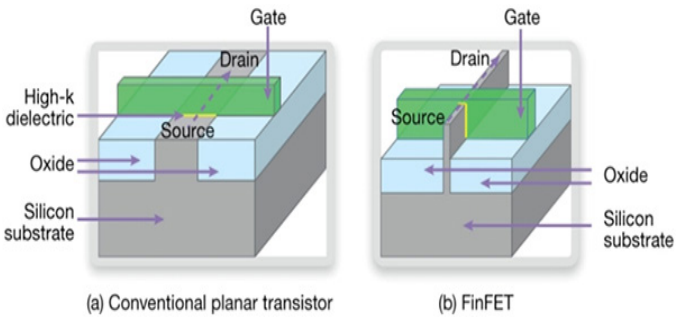

Fig. 2: a) Conventional MOSFET and b) FinFET

Hence, there is drift in transistor manufacture from CMOS to FinFET technology.[27-40]

Proposed barrel shifter circuit Using FinFET Models

The design was based on the idea of pass transistor logic. It is an 8×4 barrel shifter which means it takes 8 input bits and shifts them according to 5 shift bits and generates 4 output bits.

The table 1 explains the working of the barrel shifter shown in figure 3. The schematic diagram of 8×4 barrel shifter is constructed using NHVT (similar to NMOS in terms of functionality) transistor. There are 8 input bits of shifter as a0, a1, a2, a3, a4, a5, a6, a7 and output bits are b0, b1, b2, b3, respectively. The five control signals are sh0 to sh4 which are used for shifting operation as shown in figure 3. The gate terminal of each transistor in a column is provided with one control shift signal as input. For example, the first column transistors have control signal Sh0 is connected to each of their gate terminal. During the operation of the schematic, only one control signal (either sh0 or any one of sh1-sh4) is enabled high and others are enabled low.

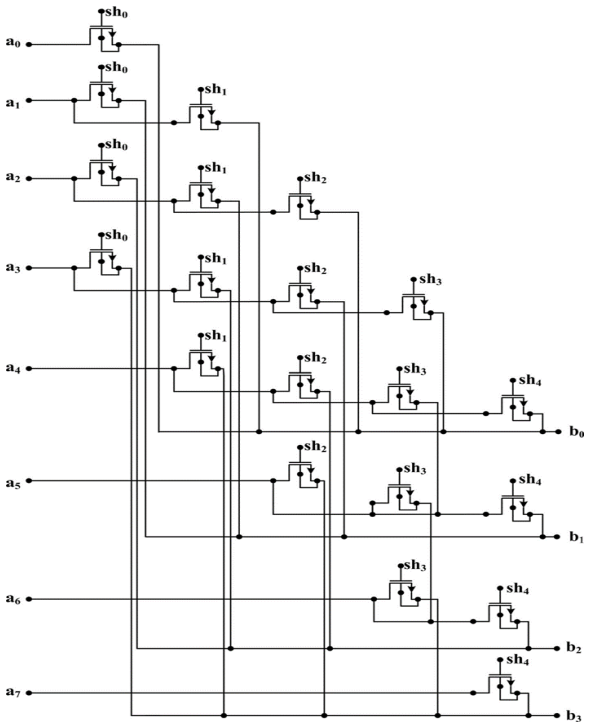

Fig. 3: Schematic diagram of 8 × 4 barrel shifter.

Table 1: Truth table for control shift bits in 8 × 4 barrel shifter

Control shift bits					*Output bits*			
Sh0	*Sh1*	*Sh2*	*Sh3*	*Sh4*	*B0*	*B1*	*B2*	*B3*
1	0	0	0	0	a0	a1	a2	a3
0	1	0	0	0	a1	a2	a3	a4
0	0	1	0	0	a2	a3	a4	a5
0	0	0	1	0	a3	a4	a5	a6
0	0	0	0	1	a4	a5	a6	a7

According to Table 3, whenever sh0 is enabled then output lines are at b0=a0, b1=a1, b2=a2, b3=a3. For the next clock cycle, when Sh1 is made high then the input bits are shifted right by one position. For the input bit pattern a0 =1, a1=1, a2=0, a3=1, a4=0, a5=0, a6=0, a7=1 and control bits as sh0=1, sh1=0, sh2=0, sh3=0, sh4=0, output becomes b0=1, b1=1, b2=0, b3=1. The barrel shifter is designed and tested using cadence tool. The schematic of the design using NHVT transistor (N-type FinFET) is shown figure 4.

A code converter converts the binary data to different codes. Out of all codes, gray codes have its application in many domains. A gray code is also known as reflective code. A binary code is converted to gray code by doing XOR operation between given bits. For example if the binary data is b3, b2, b1 and b0 the gray code can be calculated by using the following equations.

$$G3 = B3 \tag{3.1}$$

$$G2 = B3 \oplus B2 \tag{3.2}$$

$$G1 = B2 \oplus B1 \tag{3.3}$$

$$G0 = B1 \oplus B0 \tag{3.4}$$

Since it takes a 4-bit binary data, all the fifteen possibilities are tested by the code converter designed in cadence tool using the following truth table.

The gray code converter is designed in Cadence Spectre tool. To construct the design, first sub-modules are to

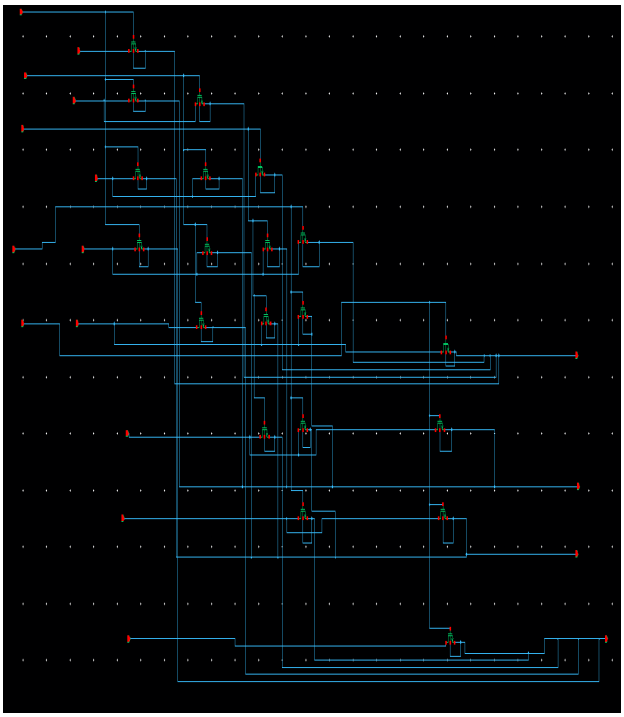

Fig. 4: Schematic diagram of 8×4 barrel shifter designed using FinFET in Cadence tool

be designed. In this XOR gates as well as inverters are designed using NHVT transistor is shown in figure 6. Later on, all the gates are integrated to design the gray code converter as shown in following figure 6.

The idea of cascading the barrel shifter with reflexive code converter is to encrypt the binary data by doing data manipulation and transmit them after converting to gray code. This Encryption helps in data security purposes and the code conversion helps in detecting errors and correcting them in future. The Integration of 8 × 4 Barrel shifter with 4-Bit Binary to reflexive Code Converter is done in Cadence tool as shown in figure 8.

The working of barrel shifter and binary to reflexive code converter is follows: After cascading of barrel shifter, the entire design is tested for functionality for five combinations. Since, barrel shifter has 5 shift signals for each combination only one control signal will be enabled and respective data will be given input to code converter

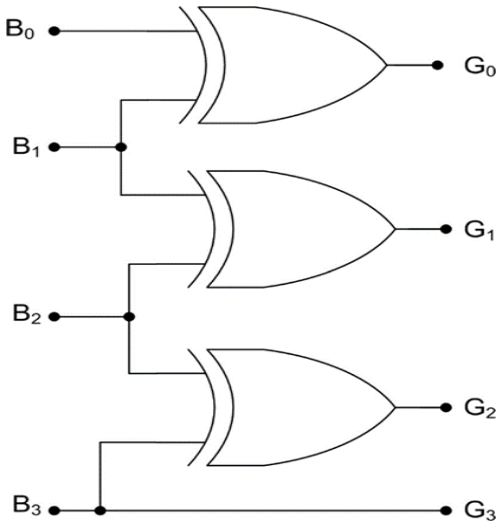

Fig. 5: Logic circuit for 4-bit binary to Gray code converter circuit

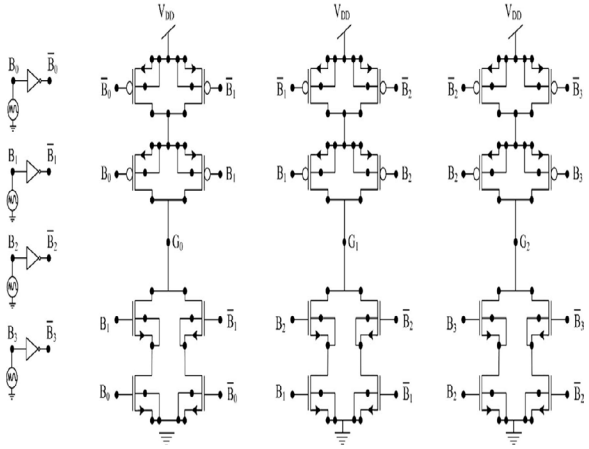

Fig. 6: Implementation of 4-bit binary to gray code converter circuit in transistor level.

to generate gray code. For example, if Sh0 is enabled and sh1-sh4 are disables the input lines a0-a4 are the binary data which are converted to gray codes. This process continues till all the 8 bit input data is manipulated and converted to gray code.

Simulation Results and Experimental Findings of the Proposed Work

The results and simulations for all the described architectures have been performed using cadence virtuoso tool.

Table 2. Truth table of Gray code converter

Binary data				Reflexive code data			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1

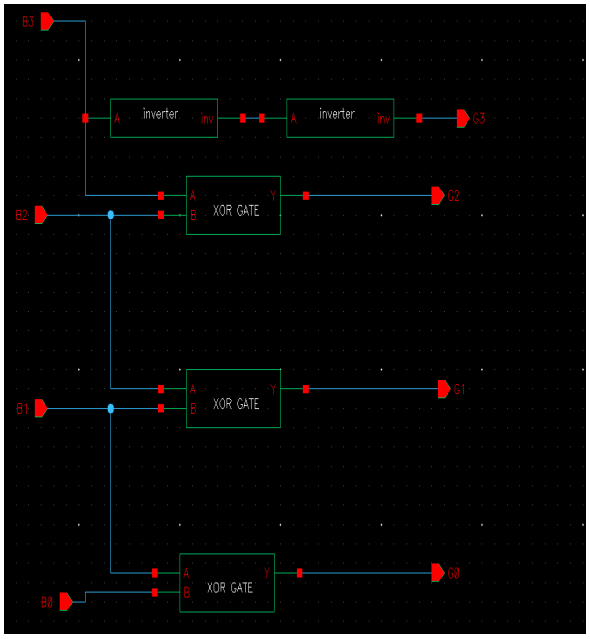

Fig. 7: Implementation of 4-bit binary to gray code converter circuit in gate level using FinFET technology in Cadence tool.

In this section the power and delay comparisons between the conventional and proposed schematics have been made. The metrics considered for the comparison are: power consumption, average delay, PDP and EDP. Regarding the delay, we noted the delay that occurs between inputs to outputs transitions, given in nanoseconds (ns). For all the examined schematics transient analysis is done for both power and delay calculations.

The following simulation waveforms figure 9 – 13 are for the above schematic designed in cadence tool at 18 nm technology. It uses Analog design environment (ADE L) tool which supports both transient analysis and DC analysis. The figure 9 shows the timing diagram of proposed design when control shift signal Sh0 is enabled.

The figure 10 shows the timing diagram of proposed design when control shift signal Sh1 is enabled.

The figure 11 shows the timing diagram of proposed design when control shift signal Sh2 is enabled. Therefore the input to shift signals would be Sh0=0, Sh1=0, Sh2=1, Sh3=0 and Sh4=0, respectively.

The figure 12 shows the diagram of proposed design when control shift signal Sh1 is enabled. Therefore the input to shift signals would be Sh0=0, Sh1=0, Sh2=0, Sh3=1 and Sh4=0, respectively.

The figure 13 shows the timing diagram of proposed design when control shift signal Sh1 is enabled. Therefore the input to shift signals would be Sh0=0, Sh1=0, Sh2=0, Sh3=0 and Sh4=1, respectively.

It is evident from simulation results that for different combinations of shift signals the binary data is converted into gray codes.

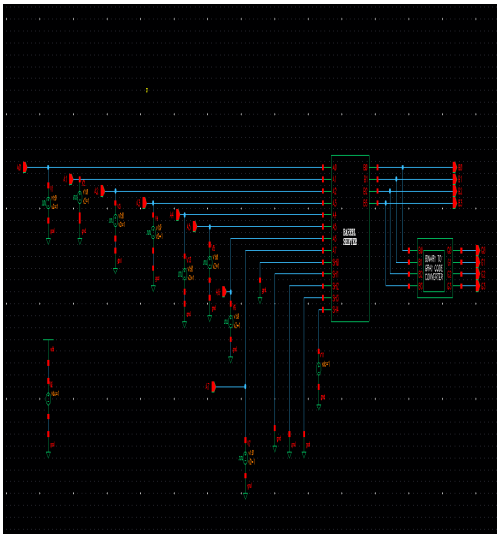

Fig. 8: Schematic showing integration of 8 x 4 Barrel shifter with 4-Bit Binary to Gray Code Converter

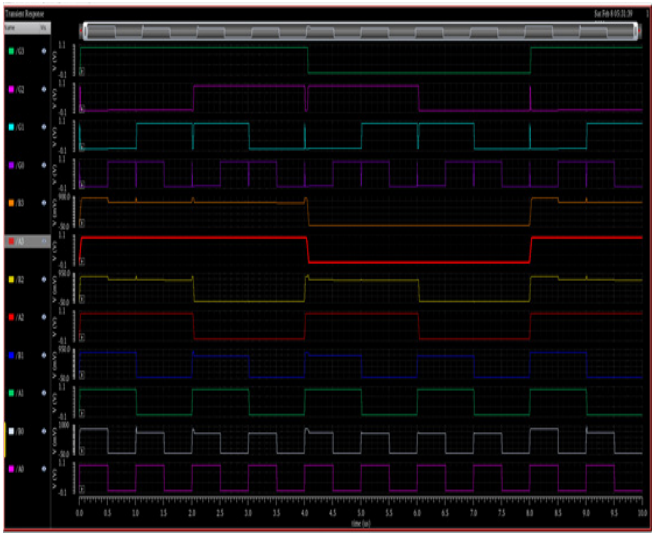

Fig. 9: Output waveform of gray code converter with only Sh0 enabled

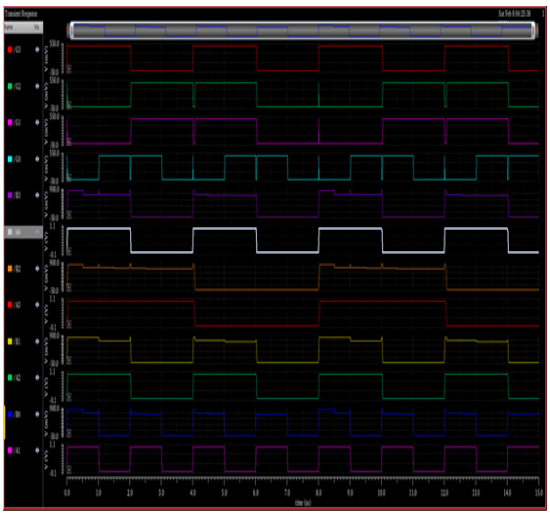

Fig. 10: Output waveform of gray code converter with only Sh1 enabled

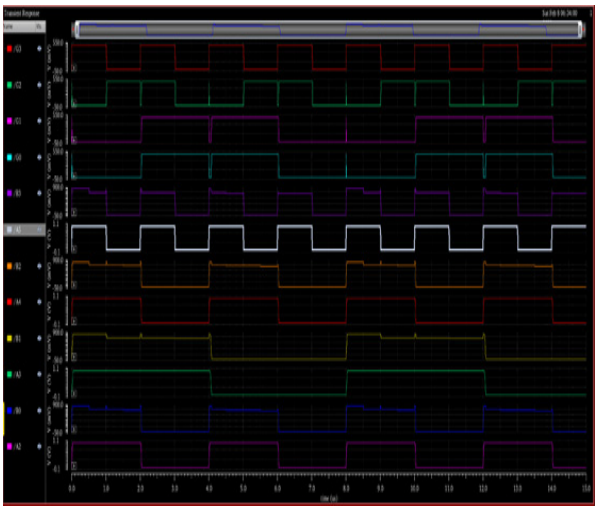

Fig. 11: Output waveform of gray code converter with only Sh2 enabled

Power Consumption

The power consumed by the code converter is noted through simulation and given in Table 3. It is seen from the outcomes that the proposed structure contributes lesser power utilization than that of the existing plan. This is due to the implementation of its design topology, which builds the transistor scalability significantly, in this manner lessens the overall power consumption. It is calculated by DC analysis with ADE L tool. Results show that power consumption is directly proportional to power supply voltage V_{DD}. It is also represented further by plotting recorded values against different voltage supplies.

From the table 14, it is noticed that power consumed by gray code converter is nearly less than half of the value at 0.5 volts. At 1volt V_{DD}, power consumption is reduced 11.92% when compared with gray code converter with MOS transistors. The Power consumption (μW) of proposed design using FinFET transistors at 18 nm technology with respect to V_{DD} is visualized using a scatter plot as shown in figure 14.

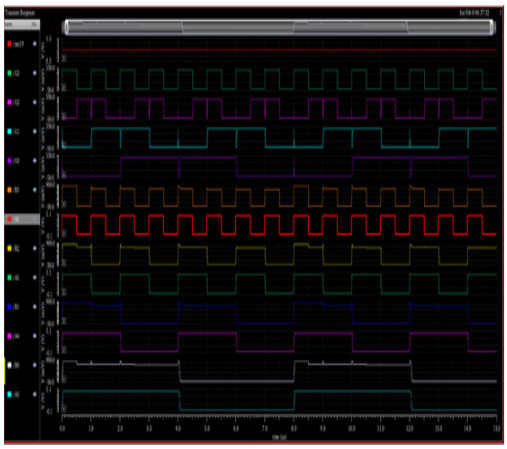

Fig. 12: Output waveform of gray code converter with only Sh3 enabled

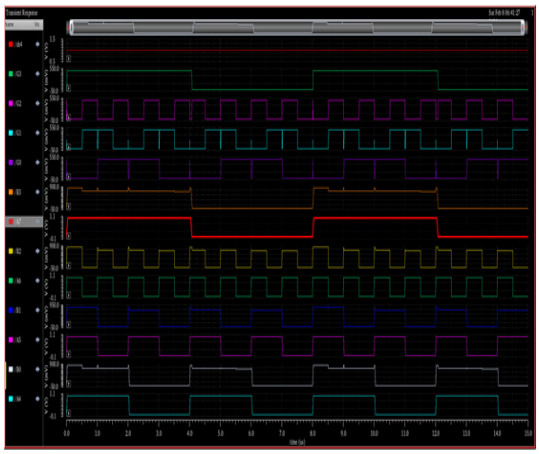

Fig. 13: Output waveform of gray code converter with only Sh4 enabled

Table 3: Comparison between power consumption of gray code converter using MOSFET and FinFET transistors.

Voltage(V)	Power consumption (μW) of 4-bit Gray code converter using MOS transistors at 150 nm technology	Power consumption (μW) of 4-bit Gray code converter using FinFET transistors at 18 nm technology
0.5	0.0324	0.0105
0.6	0.048	0.012
0.7	0.069	0.035
0.8	0.0907	0.058
0.9	0.118	0.0895
1	0.151	0.133
1.1	0.192	0.191
1.2	0.246	0.24

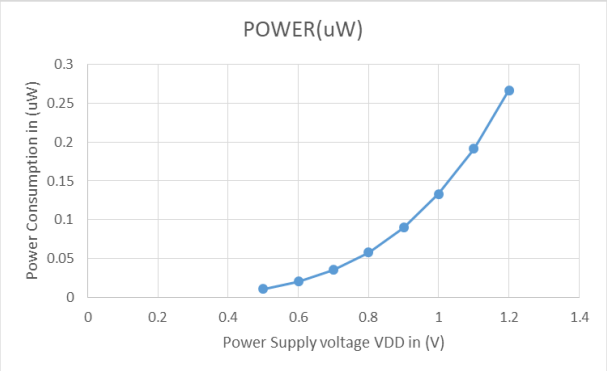

Fig. 14: Visualization for the power consumption of proposed design corresponding V_{DD}

Table 4: Path delay, PDP and EDP of proposed design with control shift signal 10000 at 18 nm node

Voltage (v)	*Power (μW)*	*Delay (ns)*	*Power delay Product ($x10^{-15}$ J)*	*Energy delay Product ($x10^{-24}$ J sec)*
0.5	0.0105	5.116	0.05	0.27
0.6	0.01994	5.02	0.1	0.50
0.7	0.035	4.88	0.17	0.83
0.8	0.0575	3.99	0.22	0.91
0.9	0.0895	3.956	0.35	1.40
1	0.133	3.55	0.47	1.67
1.1	0.1915	3.45	0.66	2.27
1.2	0.267	3.44	0.91	3.15

Analysis of delay, power-delay product and energy-delay product with control signal 10000 configuration: ss

The delay parameter always plays a vital role in determining the performance of a design [14]. After simulating the gray code converter designed with FinFET transistor for the combination of control shift signal as 10000, final results are obtained for delay, PDP and EDP and are shown in Table 4. Simulations have been carried out at 18nm technology in cadence virtuoso tool.

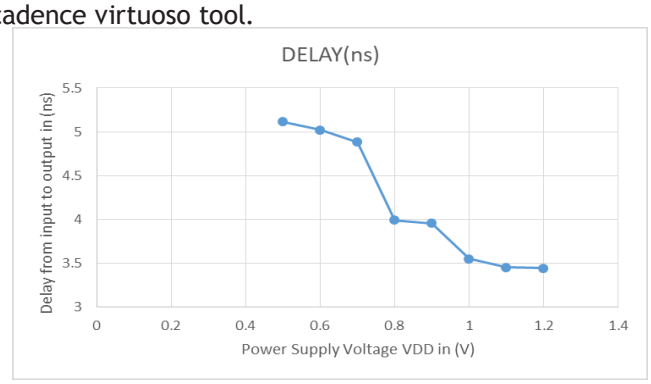

Fig. 15: Visualization for the delay of proposed design corresponding to V_{DD} with control shift signal 10000.

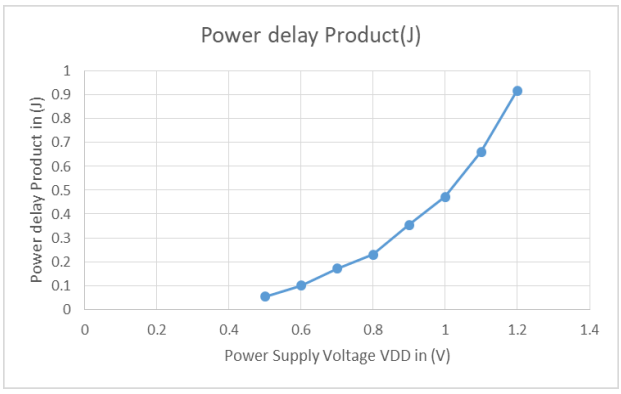

Fig. 16: Visualization for the power-delay product of proposed design corresponding to V_{DD} with control shift signal 10000

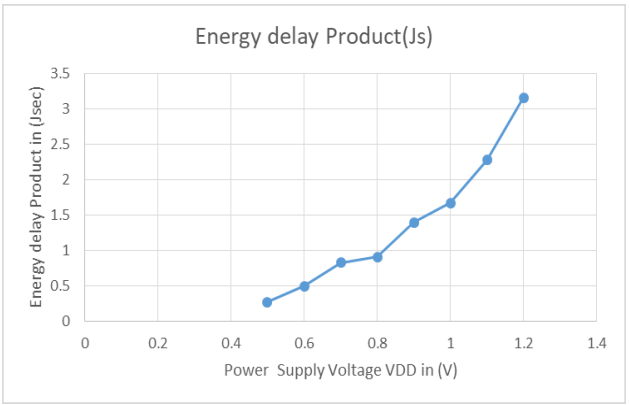

Fig. 17: Visualization for the energy-delay product of proposed design corresponding to V_{DD} with control shift signal 10000

The control shift signals that are enabled for this performing transient analysis are Sh=1, Sh=0, Sh2=0, Sh3=0 Sh4=0, respectively. The control signal Sh0 is enabled such that inputs a0 to a3 bits are traversed to cascading block of gray code converter.

The Path delay (nS) of proposed design using FinFET transistors at 18 nm technology considering V_{DD}, with control shift signal 10000 is visualized using a scatter plot as shown in figure 15.

The power-delay product (PDP) is calculated by product of power and delay as shown in table 4. The PDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with control shift signal 10000 is visualized using a scatter plot as shown in figure 16.

The Energy- efficient designs with less PDP may also performs very slowly, hence energy-delay product (EDP) which is product of energy and delay (or power and delay2) is sometimes a preferable parameter. The EDP is proportional to V_{DD}.

Analysis of delay, power-delay product and energy-delay product with control signal 01000 configuration:

In this section, the parameter analysis of delay, PDP and EDP of 4-bit binary to gray code converter with control signal combination of 01000 are carried out. The table

Table 5: Path delay, PDP and EDP of 4-bit binary to gray code converter circuit with control shift signal 01000 at 18 nm node

Voltage (v)	*Power (μW)*	*Delay (ns)*	*Power delay Product (x10-15 J)*	*Energy delay Product (x10-24 J sec)*
0.5	0.010	5.00	0.052	0.26
0.6	0.019	4.372	0.087	0.38
0.7	0.035	4.172	0.146	0.60
0.8	0.057	4.03	0.231	0.93
0.9	0.089	4.004	0.358	1.43
1	0.133	3.95	0.525	2.07
1.1	0.191	3.93	0.752	2.95
1.2	0.267	3.899	1.041	4.05

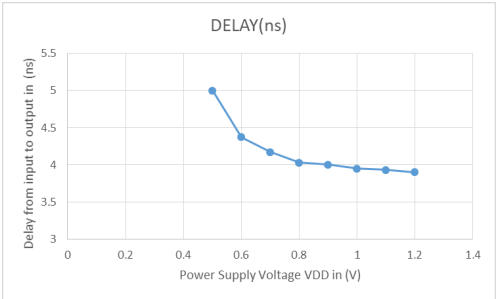

Fig. 18: Visualization for the delay of proposed design corresponding to V_{DD} with control shift signal 01000.

5 shows the results of metrics with respect to V_{DD} using FinFET technology at 18 nm node.

The control shift signals that are enabled for this performing transient analysis are Sh=0, Sh=1, Sh2=0, Sh3=0 Sh4 =0 respectively. The control signal Sh1 is enabled such that inputs a1 to a4 bits are traversed to cascading block of binary to gray code converter. The Path delay (nS) of proposed design using FinFET transistors at 18 nm technology with respect to V_{DD} is visualized using a scatter plot as shown in figure 18.

The Power-delay product specifies the amount of energy consumption per performed or switching event. The PDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with the combination of control shift signal as 01000 is visualized using a scatter plot as shown in figure 19.

The EDP of proposed design using FinFET transistors at 18 nm technology considering V_{DD}, with control shift signal 01000 is visualized using a scatter plot as shown in figure 20.

Analysis of delay, power-delay product and energy-delay product with control signal 00100 configuration

In this section, the parameter analysis of delay, PDP and EDP of 4-bit binary to gray code converter with control signal combination of 00100 are carried out. The table 6 shows the results of metrics with respect to V_{DD} using FinFET technology at 18 nm node. The control shift signals that are enabled for this performing transient analysis are Sh=0, Sh=0, Sh2=1, Sh3=0 and Sh4 =0 respectively. The control signal Sh2 is enabled such that inputs a2 to a5 bits are traversed to cascading block of gray code converter.

The Path delay (nS) of proposed design using FinFET transistors at 18 nm technology with respect to V_{DD}, with the combination of control shift signal as 00100 is visualized using a scatter plot as shown in figure 21.

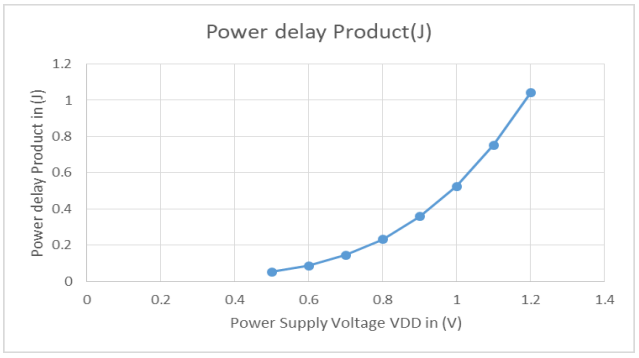

Fig. 19: Visualization for the power-delay product of proposed design corresponding to V_{DD} with control shift signal 01000

The PDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with the combination of control shift signal as 00100 is visualized using a scatter plot as shown in figure 22.

The EDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with control shift signal 00100 is visualized using a scatter plot as shown in figure 23.

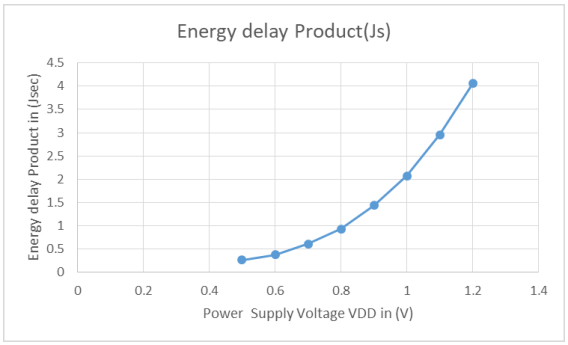

Fig. 20: Visualization for the energy-delay product of proposed design corresponding to V_{DD} with control shift signal 01000

Table 6: Path delay, PDP and EDP of 4-bit binary to gray code converter circuit with control shift signal 00100 at 18 nm node.

Voltage (v)	*Power (μW)*	*Delay (ns)*	*Power delay Product (x10-15 J)*	*Energy delay Product (x10-24 J sec)*
0.5	0.0105	4.66	0.049	0.23
0.6	0.01994	4.274	0.085	0.36
0.7	0.035	4.152	0.145	0.60
0.8	0.0575	4.159	0.24	0.99
0.9	0.0895	4.029	0.36	1.45
1	0.133	3.959	0.52	2.08
1.1	0.1915	2.927	0.56	1.64
1.2	0.267	1.494	0.39	0.59

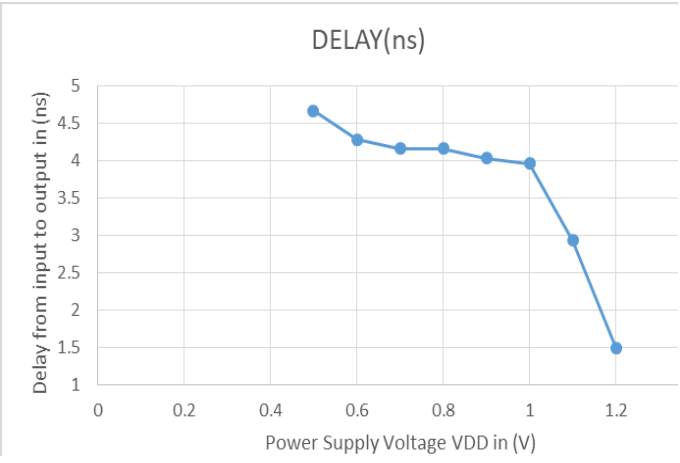

Figure 21. Visualization for the delay of proposed design corresponding to V_{DD} with control shift signal 00100.

Analysis of delay, power-delay product and energy-delay product with control signal 00010 configuration:

In this section, the parameter analysis of delay, PDP and EDP of 4-bit binary to gray code converter with control signal combination of 00010 are carried out. The table 7 shows the results of metrics with respect to V_{DD} using FinFET technology at 18 nm node.

The control shift signals that are enabled for this performing transient analysis are Sh=0, Sh=0, Sh2=0, Sh3=1 and Sh4 =0, respectively. The control signal Sh3 is enabled such that inputs a1 to a4 bits are traversed to cascading block of gray code converter.

The Path delay (nS) of proposed design using FinFET transistors at 18 nm technology with respect to V_{DD}, with the combination of control shift signal as 00010 is visualized using a scatter plot as shown in figure 24.

The PDP of proposed design using FinFET transistors at 18 nm technology corresponding to VDD, with the combination of control shift signal as 00010 is visualized using a scatter plot as shown in figure 25.

The EDP of proposed design using FinFET transistors at 18 nm technology corresponding to VDD, with control shift signal 00010 is visualized using a scatter plot as shown in figure 26.

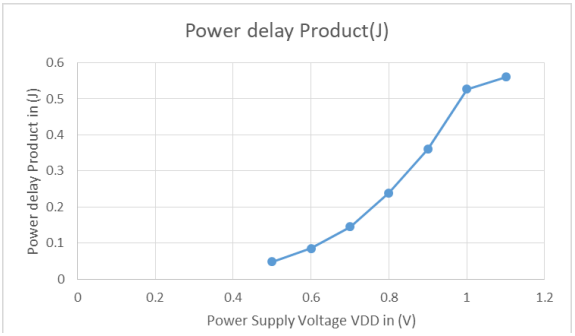

Fig. 22: Visualization for the power-delay product of proposed design corresponding to V_{DD} with control shift signal 00100.

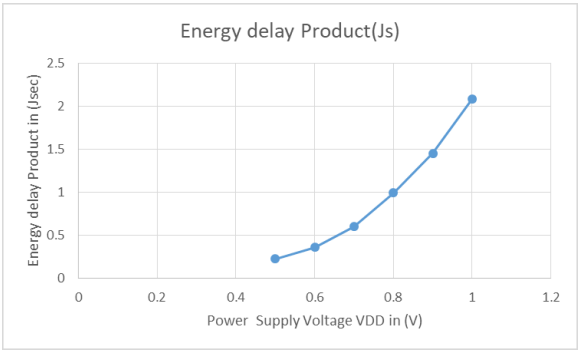

Figure 23. Visualization for the energy-delay product of of proposed design corresponding to V_{DD} with control shift signal 00100.

Analysis of delay, power-delay product and energy-delay product with control signal 00001 configuration:

In this section, the parameter analysis of delay, PDP and EDP of 4-bit binary to gray code converter with control signal combination of 00001 are carried out. The table 8 shows the results of metrics with respect to V_{DD} using FinFET technology at 18 nm node.

Table 7: Path delay, PDP and EDP of 4-bit binary to gray code converter circuit with control shift signal 00010 at 18 nm node

Voltage (v)	*Power (μW)*	*Delay (ns)*	*Power delay Product (x10-15 J)*	*Energy delay Product (x10-24 J sec)*
0.5	0.0105	4.911	0.051	0.25
0.6	0.01994	4.42	0.089	0.39
0.7	0.035	4.35	0.15	0.66
0.8	0.0575	4.23	0.24	1.02
0.9	0.0895	4.008	0.35	1.43
1	0.133	3.85	0.51	1.97
1.1	0.1915	3.55	0.67	2.41
1.2	0.267	2.89	0.77	2.23

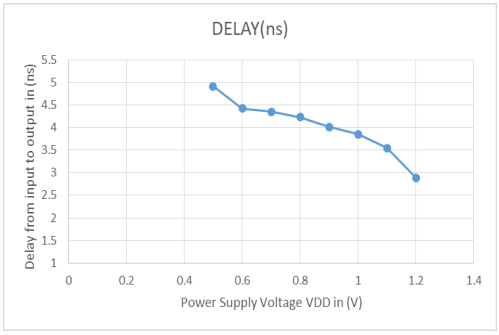

Figure 24. Visualization for the delay of proposed design corresponding to VDD with control shift signal 00010.

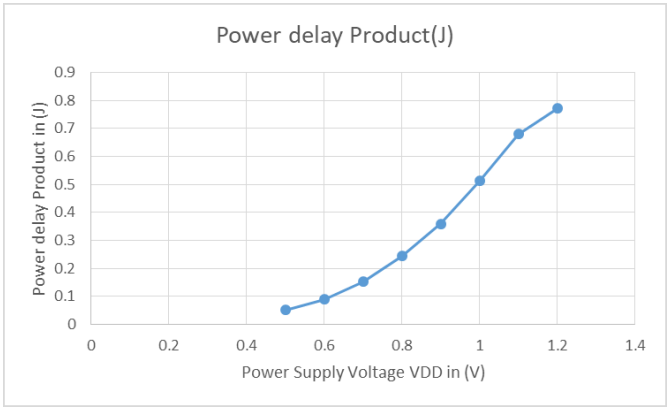

Figure 25. Visualization for the power-delay product of proposed design corresponding to V_{DD} with control shift signal 00010

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The control shift signals that are enabled for this performing transient analysis are Sh=0, Sh=0, Sh2=0, Sh3=0 and Sh4 =1 respectively. The control signal Sh4 is enabled such that inputs a1 to a4 bits are traversed to cascading block of gray code converter to generate gray codes.

The Path delay (nS) of proposed design using FinFET transistors at 18 nm technology considering V_{DD}, with the combination of control shift signal as 00001 is visualized using a scatter plot as shown in figure 27.

The PDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with the combination of control shift signal as 00001 is visualized using a scatter plot as shown in figure 28.

The EDP of proposed design using FinFET transistors at 18 nm technology corresponding to V_{DD}, with control shift signal 00001 is visualized using a scatter plot as shown in figure 29.

Thus, through simulation of results power consumed by the design as well as delay, PDP and EDP of 4-bit binary to gray converter for each and every combination of control shift signal is accomplished. Results show that power consumption is same for different combinations of control shift signals, but path delay, PDP and EDP changes from one another.

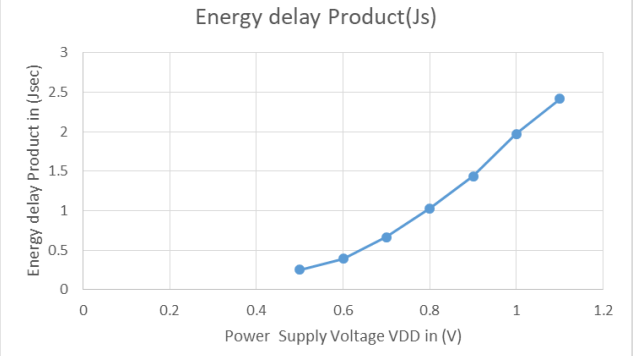

Fig. 26: Visualization for the energy-delay product of proposed design corresponding to V_{DD} with control shift signal 00010

Table 8. Path delay, PDP and EDP of 4-bit binary to gray code converter circuit with control shift signal 00001 at 18 nm node.

Voltage (v)	*Power (µW)*	*Delay (ns)*	*Power delay Product (x10-15 J)*	*Energy delay Product (x10-24 J sec)*
0.5	0.0105	4.76	0.049	0.24
0.6	0.01994	4.283	0.085	0.36
0.7	0.035	4.151	0.145	0.60
0.8	0.0575	4.03	0.23	0.93
0.9	0.0895	4.001	0.35	1.43
1	0.133	3.95	0.52	2.07
1.1	0.1915	3.65	0.69	2.55
1.2	0.267	2.89	0.77	2.23

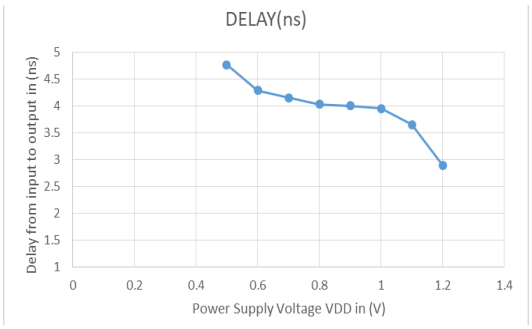

Fig. 27: Visualization for the delay of proposed design corresponding to V_{DD} with control shift signal 00001

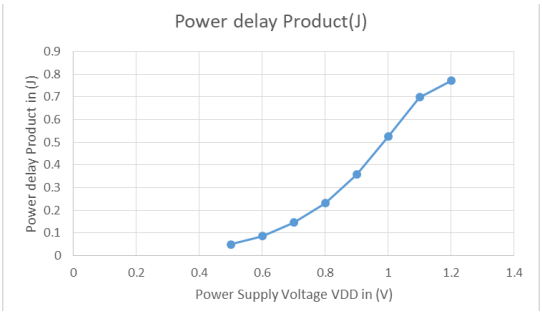

Fig. 28: Visualization for the power-delay product of proposed design corresponding to V_{DD} with control shift signal 00001

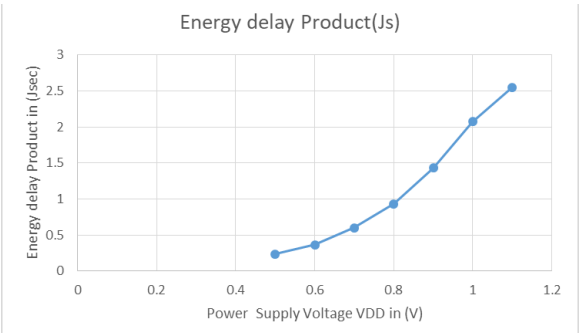

Fig. 29: Visualization for the energy-delay product of proposed design corresponding to V_{DD} with control shift signal 00001

Conclusion

In this study, an energy efficient 4 bit binary to Gray converter with 8 × 4 Barrel shifter is designed based on a new logical structure that focus mainly on power reduction by using FinFET and compared with the same design which uses MOS transistors. It is tested and simulated in Analog design environment (ADE L) tool. All the power and delay calculations were done in transient analysis and the simulation results indicated that the schematic model designed with FinFET have comparatively low power dissipation, less power delay product. The power consumed by proposed model has a power decrease of 11.92%. Hence, this design is useful in encrypting the data in digital communication with low power applications. In

future, the work can be continued by analyzing the design under different temperatures with different power supply voltages ranging from 0.5 volts to 1.2 volts, respectively. The proposed designed may be tested with advanced technologies than FinFET such as tunnel FET, carbon nanotube field-effect transistor (CNTFET) and many more. Different transistors has different behavior and properties. So the proposed designed can be designed with those transistors and can be compared with the one that was designed in this thesis for bright insights.

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