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Flip-Flop Realization: Conventional Memory Elements Design with Transistor Nodes

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Abstract

In the ultra-low-power implementation, center circuits of numerous frameworks are activated by inadequate occasions, for example, the Internet of Things (IoT) sensors and implantable clinical consideration. To guarantee that, the sensors get each and every occasion showing up whenever the circuits operate in standby mode the most of the time. Under such conditions, static power dominates in the total power consumption. For these implementations, the lessening framework leakage current can straightforwardly accomplish the greatest effectiveness of the complete framework power utilization. Since the SRAM cluster takes up a bigger bit of the circuit, it is important to decrease the power utilization of the SRAM exhibit so as to lessen circuit all-out power. Band-to-band tunneling (BTBT) mechanism introduced silicon tunnel FET (TFET), MOSFET compatible fabrication process and ultra-steep SS, which can break the 60mV/dec limitation of MOSFET at room temperature and ultra-low off-state current. Subsequently, it is required to be a promising contender for an ultra-low-power rationale circuit. The impact of forward p-I-n leakage current could prompt harm to the static noise margin (SNM), static power and power defer result of the SRAM circuit. So the proposed topology can stay away from the p-I-n intersection, by expanding SRAM cell read and hold static noise margin (SNM) and diminishing static power utilization drastically.

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Introduction

As process technologies still advance, the speed of SRAMs will increase, but devices are going to be more at risk of mismatches, which worsen the static- noise margin of SRAM cells. Because of stability concerns, the twin port designs that implement read disturb-free feature like that seen within the 7T and 8T cell implementation might become more practical in the futures RAM cell implementation.[1-5] Zone scaling abilities of numerous types of SRAM, edge help answers for voltage changeability issues, which depend on different endeavors from 6T to 8T and 10T, yet additionally fuse of various voltage supply for cell terminal biasing and having arrangement controls of read and write activity was thought about, the varieties in SRAM arrangements were investigated considering an effect on the necessary territory overhead for each plan arrangement given by ever-expanding irregular varieties. Unlike the DRAM cell, total power consumption, static power dissipation, dynamic power dissipation, static current and area which will affect the speed of operation of novel SRAM cell. Therefore, the power dissipation can have a significant effect on the performance of the memory design.[6-11] The parameters such as SNM, power, read and write are needed to be considered for planning of SRAM. Some methods might not guarantee the thermal stability of the memory system, thus a unifying framework for analysis and magnificence of 8T and 10T cell design for SRAM is to be considered. It is clear that there is a necessity to develop an acceptable transistor level design for memory system with varying temperature conditions. Hence, it's proposed to perform in depth study on SRAM memory

design with various low power logic circuits and to suggest suitable logic of SRAM cell for low power applications. The subsequent gate of FinFET can be utilized to control the limit voltage of the gadget, accordingly permitting quick turning on one side and diminished leakage current when circuits are inactive.[12-17]

SRAM is one among the recollections for the most part utilized in the storage memory of gadgets. Memory Cells (SRAM) need to be quicker, consume less power devouring and reliable. But then, this is influenced by MOSFET scaling process varieties. The previous 4-5 decades CMOS scaling starting with one innovation hub then onto the next hub has given improved execution. This empowered in creating littler, quicker and incredible advanced frameworks. Be that as it may, scaling of the CMOS results in a ton of difficulties because of the material used and procedure innovation beyond level. To beat the resultant raise in the static power consumption in chips, various device structures like Fully Depleted Silicon on Insulator (FDSOI) and FinFETs are developed and are now under production with the technology nodes below 7 nm.[18]

In order to improve the parameters such as read and write 10T FinFET based SRAM cells have been proposed. There are many issues in the parameters like write and read delays which are very long and wide for read, write operations in the sub threshold area of the CMOS based 10T SRAM cell. While reading it is observed that CMOS based 10T SRAM cell is touchy to clamor. So to decrease these issues, 10T FinFET based SRAM cell is presented. In READ '0' operation RBL line is precharged to VDD and WR is kept HIGH. By keeping the WL line as LOW, the write access FETs (TN3 & TN5) are in OFF state. As RBL and WR are ON TN7 is ON. If QB is logic HIGH, then TN8 is ON. As TN7 and TN8 are ON, RBL discharges to GND through TN7 and TN8. As RBL discharged we can verify that the value stores in QB is logic HIGH ('1'). In READ '1' operation RBL line is precharged to VDD and WR is kept at logic '1'. The WL line is kept LOW, the write access FETs (TN3 and TN5) are in OFF state. As RBL and WR are ON, TN7 is ON. If QB is logic LOW, then TN8 is OFF. As TN7 is ON and TN8 is OFF, RBL can't discharges to GND through TN7 and TN8. As RBL won't discharged we can verify that the value stores in QB is logic LOW ('0').In WRITE operation, the data which has to be written is loaded on BL and BLB through write driver. For WRITE operation, WL is set to HIGH and WR, RBL is set LOW. In WRITE '1' operation BL is made '0' and BLB as '1'. TN5 and TN6 are ON in this state. As QB is '1' in WRITE '1' operation, Qb discharges through TN5 and TN6 to GND making QB as LOW. As QB is LOW, Q is logic HIGH ('1'). In WRITE '0' operation WL, BL are HIGH then TN3 and TN4 are ON. As Q is '1' in WRITE '0' state, Q discharges to GND through TN3 and TN4 making Q as logic LOW ('0').[19-23]

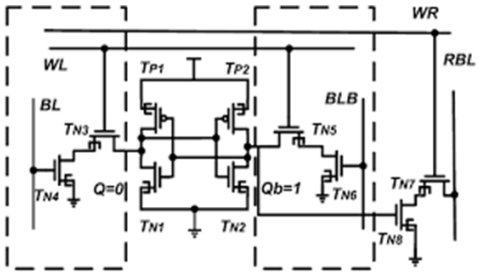


Fig. 1: Conventional 10T SRAM

FinFET Characteristics and Modeling

FinFETs are referred as multi-gate devices. By replacing the planar configuration of the standard single-gate MOSFETs, they can be characterized by a gate electrode wrapped around several sides of the conducting channel. The electrostatic control of the gate can be increased by using the transistors which are of multi gate. This also allows the decrement in leakage power as well as the short channel effects which are present inside the device. The following next years, transistors are likely to get reduced to some nanometers and further diminish of the transistors are practically impossible.[23]-[35]

The advantages of FinFETs are higher technological, maturity than planar DG, suppressed short channel effect, better in driving current, more compact and low cost. Applications of FinFETs are plausibility to spare power emerges when the two gates can be controlled independently, and at long last separate access to the two gates could likewise be utilized to configuration rearranged rationale gates. This would likewise lessen power, and spare chip zone, prompting littler, more cost proficient plans.[36-39]

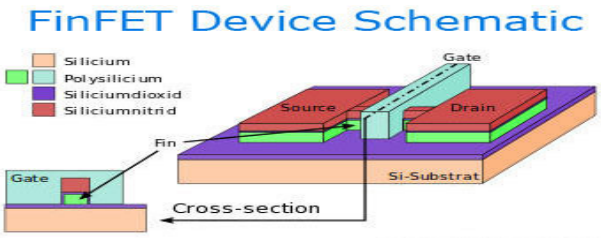


Fig. 2: **FinFET schematic**

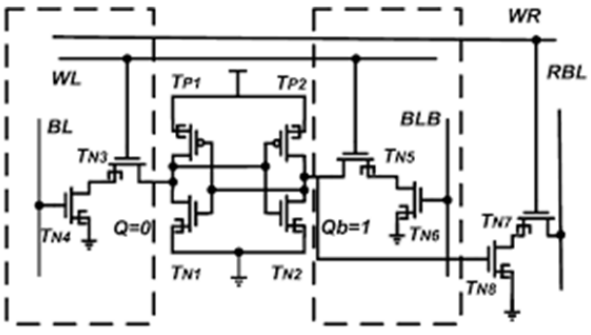


Fig. 3: 10T SRAM cell circuit

Proposed SRAM circuits Using FinFET Models

In READ '0' operation RBL line is precharged to VDD and WR is kept HIGH. By keeping the WL line as LOW, the write access FETs (TN3 & TN5) are in OFF state. As RBL and WR are ON TN7 is ON. If QB is logic HIGH, then TN8 is ON. As TN7 and TN8 are ON, RBL discharges to GND through TN7 and TN8. As RBL discharged we can verify that the value stores in QB is logic HIGH ('1'). In READ '1' operation RBL line is precharged to VDD and WR is kept at logic '1'. The WL line is kept LOW, the write access FETs (TN3 and TN5) are in OFF state. As RBL and WR are ON, TN7 is ON. If QB is logic LOW, then TN8 is OFF. As TN7 is ON and TN8 is OFF, RBL can't discharges to GND through TN7 and TN8. As RBL won't discharged we can verify that the value stores in QB is logic LOW ('0'). In WRITE operation, the data which has to be written is loaded on BL and BLB through write driver. For WRITE operation, WL is set to HIGH and WR, RBL is set LOW. In WRITE '1' operation BL is made '0' and BLB as '1'. TN5 and TN6 are ON in this state. As QB is '1' in WRITE '1' operation, Qb discharges through TN5 and TN6 to GND making QB as LOW. As QB is LOW, Q is logic HIGH ('1'). In WRITE '0' operation WL, BL are HIGH then TN3 and TN4 are ON. As Q is '1' in WRITE '0' state, Q discharges to GND through TN3 and TN4 making Q as logic LOW ('0').

In WRITE operation WWL is logic HIGH, RWL is HIGH, As WWL is HIGH MN3 is ON. If BLB is HIGH and L is logic LOW, then the voltage at L and BLB should be the same making L as '1' i.e. WRITE '1' operation and if BLB is logic LOW, then WRITE '0' operation is performed. In READ operation WWL and RWL are logic LOW. As RWL is LOW, MN7 is OFF. As WWL is LOW, MN3 AND MN4 are OFF. DATA inside the cell gets HOLD i.e. no WRITE operation is possible making the data stored inside the inverted pair.

In READ operation RWL is logic HIGH, RBL is precharged to VDD. RBL (read bit line) provides read operation output. If the value stored in QB is LOW then N5 is OFF. N6 is ON as RWL is HIGH, as N5 is OFF RBL won't discharge to GND i.e RBL will be logic HIGH which is the same as the value stored in Q('1'). In READ'0' operation i.e assuming Q is LOW and QB as HIGH. As QB is HIGH, N5 is ON. RWL and RBL are HIGH which make N6 ON. RBL discharges to GND through N6 and N5, making RBL to '0'. As RBL is LOW it concludes that the bit stored in Q is logic LOW. In WRITE operation WL is logic HIGH, the access transistors N3 and N4 are ON allowing the data through BL and BLB which are input lines in WRITE operation. In WRITE '1' operation BLB is logic LOW and BL is logic HIGH. As N3 is ON the value of BL reflects at Q through N3 making the values stored in Q as HIGH. As BLB is logic LOW and N4 is ON, the value stored in QB will be LOW and the operation of WRITE '0' is same as WRITE '1' operation only the value of BLB and BL changes to HIGH and LOW to store logic LOW at Q.

In WRITE operation there are two cases which can be considered i.e WRITE '1' and WRITE 0' operations this both operations are performed in SRAM WRITE operation.BLB

Table 1: Truth table of 10T SRAM cell

Operation	*WL*	*BL*	*BLB*	*WR*	*RBL*	*Q*	*QB*
Write 1	1	0	1	0	0	1	0
Write 0	1	1	0	0	0	0	1
Read 1	0	1	1	1	1	1	0
Read 0	0	1	1	1	1	0	1
Hold 1	0	0	0	0	0	1	0
Hold 0	0	0	0	0	0	0	1

Table 2: Truth table of 9T SRAM cell

Operation	*WWL*	*BLB*	*BL*	*L*	*H*
Write 1	1	1	0	1	0
Write 0	1	0	1	0	1
Read 1	0	1	1	1	0
Read 0	0	1	1	0	1
Hold 1	0	0	0	1	0
Hold 0	0	0	0	0	1

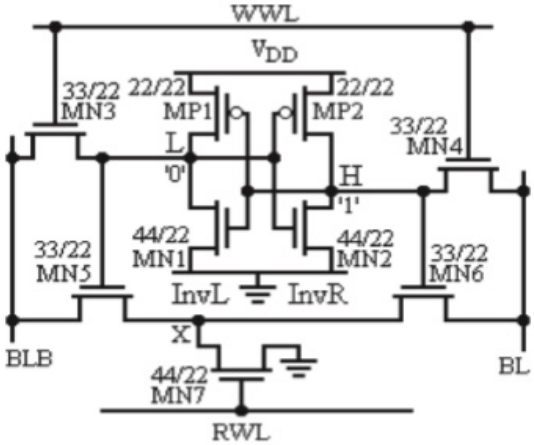


Fig. 4: 9T SRAM cell circuit

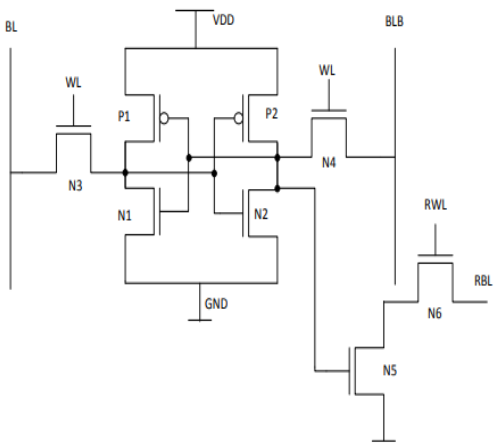


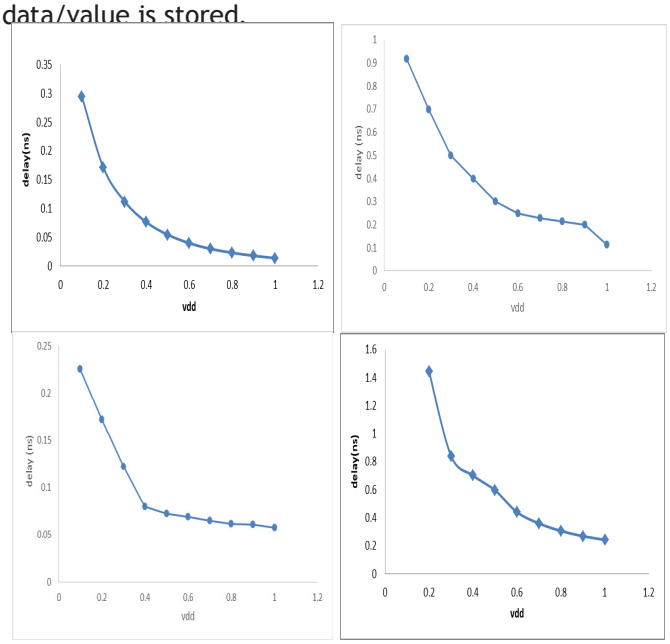
Fig. 4: 5T SRAM cell circuit

and BL are input lines in WRITE operation. In WRITE '0' W is logic LOW making N5 OFF, WL is logic HIGH making N3 ON. BLB is logic LOW as N3 is ON the value at BLB reflects at the node Q making Q logic LOW. Same operation is done in WRITE '1' operation the only difference is that BLB is logic HIGH which makes the values stored in Q to be HIGH ('1'). In READ operation the value stored inside Q is known. W is logic HIGH making N5 ON in READ operation. RL is logic HIGH making N4 ON. BL is precharged to VDD and WL is inactive i.e. logic LOW. If the values stored is LOW then BL discharges or else if the value stored is HIGH then BL won't discharge by which the values stored can be known in 7T SRAM cell.

Simulation Results and Experimental Findings of the Proposed Work

As seen in the waveform whenever WL is HIGH i.e. logic '1' and BL is logic '1' write'0' operation is carried out and when BL is logic '0' then write '1' operation is carried out making Q as '1' as seen in the waveform above. QB is the complementary to Q as in the waveform and RBL is ON i.e. logic '1' in read operation only. In HOLD operation WL, WR, RBL are logic '1' by not allowing read or write operation to proceed and making Q value as same value before the operation is taken place as in the waveform.

The waveform depicts the write, read operations, where WWL is logic '1' in write operation. We can see that L is logic HIGH in write '1' operation and H is logic LOW. In write '0' operation H is logic HIGH ('1') and is logic LOW ('0'). WWL is '0' in read operation has seen in the waveform above allowing to read the value stored in the loop of the inverters connected in cross coupled manner which is an important part in the Cell in which data/value is stored.



(a) 7T (b) 8T

(c) 9T (d) 10T

Φιγ. 1. Representation of Delay Vs VDD

Φιγ. 2.

Table 3: Truth table of 10T SRAM cell

Operation	*WL*	*BL*	*BLB*	*RWL*	*RBL*	*Q*	*QB*
Write 1	1	1	0	0	0	1	0
Write 0	1	0	1	0	0	0	1
Read 1	0	1	1	1	1	1	0
Read 0	0	1	1	1	1	0	1
Hold 1	0	0	0	0	0	1	0
Hold 0	0	0	0	0	0	0	1

Table 4: Truth table of 7T SRAM cell

Operation	*WL*	*BLB*	*BL*	*RL*	*W*	*Q*	*QB*
Write 1	1	0	1	0	0	1	0
Write 0	1	1	0	0	0	0	1
Read 1	0	1	1	1	1	1	0
Read 0	0	1	1	1	1	0	1
Hold 1	0	0	0	0	0	1	0
Hold 0	0	0	0	0	0	0	1

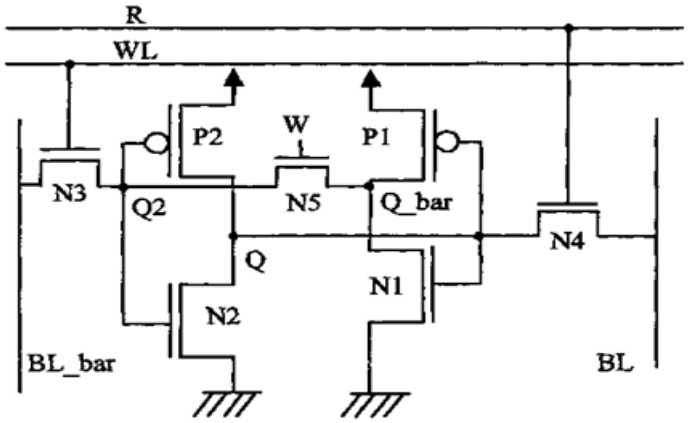


Fig. 5: 7T SRAM cell circuit

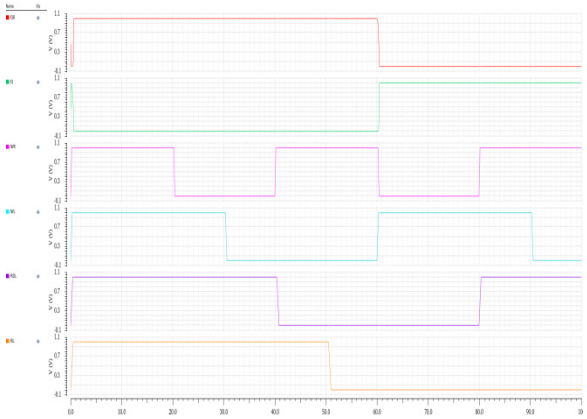


Fig. 6: Timing diagram of 10T SRAM

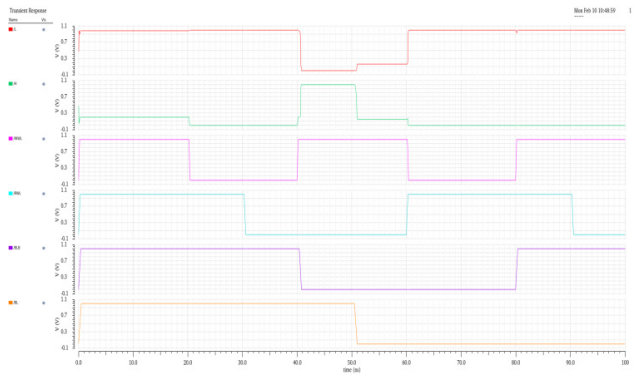


Fig. 7: Timing diagram of 10T SRAM

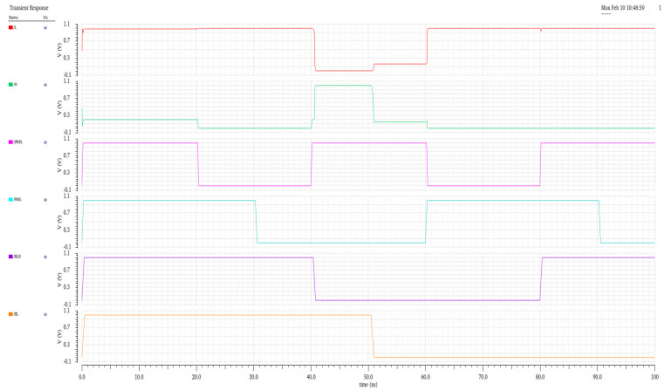
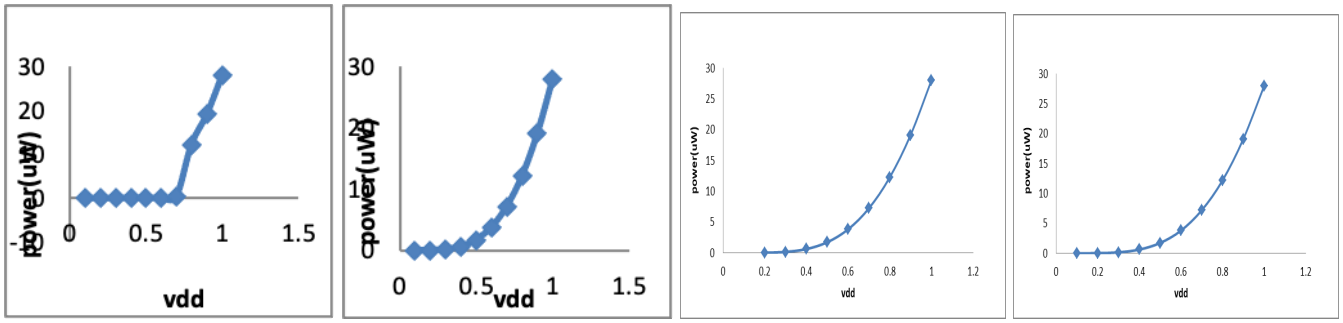
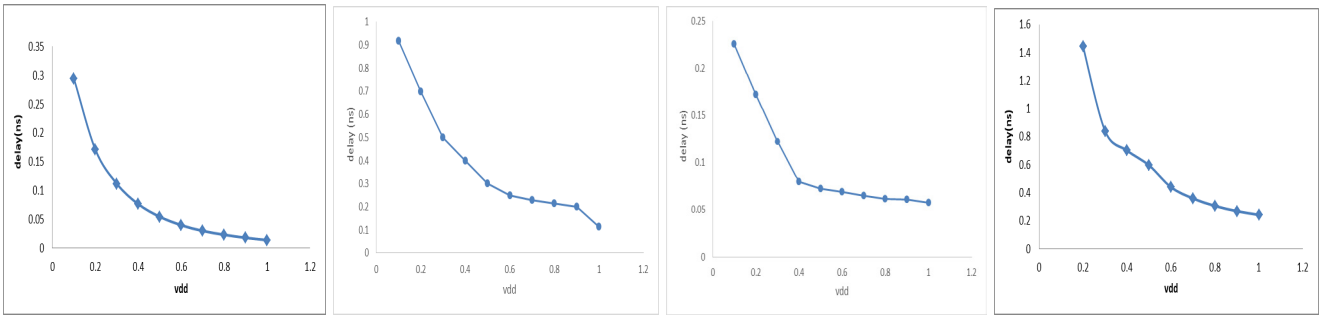


Fig. 8: Timing diagram of 9T SRAM



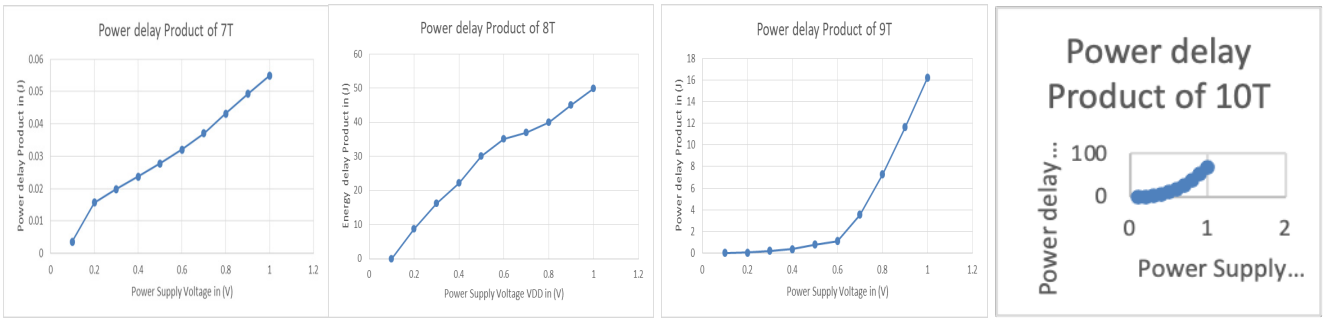
(a) 7T (b) 8T (c) 9T (d) 10T

Fig. 9: Representation of Power Vs VDD



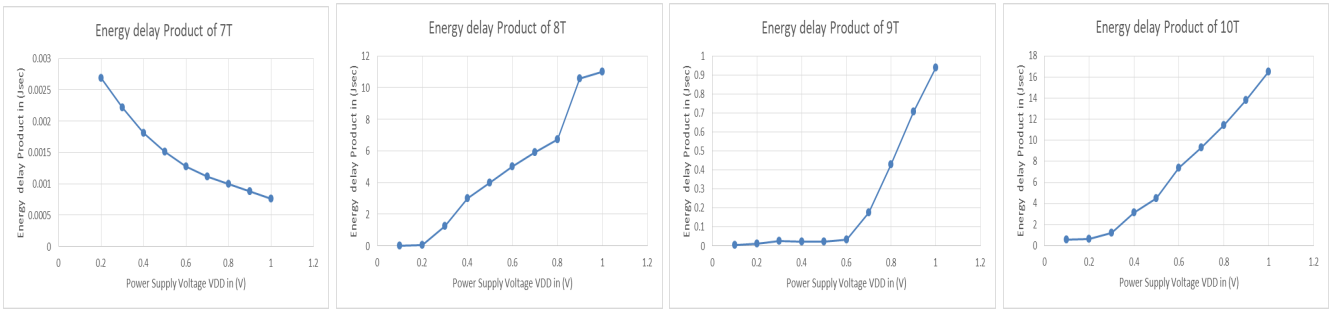
(a) 7T (b) 8T (c) 9T (d) 10T

Fig. 10: Representation of Delay Vs VDD



(a) 7T (b) 8T (c) 9T (d) 10T

Fig. 11: Representation of PDP Vs VDD



(a) 7T (b) 8T (c) 9T (d) 10T

Fig. 12: Representation of EDP Vs VDD

Conclusion

In this study, impacts of FinFET on SRAM Cells have been analyzed. It presents 10T, 9T, 8T and 7TSRAM Cells analyzed in 18nm Fine technology node using Cadence virtuoso Tool. The performance evaluations of the mentioned SRAM cells are carried out in Cadence virtuoso Tool. The design of 10TSRAM Cell has stable read and write operations unlike in 6T SRAM Cell. The parameters of 10T, 9T, 8T, 7T SRAM Cell can be compared and application suitable SRAM Cell can be used based on the results present in FinFET technology. Parameters like power, delay, power delay product, energy delay product are calculated and analyzed for10T, 9T, 8T, 7T SRAM Cells. Compared to the previous work on CMOS SRAM, the analysis on FinFET SRAM Cells has very low power consumption and read access time and less PDP values. The outcomes appears FinFET based SRAM is quicker, dependable and the force utilization is fundamentally decreased and offers great exchange offs at lower technology nodes.

References

[1] M.Muzammil Khaleeq, Kartik Penshanwar, Ananiah Durai S, Ravi V. “Design of low power SRAM Array with enhanced RNM,” by IJEAT ISSN:2249-8958, volume issue-4, in April 2019.

[2] Kiran, K. Uday, Gowtham Mamidisetti, Chandra shaker Pittala, V. Vijay, and Rajeev Ratna Vallabhuni, “A PCCN-Based Centered Deep Learning Process for Segmentation of Spine and Heart: Image Deep Learning,” In Handbook of Research on Technologies and Systems for E-Collaboration During Global Crises, pp. 15-26. IGI Global, 2022.

[3] Vallabhuni Vijay, V.R. Seshagiri Rao, Kancharapu Chaitanya, S. China Venkateshwarlu, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, “High-Performance IIR Filter Implementation Using FPGA,” 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[4] Jujavarapu Sravana, S.K. Hima Bindhu, K. Sharvani, P. Sai Preethi, Saptarshi Sanyal, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, “Implementation of Spurious Power Suppression based Radix-4 Booth Multiplier using Parallel Prefix Adders,” 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-6.

[5] Chandra Shaker Pittala, Vallabhuni Vijay, A. Usha Rani, R. Kameshwari, A. Manjula, D.Haritha, Rajeev Ratna Vallabhuni, “Design Structures Using Cell Interaction Based XOR in Quantum Dot Cellular Automata,” 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[6] S. China Venkateshwarlu, Mohammad khadir, V. Vijay, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, “Optimized Design of Power Efficient FIR Filter Using Modified Booth Multiplier,” 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[7] G. Naveen, V.R Seshagiri Rao, Nirmala. N, Pavan kalyan. L, Vallabhuni Vijay, S. China Venkateswarlu, Rajeev Ratna Vallabhuni, “Design of High-Performance Full Adder Using 20nm CNTFET Technology,” 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[8] Ratna, Vallabhuni Rajeev, and Ramya Mariserla. “Design and Implementation of Low Power 32-bit Comparator.” (2021).

[9] Vallabhuni Vijay, Kancharapu Chaitanya, T. Sai Jaideep, D. Radha Krishna Koushik, B. Sai Venumadhav, Rajeev Ratna Vallabhuni, “Design of Optimum Multiplexer In Quantum-Dot Cellular Automata,” International Conference on Innovative Computing, Intelligent Communication and Smart Electrical systems (ICSES -2021), Chennai, India, September 24-25, 2021.

[10] S. Sushma, S. Swathi, V. Bindusree, Sri Indrani Kotamraju, A. Ashish Kumar, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, “QCA Based Universal Shift Register using 2 to 1 Mux and D flip-flop,” IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3’21) 7th Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[11] M. Sreevani, S. Lakshmanachari, B. Manvitha, Y.J.N. Pravalika, T.Praveen,V.Vijay, Rajeev Ratna Vallabhuni, “Design of Carry Select Adder Using Logic Optimization Technique,” IEEE 2021 International Conference on Advances in Computing, Communication and Control (ICAC3’21) 7th

Edition (3rd and 4th December 2021), Mumbai, Maharashtra, India, December 03-04, 2021, pp. 1-6.

[12] S. Swathi, S. Sushma, C. Devi Supraja, V. Bindusree, L. Babitha and Vallabhuni Vijay, "A Hierarchical Image Matting Model for Blood Vessel Segmentation in Retinal Images," International journal of system assurance engineering and management, vol. 13, iss. 3, 2022, pp. 1093-1101.

[13] Bandi Mary Sowbhagya Rani, Vasumathi Devi Majety, Chandra Shaker Pittala, Vallabhuni Vijay, Kanumalli Satya Sandeep, Siripuri Kiran, "Road Identification Through Efficient Edge Segmentation Based on Morphological Operations," Traitement du Signal, vol. 38, no. 5, Oct. 2021, pp. 1503-1508.

[14] M. Lavanya, Malla Jyothsna Priya, Ponukumatla Janet, Kavuluri Pavan Kalyan, and Vijay Vallabhuni, "Advanced 18nm FinFET Node Based Energy Efficient and High-Speed Data Comparator using SR Latch," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[15] M. Saritha, Chelle Radhika, M. Narendra Reddy, M. lavanya, A. Karthik, Vallabhuni Vijay, Rajeev Ratna Vallabhuni, "Pipelined Distributive Arithmetic-based FIR Filter Using Carry Save and Ripple Carry Adder," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[16] S. Swathi, S. Sushma, V. Bindusree, L Babitha, Sukesh Goud. K, S. Chinavenkateswarlu, V. Vijay, Rajeev Ratna Vallabhuni, "Implementation of An Energy-Efficient Binary Square Rooter Using Reversible Logic By Applying The Non-Restoring Algorithm," Second IEEE International Conference on Communication, Computing and Industry 4.0 (C2I4-2021), Bengaluru, Karnataka, India, December 16-17, 2021, pp. 1-6.

[17] Mohammad khadir, S. Shakthi, S. Lakshmanachari, Vallabhuni Vijay, S. China Venkateswarlu, P. Saritha, Rajeev Ratna Vallabhuni, "QCA Based Optimized Arithmetic Models," 4th International Conference on Recent Trends in Computer Science and Technology (ICRTCST-2021), Jamshedpur, India, February 11-12, 2022, pp. 1-5.

[18] P. Ashok Babu, P. Sridhar, and Rajeev Ratna Vallabhuni, "Fake Currency Recognition System Using Edge Detection," 2022 Interdisciplinary Research in Technology and Management (IRTM), Kolkata, India, February 24-26, 2022, pp. 1-5.

[19] Koteshwaramma, K. C., Vallabhuni Vijay, V. Bindusree, Sri Indrani Kotamraju, Yasala Spandhana, B. Vasu D. Reddy, Ashala S. Charan, Chandra S. Pittala, and Rajeev R. Vallabhuni, "ASIC Implementation of An Effective Reversible R2B Fft for 5G Technology Using Reversible Logic," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 5-13.

[20] Vijay, Vallabhuni, Kancharapu Chaitanya, Chandra Shaker Pittala, S. Susri Susmitha, J. Tanusha, S. China Venkateshwarlu, and Rajeev Ratna Vallabhuni, "Physically Unclonable Functions Using Two-Level Finite State Machine," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 33-41.

[21] Vijay, Vallabhuni, M. Sreevani, E. Mani Rekha, K. Moses, Chandra S. Pittala, KA Sadulla Shaik, C. Koteshwaramma, R. Jashwanth Sai, and Rajeev R. Vallabhuni, "A Review On N-Bit Ripple-Carry Adder, Carry-Select Adder And Carry-Skip Adder," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 27-32.

[22] Vijay, Vallabhuni, Chandra S. Pittala, A. Usha Rani, Sadulla Shaik, M. V. Saranya, B. Vinod Kumar, RES Praveen Kumar, and Rajeev R. Vallabhuni, "Implementation of Fundamental Modules Using Quantum Dot Cellular Automata," Journal of VLSI circuits and systems, vol. 4, no. 01, 2022, pp. 12-19.

[23] Gollamandala Udaykiran Bhargava, Vasujadevi Midasala, and Vallabhuni Rajeev Ratna, "FPGA implementation of hybrid recursive reversable box filter-based fast adaptive bilateral filter for image denoising," Microprocessors and Microsystems, vol. 90, 2022, 104520.

[24] Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, Vallabhuni Vijay, Usha Rani Anam, Kancharapu Chaitanya, "Numerical analysis of various plasmonic MIM/MDM slot waveguide structures," International Journal of System Assurance Engineering and Management, 2022.

[25] Chandra Shaker Pittala, Vallabhuni Vijay, B. Naresh Kumar Reddy, "1-Bit FinFET Carry Cells for Low Voltage High-Speed Digital Signal Processing Applications," Silicon, 2022. https://doi.org/10.1007/s12633-022-02016-8.

[26] M. Saritha, M. Lavanya, G. Ajitha, Mulinti Narendra Reddy, P. Annapurna, M. Sreevani, S. Swathi, S. Sushma, Vallabhuni Vijay, "A VLSI design of clock gated technique based ADC lock-in amplifier," International Journal of System Assurance Engineering and Management, 2022, pp. 1-8. https://doi.org/10.1007/s13198-022-01747-6

[27] K. C. Koteswaramma, Ande Shreya, N. Harsha Vardhan, Kantem Tarun, S. China Venkateswarlu, and Vallabhuni Vijay, "ASIC Implementation of division circuit using reversible logic gates applicable in ALUs," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.

[28] Vallabhuni Vijay, J. Sravana, K.S. Indrani, G. Ajitha, A. Prashanth, K. Nagaraja, K.C. Koteswaramma, C. Radhika, M. Hima Bindu, N. Manjula, "A System for Controlling Positioning According To Movement Of Terminal In Wireless Communication Based On Ai Interface," The Patent Office Journal No. 50/2021, India. Application No. 202141055995 A.

[29] Dr. L.V. Narasimha Prasad, Dr. Vijay Vallabhuni, Dr. S. China Venkateswarlu, Dr. V. Vhandra Jagan Mohan, Ms. P. Sruthilaya, Mr. K. Tarun Kumar, Mr. B. Raju, Mr. P. Ravinder, "Garbage Collector with Smart Segregation and Method of Segregation Thereof," The Patent Office Journal No. 04/2022, India. Application No. 202141062270 A.

[30] Sravana, J., K. S. Indrani, M. Saranya, P. Sai Kiran, C. Reshma, and Vallabhuni Vijay, "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer," Journal of VLSI circuits and systems, vol. 4, no. 2, 2022, pp. 14-21.

[31] V. Vijay, J. Prathiba, S. Niranjan Reddy, V. Raghavendra Rao, "Energy efficient CMOS Full-Adder Designed with TSMC 0.18µm Technology," International Conference on Technology and Management (ICTM-2011), Hyderabad, India, June 8-10, 2011, pp. 356-361.

[32] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Optimal design of VLSI implemented Viterbi decoding," Na-

tional conference on Recent Advances in Communications & Energy Systems, (RACES-2011), Vadlamudi, India, December 5, 2011, pp. 67-71.

[33] Ch. Srivalli, S. Niranjan reddy, V. Vijay, J. Pratibha, "Low power based optimal design for FPGA implemented VMFU with equipped SPST technique," National Conference on Emerging Trends in Engineering Application (NCETEA-2011), India, June 18, 2011, pp. 224-227.

[34] Vallabhuni Vijay, and Avireni Srinivasulu, "A Novel Square Wave Generator Using Second Generation Differential Current Conveyor," Arabian Journal for Science and Engineering, vol. 42, iss. 12, 2017, pp. 4983–4990.

[35] Vallabhuni Vijay, Pittala Chandra shekar, Shaik Sadulla, Putta Manoja, Rallabhandy Abhinaya, Merugu rachana, and Nakka nikhil, "Design and performance evaluation of energy efficient 8-bit ALU at ultra low supply voltages using FinFET with 20nm Technology," VLSI Architecture for Signal, Speech, and Image Processing, edited by Durgesh Nandan, Basant Kumar Mohanty, Sanjeev Kumar, Rajeev Kumar Arya, CRC press, 2021.

[36] B. M. S. Rani, Vallabhuni Rajeev Ratna, V. Prasanna Srinivasan, S. Thenmalar, and R. Kanimozhi, "Disease prediction based retinal segmentation using bi-directional ConvLSTMU-Net," Journal of Ambient Intelligence and Humanized Computing, 2021, pp. 1-10. https://doi.org/10.1007/s12652-021-03017-y

[37] Vallabhuni Vijay, C. V. Sai Kumar Reddy, Chandra Shaker Pittala, Rajeev Ratna Vallabhuni, M. Saritha, M. Lavanya, S. China Venkateswarlu and M. Sreevani, "ECG Performance Validation Using Operational Transconductance Amplifier with Bias Current," International Journal of System Assurance Engineering and Management, vol. 12, iss. 6, 2021, pp. 1173-1179.

[38] J. Sravana, K.S. Indrani, Sankeerth Mahurkar, M. Pranathi, D. Rakesh Reddy, and Vijay Vallabhuni, "Optimised VLSI Design of Squaring Multiplier using Yavadunam Sutra through Deficiency Bits Reduction," International Conference On Advances In Signal Processing And Communication Engineering (ICASPACE 2021), Hyderabad, India, July 29-31, 2021.

[39] L. Babitha, U. Somanaidu, CH. Poojitha, K. Niharika, V. Mahesh, and Vallabhuni Vijay, "An Efficient Implementation of Programmable IIR Filter for FPGA," 1st International Conference on Innovations in Signal Processing and Embedded systems (ICISPES-2021), Hyderabad, India, October 22-23, 2021.